

WHAT IS CLAIMED IS:

1. A method for fabricating a fan-out wafer-level package for one or more integrated circuit (IC) dies, the method comprising:
 - providing a silicon substrate layer having a first thickness;
 - forming one or more active/passive devices comprising at least sources and drains and one or more diffusion layers adjoining the sources and drains, wherein forming the one or more active/passive devices comprises forming the sources and the drains in a front-end-of-line (FEOL) layer on a first side of the silicon substrate layer while forming the one or more diffusion layers at locations in the silicon substrate layer adjoining the sources and the drains;
 - forming a redistribution layer (RDL) over the FEOL layer by copper damascene formation of multiple metallization layers for connecting the one or more active/passive devices to the one or more IC dies when the one or more IC dies are mounted on a side of the RDL opposite the FEOL layer;
 - thinning the silicon substrate layer to a second thickness to form a thinned silicon substrate, the thinned silicon substrate comprising at least the one or more diffusion layers; and
 - patterning the thinned silicon substrate to form one or more silicon regions, each of the one or more silicon regions comprising the one or more diffusion layers.
2. The method of claim 1, wherein forming the one or more active/passive devices further comprises forming one or more shallow trench isolation (STI) regions in the silicon substrate layer, and wherein the thinned silicon substrate further comprises the one or more STI regions, the patterning step comprising patterning the thinned silicon substrate to form the one or more silicon regions, the one or more silicon regions comprising the one or more diffusion layers and the one or more STI regions.

3. The method of claim 1, wherein thinning the silicon substrate layer comprises backgrinding or cleaving the silicon substrate layer.
4. The method of any one of claims 1 to 3, wherein patterning the thinned silicon substrate comprises etching the thinned silicon substrate to form the one or more silicon regions.
5. The method of any one of claims 1 to 4, further comprising:
 - after the patterning step, depositing a SiN chemical vapor deposition layer over the one or more silicon regions and the FEOL layer as a diffusion barrier layer to prevent metal contamination of the one or more silicon regions during subsequent processing.
6. The method of claim 5, further comprising:
 - depositing a nonconductive material over the diffusion barrier layer to form a buffer layer; and
 - forming one or more conductive contacts through the buffer layer, the diffusion layer and the FEOL layer to connect to connections in the RDL, the one or more conductive contacts formed through areas of the buffer layer, the diffusion barrier layer and the FEOL layer that do not comprise the one or more active/passive devices nor the one or more diffusion layers of the one or more active/passive devices.
7. The method of claim 6, wherein forming the one or more conductive contacts comprises:
 - forming one or more openings through the buffer layer, the diffusion barrier layer and the FEOL layer; and
 - depositing conductive material at least onto sides of the one or more openings.
8. The method of claim 5, further comprising:

depositing a nonconductive material over the diffusion barrier layer to form a buffer layer; and

forming a plurality of conductive contacts through the buffer layer, the diffusion barrier layer and the FEOL layer, the step of forming the plurality of conductive contacts comprising:

forming a first set of one or more contact openings through the buffer layer, the diffusion barrier layer and the FEOL layer to connect to connections in the RDL, and

forming a second set of one or more contacts openings through the buffer layer and the diffusion barrier layer to connect to a backside of at least one of the one or more active/passive devices; and

depositing conductive material at least onto sides of the first and second sets of one or more contact openings.

9. The method of any one of claims 1 to 5 and 8, wherein the thinning step further comprises:

depositing one or more metal layers over the thinned silicon substrate layer to enhance backside conductive connection to the one or more silicon regions.

10. The method of any one of claims 1 to 9, further comprising after the one or more IC dies are mounted on the side of the RDL opposite the FEOL layer, encapsulating the one or more IC dies with resin.

11. The method of any one of claims 1 to 10, further comprising after the one or more IC dies are mounted on the side of the RDL opposite the FEOL layer and encapsulated by resin, attaching a stiffener plate onto the one or more IC dies.

12. A fan-out wafer-level package (FO-WLP) for mounting one or more integrated circuit (IC) dies thereon, comprising:

a redistribution layer (RDL) comprising metallization layers for connecting the one or more IC dies to one or more active/passive devices when the one or more IC dies are mounted on a first side of the RDL;

a front-end-of-line (FEOL) layer, wherein a first side of the FEOL layer adjoins a second side of the RDL and has the one or more active/passive devices partly formed therein, the second side of the RDL opposite the first side of the RDL; and

one or more silicon regions formed on a second side of the FEOL layer, wherein one or more diffusion layers of the one or more active/passive devices are formed in the one or more silicon regions.

13. The FO-WLP of claim 12, further comprising:

a nonconductive material layer formed over the one or more silicon regions and the second side of the FEOL layer.

14. The FO-WLP of claim 12 or 13, further comprising a diffusion barrier layer formed over the second side of the FEOL layer and the one or more silicon regions and below the nonconductive material layer.

15. The FO-WLP of claim 13 or 14, further comprising:

a first set of one or more conductive contacts formed through the nonconductive material layer and the FEOL layer to connect to connections in the RDL, the first set of one or more conductive contacts passing through the FEOL layer at locations other than where the one or more active/passive devices are formed.

16. The FO-WLP of claim 15, wherein the first set of one or more conductive contacts comprises at least a conductive layer formed along sides of one or more openings formed through the nonconductive material layer and the FEOL layer to provide connection from the RDL to outside the FO-WLP, wherein the first set of one or more conductive contacts are formed through areas of the nonconductive material layer and the FEOL layer that do not comprise the one or more active/passive devices.
17. The FO-WLP of any one of claims 13 to 16, further comprising:
a second set of one or more conductive contacts formed through the nonconductive material layer to provide connection from a backside of at least one of the one or more active/passive devices to outside the FO-WLP.