DESCRIPTION

Title of Invention: SEMICONDUCTOR DEVICE PRODUCTION METHOD AND SEMICONDUCTOR DEVICE

Technical Field

[0001]

The present invention relates to a semiconductor device production method and a semiconductor device.

Background Art

[0002]

The degree of integration of semiconductor integrated circuits, in particular, integrated circuits that use MOS transistors, continues to increase. With the increase in the degree of integration, MOS transistors used in the circuits have been miniaturized to a nanometer scale. With miniaturization of MOS transistors, issues have arisen in that reducing leakage current has become difficult and decreasing the area occupied by circuits has become difficult due to need of securing the required amount of current. In order to address these issues, a surrounding gate transistor (hereinafter referred to as an "SGT") has been proposed in which a source, a gate, and a drain are arranged in a direction perpendicular to a substrate and a gate electrode surrounds a pillar-shaped semiconductor layer (for example, refer to PTL 1, PTL 2, and PTL 3).

[0003]

According to an SGT production method of related art, a silicon pillar with a pillar-shaped nitride film hard mask is formed, a diffusion layer is formed below the silicon pillar, and then a gate material is deposited. Subsequently, the gate material is planarized and etched back to form an insulating film side wall on side walls of the silicon pillar and the nitride film hard mask. Then a resist pattern for a gate line is formed, the gate material is etched, the nitride film hard mask is removed, and a diffusion layer is formed in an upper portion of the silicon pillar so as to produce an SGT (for example, refer to PTL 4).

[0004]

As the distance between adjacent silicon pillars decreases, it becomes necessary to deposit a thick gate material between such silicon pillars and very small holes called voids are sometimes formed between the silicon pillars according to the above-mentioned method. If such voids are formed, holes are formed in the gate material after etch back. If an insulating film is subsequently deposited between the silicon pillars to form an insulating film side wall, the insulating film is deposited in the voids as well. Accordingly, it becomes difficult to process the gate material that lies between silicon pillars.

[0005]

To address this, a technique that involves the following has been disclosed (for example, refer to NPL 1): A gate oxide film is formed after formation of a silicon pillar. After a thin polysilicon is deposited, a resist for forming a gate line covering an upper portion of the silicon pillar is formed. The gate line is etched, a thick oxide film is deposited, an upper portion of the silicon pillar is exposed, and a thin polysilicon on the upper portion of the silicon pillar is removed. Lastly, the thick oxide film is removed by wet etching.

[0006]

However, according to the related art, a technique that uses metal in gate electrodes is not demonstrated. Moreover, formation of a resist is necessary to form a gate line that covers the upper portion of the silicon pillar; since the resist covers the upper portion of the silicon pillar, the process is not a self-aligned process.

Citation List

Patent Literature

[0007]

[PTL 1] Japanese Unexamined Patent Application Publication No. 2-71556

[PTL 2] Japanese Unexamined Patent Application Publication No. 2-188966

[PTL 3] Japanese Unexamined Patent Application

Publication No. 3-145761

[PTL 4] Japanese Unexamined Patent Application Publication No. 2009-182317

[0008]

[NPL 1] B. Yang, K.D. Buddharaju, S.H.G. Teo, N. Singh, G.D. Lo, and D.L. Kwong, "Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET", IEEE Electron Device Letters, VOL. 29, No. 7, July 2008, pp 791-794.

Summary of Invention

Technical Problem

[0009]

An object of the present invention is to provide a method for producing a semiconductor device having an SGT structure, with which a gate electrode composed of a metal material is formed by a self-aligned process by using a thin gate material, and to provide an SGT structure obtained by the method.

Solution to Problem

[0010]

A first aspect of the present invention provides a semiconductor device production method that includes

a first step of forming a planar semiconductor layer on a semiconductor substrate and forming a first pillar-shaped semiconductor layer and a second pillar-shaped semiconductor layer on the planar semiconductor layer;

after the first step, a second step of

forming a gate insulating film around the first pillar-shaped semiconductor layer and the second pillar-shaped semiconductor layer,

forming a metal film and a polysilicon film around the gate insulating film,

controlling a thickness of the polysilicon film to be smaller than a half of a distance between the first pillar-shaped semiconductor layer and the second pillar-shaped semiconductor layer, and

depositing a third resist, exposing the polysilicon film on side walls of upper portions of the first pillar-shaped semiconductor layer and the second pillar-shaped semiconductor layer, removing the exposed polysilicon film by etching, stripping the third resist, and removing the metal film by etching; and

after the second step,

a third step of forming a fourth resist for forming a gate line and performing anisotropic etching to form a gate line, a first gate electrode, and a second gate electrode.

[0011]

Preferably, after the first step,

a step of forming oxide film hard masks on the first pillar-shaped silicon layer and the second pillar-shaped silicon layer and forming an oxide film on the planar

silicon layer, the oxide film being thicker than the gate insulating film is further contained.

Preferably, a height of an upper surface of the fourth resist is less than a height of an upper surface of the polysilicon film that has undergone the second step.

[0012]

A fourth step of forming a first n-type diffusion layer in an upper portion of the first pillar-shaped semiconductor layer, forming a second n-type diffusion layer in a lower portion of the first pillar-shaped semiconductor layer and an upper portion of the planar semiconductor layer, forming a first p-type diffusion layer in an upper portion of the second pillar-shaped semiconductor layer, and forming a second p-type diffusion layer in a lower portion of the second pillar-shaped semiconductor layer and an upper portion of the planar semiconductor layer is preferably further contained.

[0013]

A sixth step of forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line is preferably further contained.

[0014]

A second aspect of the present invention provides a semiconductor device that includes

a planar semiconductor layer formed on a semiconductor substrate;

first and second pillar-shaped semiconductor layers formed on the planar semiconductor layer;

a first gate insulating film formed around the first pillar-shaped semiconductor layer;

a first gate electrode having a laminated structure constituted by a metal film and a polysilicon film formed around the first gate insulating film;

a second gate insulating film formed around the second pillar-shaped semiconductor layer;

a second gate electrode having a laminated structure constituted by a metal film and a polysilicon film formed around the second gate insulating film;

a gate line connected to the first and second gate electrodes;

an oxide film formed between the gate line and the planar semiconductor layer and having a thickness larger than that of the gate insulating film;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped semiconductor layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped semiconductor layer and an upper portion of the planar semiconductor layer;

a first p-type diffusion layer formed in an upper

portion of the second pillar-shaped semiconductor layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped semiconductor layer and an upper portion of the planar semiconductor layer.

A thickness of the polysilicon film is preferably smaller than a half of a distance between the first pillar-shaped semiconductor layer and the second pillar-shaped semiconductor layer.

A height of an upper surface of the metal film is preferably more than a height of an upper surface of the polysilicon film.

A height of an upper surface of the gate line is preferably less than a height of upper surfaces of the first and second gate electrodes.

[0015]

The gate line preferably has a laminated structure constituted by the metal film and a silicide.

[0016]

Preferably, there is a particular offset between a center line of the gate line and a line that connects a center point of the first pillar-shaped semiconductor layer and a center point of the second pillar-shaped semiconductor layer.

[0017]

Preferably, silicides formed on the first and second n-

type diffusion layers and the first and second p-type diffusion layers are further included.

Advantageous Effects of Invention

[0018]

The present invention provides a metal-gate SGT production method through a self-aligned process that uses a thin gate material, and an SGT structure obtained by this method.

Brief Description of Drawings

[0019]

[Fig. 1] (A) is a plan view of a semiconductor device according to an embodiment of the present invention, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 2] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 3] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 4] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and

(C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 5] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 6] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 7] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 8] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 9] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 10] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 11] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 12] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 13] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 14] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 15] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 16] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 17] (A) is a plan view showing a semiconductor

device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 18] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 19] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 20] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 21] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 22] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 23] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B)

is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 24] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 25] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 26] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 27] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 28] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 29] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and

(C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 30] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 31] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 32] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 33] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 34] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 35] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 36] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 37] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 38] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 39] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

[Fig. 40] (A) is a plan view showing a semiconductor device production method according to this embodiment, (B) is a cross-sectional view taken along line X-X' in (A), and (C) is a cross-sectional view taken along line Y-Y' in (A).

Description of Embodiments

[0020]

A semiconductor device having an SGT structure produced by a semiconductor device production method according to an embodiment of the present invention has the following

structure.

[0021]

As shown in Fig. 1, a semiconductor device that has an SGT structure according to this embodiment includes a planar silicon layer 107 formed on a silicon substrate 101, first and second pillar-shaped silicon layers 104 and 105 formed on the planar silicon layer 107, a gate insulating film 113 formed around the first pillar-shaped silicon layer 104, and a first gate electrode 119b having a laminated structure constituted by a metal film 115 and a polysilicon film 116 formed around the gate insulating film 113.

[0022]

A gate insulating film 114, a second gate electrode 119a having a laminated structure constituted by the metal film 115 and the polysilicon film 116 formed around the gate insulating film 114, and a polysilicon film 116 are formed around the second pillar-shaped silicon layer 105.

The gate insulating film 114, the second gate electrode 119a having a laminated structure constituted by the metal film 115 and the polysilicon film 116 formed around the gate insulating film 114, and the polysilicon film 116 each have a thickness smaller than a half of a distance between the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105; and the height of the upper surface of the metal film 115 is more than the height of the

upper surface of the polysilicon film 116.

The height of the upper surface of a gate line 119c connected to the first and second gate electrodes 119b and 119a is less than the height of the upper surfaces of the first and second gate electrodes 119b and 119a.

[0023]

The semiconductor device having an SGT structure according to this embodiment further includes a second oxide film 110 that is formed between the gate line 119c and the planar silicon layer 107 and has a thickness larger than that of the gate insulating films 113 and 114, a first n-type diffusion layer 121 formed in an upper portion of the first pillar-shaped silicon layer 104, a second n-type diffusion layer 122 formed in a lower portion of the first pillar-shaped silicon layer 104 and in an upper portion of the planar silicon layer 107, a first p-type diffusion layer 124 formed in an upper portion of the second pillar-shaped silicon layer 105, and a second p-type diffusion layer 125 formed in a lower portion of the second pillar-shaped silicon layer 105 and an upper portion of the planar silicon layer 107.

[0024]

A method for producing a semiconductor device having an SGT structure according to an embodiment of the present invention will now be described with reference to Figs. 2 to

40.

[0025]

Provided below is a detailed description of a first step of forming a planar silicon layer 107 (planar semiconductor layer) on a silicon substrate 101 (semiconductor substrate), and forming a first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and a second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer) on the planar silicon layer 107.

[0026]

As shown in Fig. 2, first, first resists 102 and 103 for forming a first pillar-shaped silicon layer 104 and a second pillar-shaped silicon layer 105 are formed on a silicon substrate 101. In this embodiment, a silicon substrate 101 is used as a substrate for forming a semiconductor device but the substrate may be any other substrate used in production of semiconductor devices.

[0027]

Next, as shown in Fig. 3, the silicon substrate 101 is etched to form a first pillar-shaped silicon layer 104 and a second pillar-shaped silicon layer 105 under the first resists 102 and 103. Here, the pillar-shaped silicon layers are formed by using a hard mask such as an oxide film or a nitride film.

[0028]

Subsequently, as shown in Fig. 4, the first resists 102 and 103 are stripped and removed.

[0029]

Subsequently, as shown in Fig. 5, a second resist 106 for forming a planar silicon layer 107 is formed.

[0030]

Subsequently, as shown in Fig. 6, the silicon substrate 101 is etched to form a planar silicon layer 107 under the second resist 106.

[0031]

Subsequently, as shown in Fig. 7, the second resist 106 is stripped and removed.

[0032]

Subsequently, as shown in Fig. 8, an element isolation film 108 is formed around the planar silicon layer 107.

[0033]

Subsequently, as shown in Fig. 9, a first oxide film 109 is deposited so as to cover the first pillar-shaped silicon layer 104, the second pillar-shaped silicon layer 105, and the planar silicon layer 107. Here, the oxide film 109 is preferably deposited by normal-pressure CVD (chemical vapor-phase deposition). When a first oxide film 109 is deposited by normal-pressure CVD, a thick first oxide film 109 is deposited on the first pillar-shaped silicon layer 104, the second pillar-shaped silicon layer 105, and the

planar silicon layer 107, and a thin first oxide film 109 is deposited on side walls of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105. According to the normal-pressure CVD, the thickness of the first oxide film 109 deposited on the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 is larger than the thickness of the first oxide film 109 deposited on the planar silicon layer 107.

[0034]

Subsequently, as shown in Fig. 10, the oxide film 109 is removed by isotropic etching so as to form oxide film hard masks 111 and 112 on the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105. A second oxide film 110 thicker than gate insulating films 113 and 114 (refer to Fig. 11) is formed on the planar silicon layer 107.

[0035]

The description above has shown the first step of forming a planar silicon layer 107 (planar semiconductor layer) on a silicon substrate 101 (semiconductor substrate), forming a first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and a second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer) on the planar silicon layer 107.

[0036]

Described in detail next is a second step that involves the following: Gate insulating films 113 and 114 (refer to Fig. 11) are formed around the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer), and a metal film 115 and a thin polysilicon film 116 are formed around the gate insulating films 113 and 114. Here, the thickness of the polysilicon film 116 is adjusted to be smaller than a half of the distance between the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer). Then a third resist 117 is deposited from above the polysilicon film 116, and the polysilicon film 116 on side walls of upper portions of the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer) are exposed from the third resist 117. Then the polysilicon film 116 exposed from the third resist 117 is removed by etching, the third resist 117 is stripped, and the metal film 115 is removed by etching.

[0037]

As shown in Fig. 11, first, gate insulating films 113 and 114 are formed around the first pillar-shaped silicon

layer 104 and the second pillar-shaped silicon layer 105, and a metal film 115 and a thin polysilicon film 116 are formed around the gate insulating films 113 and 114. Since a thin polysilicon is used, occurrence of voids in the polysilicon film 116 is prevented. Here, titanium nitride is used as a material for the metal film 115 but any metal, such as titanium nitride, that is capable of setting a threshold voltage of a transistor and used in semiconductor production processes can be used as a material for the metal film 115. Those used in semiconductor processes, such as oxide films, oxynitride films, and high-k dielectric films, can be used as the gate insulating films 113 and 114.
[0038]

Subsequently, as shown in Fig. 12, a third resist 117 is deposited, and the polysilicon film 116 on side walls of upper portions of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 is exposed from the third resist 117. Preferably, resist etch back is employed to expose the polysilicon film 116 on the side walls of the upper portions. Alternatively, the polysilicon film 116 on the side walls of the upper portions may be exposed by using a coating film such as spin-on-glass.
[0039]

Subsequently, as shown in Fig. 13, the polysilicon film 116 exposed from the third resist 117 is removed by etching.

The polysilicon film 116 is preferably removed by isotropic dry etching.

[0040]

Subsequently, as shown in Fig. 14, the third resist 117 is removed.

[0041]

Subsequently, as shown in Fig. 15, the metal film 115 is removed by etching. In removing the metal film 115 on the upper portion of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 by etching, the metal film 115 that lies between the polysilicon film 116 and the first pillar-shaped silicon layer 104 and between the polysilicon film 116 and the second pillar-shaped silicon layer 105 will be etched if wet etching is employed, and voids may occur between the polysilicon film 116 and the first pillar-shaped silicon layer 104 and between the polysilicon film 116 and the second pillar-shaped silicon layer 105.

[0042]

The description above has shown the second step that involves the following: Gate insulating films 113 and 114 are formed around the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer), and a metal film 115 and a thin

polysilicon film 116 are formed around the gate insulating films 113 and 114. Here, the thickness of the polysilicon film 116 is controlled to be smaller than a half of the distance between the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer). Then a third resist 117 is deposited from above the polysilicon film 116, and the polysilicon film 116 on side walls of upper portions of the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer) are exposed from the third resist 117. Then the polysilicon film 116 exposed from the third resist 117 is removed by etching, the third resist 117 is stripped, and the metal film 115 is removed by etching.

[0043]

Described in detail next is a third step of forming a fourth resist 118 for forming a gate line 119c and performing anisotropic etching so as to form a gate line 119c, a first gate electrode 119b, and a second gate electrode 119a.

[0044]

Subsequently, as shown in Fig. 16, first, a fourth resist 118 for forming a gate line 119c (refer to Fig. 17)

is formed. The height of the upper surface of the fourth resist 118 is preferably less than the height of the upper surface of the polysilicon film 116 that has undergone the second step. By employing anisotropic etching in forming the gate line 119c, the polysilicon film 116 above the first and second gate electrodes 119a and 119b (refer to Fig. 17) is removed and thus the height of the upper surface of the metal film 115 can be made more than the height of the upper surface of the polysilicon film 116.

[0045]

Moreover, in the step shown in Fig. 16, the third resist 117 is preferably formed so that there is a particular offset (refer to Fig. 17) between the center line of the fourth resist 118 for forming a gate line 119c and the line connecting the center point of the first pillar-shaped silicon layer 104 and the center point of the second pillar-shaped silicon layer 105. When there is a particular offset as such, it becomes easier to form a silicide 135 (refer to Fig. 28) that connects a second n-type diffusion layer 122 to a second p-type diffusion layer 125.

[0046]

Subsequently, as shown in Fig. 17, the polysilicon film 116 and the metal film 115 are etched to form first and second gate electrodes 119a and 119b, and a gate line 119c. As a result, a self-aligned process is realized. In this

embodiment, it is sufficient to merely bring a fourth resist 118 for forming the gate line 119c into contact with the gate electrodes 119a and 119b formed around the silicon pillars. In this manner, the margin for alignment for the gate line 119c is increased and thus a self-aligned process is realized. During this process, upper portions of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 are protected by the oxide film hard masks 111 and 112. Furthermore, since the polysilicon film 116 above the first gate electrode 119b and the second gate electrode 119a is removed by anisotropic etching, the height of the upper surface of the metal film 115 can be controlled to be more than the height of the upper surface of the polysilicon film 116.

[0047]

Subsequently, as shown in Fig. 18, the second oxide film 110 is removed by etching.

[0048]

Subsequently, as shown in Fig. 19, the fourth resist 118 is stripped and removed.

[0049]

The description above has shown the third step of forming a fourth resist 118 for forming a gate line 119c and performing anisotropic etching so as to form a gate line 119c, a first gate electrode 119b, and a second gate

electrode 119a.

[0050]

Described in detail next is a fourth step that involves the following: A first n-type diffusion layer 121 is formed in an upper portion of the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and a second n-type diffusion layer 122 is formed in a lower portion of the first pillar-shaped silicon layer 104 and an upper portion of the planar silicon layer 107 (planar semiconductor layer). Then a first p-type diffusion layer 124 is formed in an upper portion of the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer) and a second p-type diffusion layer 125 is formed in a lower portion of the second pillar-shaped silicon layer 105 and an upper portion of the planar silicon layer 107.

[0051]

As shown in Fig. 20, a fifth resist 120 for forming a first n-type diffusion layer 121 and a second n-type diffusion layer 122 is formed. Note that a thin oxide film may be deposited on an upper surface of the planar silicon layer 107 prior to forming the fifth resist 120.

[0052]

Subsequently, as shown in Fig. 21, arsenic (As) is implanted into an upper portion and a lower portion of the first pillar-shaped silicon layer 104 so as to form a first

n-type diffusion layer 121 and a second n-type diffusion layer 122.

[0053]

Subsequently, as shown in Fig. 22, the fifth resist 120 is stripped and removed.

[0054]

Subsequently, as shown in Fig. 23, a sixth resist 123 for forming a first p-type diffusion layer 124 and a second p-type diffusion layer 125 (refer to Fig. 24) is formed.

[0055]

Subsequently, as shown in Fig. 24, boron or boron fluoride is implanted into an upper portion and a lower portion of the second pillar-shaped silicon layer 105 to form a first p-type diffusion layer 124 and a second p-type diffusion layer 125.

[0056]

Subsequently, as shown in Fig., 25, the sixth resist 123 is stripped and removed.

[0057]

Subsequently, as shown in Fig. 26, an oxide film 126 and a nitride film 127 are deposited to form uniform layers, and a heat treatment is conducted.

[0058]

The description above has shown the fourth step that involves the following: A first n-type diffusion layer 121

is formed in an upper portion of the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and a second n-type diffusion layer 122 is formed in a lower portion of the first pillar-shaped silicon layer 104 and an upper portion of the planar silicon layer 107 (planar semiconductor layer). Then a first p-type diffusion layer 124 is formed in an upper portion of the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer) and a second p-type diffusion layer 125 is formed in a lower portion of the second pillar-shaped silicon layer 105 and an upper portion of the planar silicon layer 107.

[0059]

Described in detail next is a fifth step of forming silicides 131, 135, 132, 134, 130, and 133 on the first n-type diffusion layer 121, the second n-type diffusion layer 122, the first p-type diffusion layer 124, the second p-type diffusion layer 125, and the gate line 119c.

[0060]

As shown in Fig. 27, first, the oxide film 126 and the nitride film 127 are partly removed by etching so as to form insulating film side walls 128a, 128b, 129a, 129b, and 129c.

[0061]

Subsequently, as shown in Fig. 28, a metal material is deposited and a heat treatment is performed to remove unreacted metal materials so as to form silicides 131, 135,

132, 134, 130, and 133 on the first n-type diffusion layer 121, the second n-type diffusion layer 122, the first p-type diffusion layer 124, the second p-type diffusion layer 125, and the gate line 119c. Here, the insulating film side walls may be nitride film side walls.

[0062]

As a result, the second n-type diffusion layer 122 connects to the second p-type diffusion layer 125 via the silicide 135. As shown in Fig. 17, since there is a particular offset between the center line of the gate line 119c and the line connecting the center point of the first pillar-shaped silicon layer 104 and the center point of the second pillar-shaped silicon layer 105, formation of the silicide 135 is easy. Consequently, high integration of semiconductor devices is achieved.

[0063]

According to this structure, since the polysilicon film 116 is thin, the gate line 119c can be easily formed to have a laminated structure constituted by the metal film 115 and the silicide 130. Since the silicide 130 and the metal film 115 come in direct contact with each other in the gate line 119c, the resistance of the gate line 119c is decreased.

[0064]

The description above has shown the fifth step of forming silicides 131, 135, 132, 134, 130, and 133 on the

first n-type diffusion layer 121, the second n-type diffusion layer 122, the first p-type diffusion layer 124, the second p-type diffusion layer 125, and the gate line 119c.

[0065]

Subsequent to the fifth step, as shown in Fig. 29, a contact stopper 136 such as a nitride film is deposited to form a layer that covers the entire structure so as to form an interlayer insulating film 137.

[0066]

Subsequently, as shown in Fig. 30, a seventh resist 138 for forming contact holes 139 and 140 (refer to Fig. 31) is formed.

[0067]

Subsequently, as shown in Fig. 31, the interlayer insulating film 137 is etched to form contact holes 139 and 140 in openings of the seventh resist 138.

[0068]

Subsequently, as shown in Fig. 32, the seventh resist 138 is stripped and removed.

[0069]

Subsequently, as shown in Fig. 33, an eighth resist 141 for forming contact holes 142 and 143 (refer to Fig. 34) is formed.

[0070]

Subsequently, as shown in Fig. 34, the interlayer insulating film 137 is etched to form contact holes 142 and 143 in openings of the eighth resist 141.

[0071]

Subsequently, as shown in Fig. 35, the eighth resist 141 is stripped and removed.

[0072]

Subsequently, as shown in Fig. 36, the contact stopper 136 is etched to remove the contact stopper 136 under the contact holes 139 and 140 and the contact holes 142 and 143.

[0073]

Subsequently, as shown in Fig. 37, a metal material is deposited to form a metal layer 148 so as to form contacts 144, 145, 146, and 147 that form connections with conductor layers at lower levels.

[0074]

Subsequently, as shown in Fig. 38, ninth resists 149, 150, 151, and 152 for forming metal lines 153, 154, 155, and 156 (refer to Fig. 39) are formed.

[0075]

Subsequently, as shown in Fig. 39, the metal layer 148 is etched to form metal lines 153, 154, 155, and 156.

[0076]

Subsequently, as shown in Fig. 40, the ninth resists 149, 150, 151, and 152 are stripped and removed.

The description above has shown the method for producing a semiconductor device having an SGT structure in which a gate electrode composed of a metal material is formed by using a thin gate material (polysilicon) by a self-aligned process.

[0077]

Since the height of the upper surface of the metal film 115 is more than the height of the upper surface of the polysilicon film 116, voids do not occur between the polysilicon film 116 and the first pillar-shaped silicon layer 104 and between the polysilicon film 116 and the second pillar-shaped silicon layer 105, and the decrease in the capacity between the gate electrodes 119a and 119b and the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 can be prevented.

[0078]

A semiconductor device having an SGT produced by this embodiment includes a second oxide film 110 thicker than the gate insulating films 113 and 114 formed between the gate line 119c and the planar silicon layer 107. Thus, the capacity between the gate line 119c and the silicon substrate 101 can be decreased and insulation between the gate line 119c and the silicon substrate 101 is ensured.

[0079]

According to this embodiment, the gate line 119c is

formed of a laminated structure constituted by a metal film 115 and a silicide 130. As such, since the silicide 130 and the metal film 115 in the gate line 119c make direct contact to each other, the resistance of the gate line 119c is decreased.

[0080]

According to this embodiment, there is a particular offset (refer to Fig. 17) between the center line of the gate line 119c and the line connecting the center point of the first pillar-shaped silicon layer 104 and the center point of the second pillar-shaped silicon layer 105. Accordingly, a silicide 135 that connects the second n-type diffusion layer 122 to the second p-type diffusion layer 125 can be easily formed. As a result, high-integration of semiconductor devices is achieved on a mass production basis.

[0081]

According to the embodiment described above, the first step is followed by a second step that involves the following: Gate insulating films 113 and 114 are formed around the first pillar-shaped silicon layer 104 (first pillar-shaped semiconductor layer) and the second pillar-shaped silicon layer 105 (second pillar-shaped semiconductor layer) after the first step. Subsequently, a metal film 115 and a thin polysilicon film 116 are formed around the gate

insulating films 113 and 114. The thickness of the polysilicon film 116 is to be smaller than a half of the distance between the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105. Then a third resist 117 is deposited and the polysilicon film 116 on side walls of upper portions of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 is exposed. Then the exposed polysilicon film 116 is removed by etching, the third resist 117 is stripped, and the metal film 115 is removed by etching. This second step is followed by a third step of forming a fourth resist 118 for forming a gate line 119c and performing anisotropic etching so as to form a gate line 119c, a first gate electrode 119b, and a second gate electrode 119a. As a result, a self-aligned process is realized. According to this embodiment, since a semiconductor device is produced by a self-aligned process, there is no need to use a mask formed of a different member and thus high integration of semiconductor devices is achieved.

[0082]

In removing the metal film 115 on the upper portion of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 by etching, the metal film 115 that lies between the polysilicon film 116 and the first pillar-shaped silicon layer 104 and between the polysilicon

film 116 and the second pillar-shaped silicon layer 105 will be etched if wet etching is employed. As a result, voids may occur between the polysilicon film 116 and the first pillar-shaped silicon layer 104 and between the polysilicon film 116 and the second pillar-shaped silicon layer 105. If voids occur as such, the specific dielectric constant (ratio of the dielectric constant of a medium to the dielectric constant of vacuum, $\varepsilon/\varepsilon 0 = \varepsilon r$) of the part where voids occurred turns out to be approximately 1 (1.00059) which is about the same as that of air and thus the capacity between the gate electrodes 119a and 119b and the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 is decreased. However, in this embodiment, the gate line 119c is formed by anisotropic etching after the metal film 115 on the upper portions of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 is removed by etching. During this process, since the polysilicon film 116 that lies above the first and second gate electrodes 119b and 119a is removed by anisotropic etching, the height of the upper surface of the metal film 115 can be controlled to be more than the height of the upper surface of the polysilicon film 116. Accordingly, occurrence of voids between the polysilicon film 116 and the first pillar-shaped silicon layer 104 and between the polysilicon film 116 and the second pillar-

shaped silicon layer 105 can be prevented.

[0083]

Note that various embodiments and modifications of the present invention are possible without departing from the broad spirit and scope of the present invention. The embodiment described above is merely illustrative and does not limit the scope of the present invention. The embodiments and modifications can be freely combined. Omitting some of the features of the embodiment as needed is also within the technical idea of the present invention.

[0084]

For example, in the embodiment described above, a method for producing a semiconductor device in which p-type (including p^+-type) and n-type (including n^+-type) are revered, and a semiconductor device obtained by such a method naturally fall within the technical scope of the present invention.

Industrial Applicability

[0085]

According to a semiconductor device production method of the present invention, a semiconductor device that is highly integrated and has SGTs can be produced.

Reference Signs List

101. silicon substrate

102. first resist

103. first resist

104. first pillar-shaped silicon layer

105. second pillar-shaped silicon layer

106. second resist

107. planar silicon layer

108. element isolation film

109. oxide film

110. second oxide film

111. oxide film hard mask

112. oxide film hard mask

113. gate insulating film

114. gate insulating film

115. metal film

116. polysilicon film

117. third resist

118. fourth resist

119a. second gate electrode

119b. first gate electrode

119c. gate line

120. fifth resist

121. first n-type diffusion layer

122. second n-type diffusion layer

123. sixth resist

124. first p-type diffusion layer

125. second p-type diffusion layer

126. oxide film

127. nitride film

128a. insulating film side wall

128b. insulating film side wall

129a. insulating film side wall

129b. insulating film side wall

129c. insulating film side wall

130. silicide

131. silicide

132. silicide

133. silicide

134. silicide

135. silicide

136. contact stopper

137. interlayer insulating film

138. seventh resist

139. contact hole

140. contact hole

141. eighth resist

142. contact hole

143. contact hole

144. contact

145. contact

146. contact

147. contact

148. metal layer

149. ninth resist

150. ninth resist

151. ninth resist

152. ninth resist

153. metal line

154. metal line

155. metal line

156. metal line

CLAIMS

[Claim 1]

A semiconductor device production method comprising:

a first step of forming a planar semiconductor layer on a semiconductor substrate and forming a first pillar-shaped semiconductor layer and a second pillar-shaped semiconductor layer on the planar semiconductor layer;

after the first step, a second step of

forming a gate insulating film around the first pillar-shaped semiconductor layer and the second pillar-shaped semiconductor layer,

forming a metal film and a polysilicon film around the gate insulating film,

controlling a thickness of the polysilicon film to be smaller than a half of a distance between the first pillar-shaped semiconductor layer and the second pillar-shaped semiconductor layer, and

depositing a third resist, exposing the polysilicon film on side walls of upper portions of the first pillar-shaped semiconductor layer and the second pillar-shaped semiconductor layer, removing the exposed polysilicon film by etching, stripping the third resist, and removing the metal film by etching; and

after the second step,

a third step of forming a fourth resist for forming a

gate line and performing anisotropic etching to form a gate line, a first gate electrode, and a second gate electrode.

[Claim 2]

The semiconductor device production method according to Claim 1, further comprising, after the first step,

a step of forming oxide film hard masks on the first pillar-shaped silicon layer and the second pillar-shaped silicon layer and forming an oxide film on the planar silicon layer, the oxide film being thicker than the gate insulating film.

[Claim 3]

The semiconductor device production method according to Claim 1, wherein a height of an upper surface of the fourth resist is less than a height of an upper surface of the polysilicon film that has undergone the second step.

[Claim 4]

The semiconductor device production method according to Claim 1, further comprising a fourth step of forming a first n-type diffusion layer in an upper portion of the first pillar-shaped semiconductor layer, forming a second n-type diffusion layer in a lower portion of the first pillar-shaped semiconductor layer and an upper portion of the planar semiconductor layer, forming a first p-type diffusion layer in an upper portion of the second pillar-shaped semiconductor layer, and forming a second p-type diffusion

layer in a lower portion of the second pillar-shaped semiconductor layer and an upper portion of the planar semiconductor layer.

[Claim 5]

The semiconductor device production method according to Claim 4, further comprising a sixth step of forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.

[Claim 6]

A semiconductor device comprising:

a planar semiconductor layer formed on a semiconductor substrate;

first and second pillar-shaped semiconductor layers formed on the planar semiconductor layer;

a first gate insulating film formed around the first pillar-shaped semiconductor layer;

a first gate electrode having a laminated structure constituted by a metal film and a polysilicon film formed around the first gate insulating film;

a second gate insulating film formed around the second pillar-shaped semiconductor layer;

a second gate electrode having a laminated structure constituted by a metal film and a polysilicon film formed around the second gate insulating film;

a gate line connected to the first and second gate electrodes;

an oxide film formed between the gate line and the planar semiconductor layer and having a thickness larger than that of the gate insulating film;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped semiconductor layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped semiconductor layer and an upper portion of the planar semiconductor layer;

a first p-type diffusion layer formed in an upper portion of the second pillar-shaped semiconductor layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped semiconductor layer and an upper portion of the planar semiconductor layer,

wherein a thickness of the polysilicon film is smaller than a half of a distance between the first pillar-shaped semiconductor layer and the second pillar-shaped semiconductor layer,

a height of an upper surface of the metal film is more than a height of an upper surface of the polysilicon film, and

a height of an upper surface of the gate line is less than a height of upper surfaces of the first and second gate electrodes.

[Claim 7]

The semiconductor device according to Claim 6, wherein the gate line has a laminated structure constituted by the metal film and a silicide.

[Claim 8]

The semiconductor device according to Claim 7, wherein there is a particular offset between a center line of the gate line and a line that connects a center point of the first pillar-shaped semiconductor layer and a center point of the second pillar-shaped semiconductor layer.

[Claim 9]

The semiconductor device according to Claim 8, further comprising silicides formed on the first and second n-type diffusion layers and the first and second p-type diffusion layers.