

## DESCRIPTION

**TITLE: Method for production of an SOI structure which in particular is designed for photonic applications, and support substrate for the said structure**

### FIELD OF THE INVENTION:

The field of the present invention is that of semiconductors and microelectronics. It concerns a method for production of an SOI (Silicon On Insulator) structure, which in particular is suitable for photonic applications. The invention also concerns a support substrate for the said structure.

### TECHNOLOGICAL BACKGROUND OF THE INVENTION:

In the field of photonics on SOI, certain techniques for coupling of the optical fibres to the components make it necessary to produce V-grooves by anisotropic chemical etching in the support substrate of the SOI structure, to a depth of approximately 50 to 80µm. In addition, it is increasingly in demand to co-integrate components, thus making it possible to connect the front face and the rear face of the SOI structure electrically. Connection of this type is conventionally carried out by means of TSVs (Through Silicon Via) conductors provided by etching of the support substrate of the SOI structure, typically to a depth of 50 to 100µm. It should be noted that the support structure is thicker than 100µm throughout the processes for production of the SOI structure and production of the components, but it is habitually thinned at the rear face in these ranges of thickness, which makes it possible to recuperate the electrical contact by means of the via(s) opening out.

The presence of defects in the support substrate, such as in particular micro-defects (BMDs – Bulk Micro-Defects) which are well known in the monocrystalline silicon industry, can disrupt the etching of the V-grooves or vias, and give rise to subsequent failures of the components. These BMD micro-defects are derived from precipitation of interstitial oxygen on preferential nucleation sites (for example vacancies), and are not favourable when deep etchings such as the aforementioned types are provided in the support substrate.

In addition, the production of SOI structures requires thermal budgets at very high temperatures. It can in particular implement the Smart Cut™ method for the transfer of the useful monocrystalline silicon layer (c-Si) onto the support substrate, via an intermediate dielectric layer. The well-known Smart Cut method is based on the implantation of light ions into a c-Si donor substrate, in order to form an embedded fragile plane which, together with the front face of the donor substrate, defines the useful layer to be transferred. The implanted donor substrate is then assembled on the support substrate. In

general, a dielectric layer is formed on the donor substrate, on the support substrate, or on both substrates, before the assembly: this dielectric layer is designed to form the embedded insulating layer of the SOI structure. The following step consists of separation along the embedded fragile plane, giving rise firstly to an intermediate structure comprising the useful layer transferred onto the support substrate via the dielectric layer, and secondly the remainder of the donor substrate.

After the separation of the useful layer and its transfer onto the support substrate, heat treatments are required to smooth the free surface of the useful layer, and eliminate crystalline defects present therein. This requires the support substrate of the SOI structure to be resistant to failure modes of the slip lines type, marks, or other deformations which are liable to be generated during the heat treatment, as a result of temperature gradients or points of contact between the substrate and maintenance elements in the furnace. In order to protect the support substrate against these failures, it is advantageous for it to have a BMD micro-defect density which is sufficient and homogeneous both radially and in depth, which micro-defects make it resistant to mechanical deformation. In addition, the BMD micro-defects permit trapping of substances (in particular metal contamination) in the support substrate, thus limiting the diffusion of contaminants as far as the useful layer during the production of the components.

#### **SUBJECT OF THE INVENTION:**

In order to reconcile the different constraints associated with the presence of BMD micro-defects in the support substrate of an SOI structure, the present invention proposes a method for production of an SOI structure which in particular is designed for photonic applications, the support structure of which comprises:

- a surface layer which is depleted in BMD micro-defects, with a thickness of more than 40µm, typically between 40µm and 100µm; and
- a deep layer which is rich in BMD micro-defects, in order to guarantee stable mechanical behaviour of the support substrate, and thus of the SOI structure, during its production and during production of the components.

#### **BRIEF DESCRIPTION OF THE INVENTION:**

The present invention concerns a method for production of an SOI structure, comprising the following steps:

a) supply of an initial monocrystalline silicon substrate, with an interstitial oxygen content of between 15 and 27 ppma, in accordance with the standard ASTM'79, and resistivity lower than 200 ohms.cm, with the initial substrate being designed to form a support substrate for the SOI structure after having undergone the subsequent step b);

b) implementation of a sequence of heat treatments to the initial substrate while, at least on a front face, it is without a layer of silicon oxide, other than optionally a layer of native oxide, the said sequence consisting of:

- a first heat treatment defined by a plateau at a temperature higher than 1200°C and lower than 1280°C, and with a duration of between 1 second and 60 seconds, by a temperature decrease ramp of between 10°C/s and 70°C/s, and by an atmosphere of an argon or argon-hydrogen type, followed by:
- a second heat treatment defined by a plateau at a temperature of between 900°C and 1100°C, without a stage before this temperature, under a neutral or oxidising atmosphere, in order to form a support substrate comprising:
  - a denuded surface layer, with a thickness greater than 40µm, and having a concentration of BMD micro-defects lower than  $10^8/\text{cm}^3$ ; and
  - an enriched deep layer, below the denuded surface layer, with a concentration of micro-defects of between  $2.10^8/\text{cm}^3$  and  $5.10^{10}/\text{cm}^3$ .

According to advantageous characteristics of the invention, taken alone or according to any achievable combination:

- the temperature of the plateau of the first heat treatment is between 1220°C and 1260°C;
- the second heat treatment is defined by temperature ramp-up and temperature ramp-down of between 0.5°C/min et 10°C/min;
- the temperature of the plateau of the second heat treatment is between 950°C and 1000°C;
- the atmosphere of the second heat treatment is oxidising, at least during the plateau, in order to form, on the support substrate, all or part of a silicon oxide dielectric layer, the said dielectric layer being designed to be positioned between a useful layer and the support substrate in the SOI structure;
- after the step b) of implementation of the sequence of heat treatments, the manufacturing method comprises a step c) of oxidation of the support substrate, in order to form on the support substrate all or part of a silicon oxide dielectric layer, the said dielectric layer being designed to be positioned between a useful layer and the support substrate in the SOI structure;
- the manufacturing method also comprises the following steps:
  - d) formation of an intermediate structure comprising the useful monocrystalline silicon layer positioned on the dielectric layer, which itself is positioned on the front face of the support substrate, by means of a thin-layer transfer technique;

- e) implementation of a third heat treatment to the intermediate structure, at a temperature of between 900°C and 1250°C, under a neutral or reductive atmosphere, in order to form the SOI structure.

The invention also concerns a monocrystalline silicon support substrate with:

- resistivity lower than 200 ohm.cm;
- a denuded surface layer, with a thickness greater than 40µm, and having a concentration of BMD micro-defects lower than  $10^8/\text{cm}^3$ ;
- an enriched deep layer, below the denuded layer, with a concentration of BMD micro-defects of between  $2 \cdot 10^8/\text{cm}^3$  and  $5 \cdot 10^{10}/\text{cm}^3$ .

The support substrate can comprise a silicon oxide dielectric layer at least on its front face.

Finally, the invention concerns an SOI structure comprising a useful layer positioned on the dielectric layer, which itself is positioned on a support substrate such as previously described.

The dielectric layer advantageously has a thickness of between 500nm and 2000nm.

#### **BRIEF DESCRIPTION OF THE DRAWINGS:**

Other characteristics and advantages of the invention will become apparent from the following detailed description, which is provided with reference to the appended figures, in which:

[Fig. 1a]

[Fig. 1b]

[Fig. 1c] Figures 1a, 1b and 1c show the steps of the manufacturing method of a support substrate for an SOI structure according to the invention;

[Fig. 2] Figure 2 shows an SOI structure comprising a support substrate according to the invention;

[Fig. 3] Figure 3 shows images in cross-section of support substrates according to the invention, obtained by light-scattering tomography (LST); the measurement, carried out on each cleaved support substrate, is based on the collection of the light diffused by the BMD micro-defects at the section of the said support substrate;

[Fig. 4] Figure 4 shows images in cross-section of support substrates which are not in conformity with the invention, which images are also obtained by LST.

Certain figures are schematic representations which, for the purpose of legibility, are not to scale. In particular, the thicknesses of the layers along the z axis are not to scale in relation to the lateral dimensions along the x and y axes.

#### **DETAILED DESCRIPTION OF THE INVENTION:**

The invention concerns a manufacturing method of an SOI structure 100 which is particularly suitable for photonic applications, which require in particular the formation of V-grooves and conductive vias in the support substrate 10 of the said structure 100. The SOI structure 100 comprises a thick embedded dielectric layer, typically of between 500nm and 2000nm.

The method firstly comprises a step a) corresponding to the supply of a CZ monocrystalline silicon initial substrate 10' (CZ for Czochralski's growth process). The initial substrate 10' has a front face 10a and a rear face 10b, which are substantially parallel to a main plane (x,y) (figure 1a). It advantageously has the form of a small plate with a circular form, and a diameter typically of between 200mm and 450mm. Its total thickness, along the axis z normal to the main plane (x,y), can vary between a few hundred microns (for example 300µm) and 1000µm.

The initial substrate 10' has an interstitial oxygen content of between 15 and 27ppma according to the standard ASTM'79. Its resistivity is lower than 200 ohms.cm, typically between 1 ohm.cm and 100 ohms.cm. The initial substrate 10' is designed to form a support substrate 10 for the SOI structure 100, after having undergone the subsequent step b).

The step b) corresponds to the implementation of a sequence of heat treatments to the bare initial substrate 10', i.e. which, on its front face 10a at least, is without any layer of silicon oxide other than optionally a layer of native oxide. The sequence consists of two successive heat treatments, without another thermal cycle interposed.

The first heat treatment is carried out in RTA (Rapid Thermal Anneal) equipment, and is defined by a temperature plateau, temperature ramp-up and temperature ramp-down, and a gaseous atmosphere. The temperature of the plateau is higher than 1200°C and lower than 1280°C. Advantageously, it is between 1220°C and 1260°C, or between 1220°C and 1250°C. The duration of the plateau can be

from 1 second to 60 seconds. The temperature ramp-down is between  $10^{\circ}\text{C/s}$  and  $70^{\circ}\text{C/s}$ . The temperature ramp-up is also rapid, but can be selected from a more extensive range than temperature ramp-down, in particular between  $10^{\circ}\text{C/s}$  and  $100^{\circ}\text{C/s}$ . The atmosphere during this first heat treatment is of the argon or argon-hydrogen type (typically  $\text{Ar} > 70\%$ ). A nitrogen atmosphere cannot be envisaged because an excessive number of vacancies is injected into the substrate, in particular via the front face 10a, which does not assist the thinning out of vacancies of a thick surface layer. An oxidising atmosphere is also proscribed, since it participates in compensating for the injection of vacancies, in particular into a deep layer of the substrate, which, on the contrary, it is wished to enrich with vacancies.

This first heat treatment applied to the bare initial substrate 10' makes it possible to generate a profile of vacancies in its depth, i.e. a low concentration of vacancies in a surface layer 11', 13', and a high concentration of vacancies in a deep layer 12'.

"Surface layer 11', 13'" means a layer, the thickness of which starts at a free face 10a, 10b of the initial substrate 10' (in particular its front face 10a, but potentially also its rear face 10b), and extends over a depth, equal to  $40\mu\text{m}$  or more, in the volume of the said substrate 10' (figure 1b). It should be noted that a surface layer 13' with a low concentration of vacancies can be formed on the side of the rear face 10b of the initial substrate 10', if this rear face 10b is – like the front face 10a – bare, during the first heat treatment.

"Deep layer 12'" means a layer which is situated below the surface layer 11' 13' (starting from the free face of the surface layer concerned), and extends in the volume of the initial substrate 10'. This deep layer with a high concentration of vacancies can for example extend between the surface layer 11' on the front face 10a, and that 13' on the rear face 10b of the initial substrate 10'. Later in the thermal sequence applied to the initial substrate 10', the vacancies will help to fix precipitations of oxygen where they are present, thus constituting preferential nucleation sites.

During the plateau of the first heat treatment, vacancies can be generated everywhere in the initial substrate 10', on the surface and in the depth, with a density which depends on the thermal budget applied. When the temperature descends, these vacancies are diffused very quickly, the probability that they will recombine on the surface is greater if they are close to the surface, and there is therefore a gradient of vacancies on the surface, which can be modulated in particular by the rate of the temperature ramp-down: the faster the descent, the more the vacancies will be fixed in place, and will recombine little on the surface, which gives rise to a thin, vacancy-depleted surface layer; the slower the descent, the more the gradient of concentration of vacancies will be pronounced, which results in a thicker surface layer. In this case, below a certain rate of temperature ramp-down, even the vacancies

which are situated deeply tend to diffuse and recombine on the surface, which has a negative impact on the deep layer which is expected to be rich in vacancies. The annealing atmosphere also has an impact: compared with an argon atmosphere, an argon-hydrogen environment adds participation of the hydrogen (which diffuses quickly in the initial substrate 10') in the passivation of the vacancies, on the surface but also deeper, which can make it possible to increase the thickness of the surface layer. On the other hand, in certain conditions of implementation, an Ar/H atmosphere can reduce the concentration of vacancies of the deep layer, which is not desirable.

The aforementioned conditions of the first heat treatment (temperatures of the plateau, ramps, durations, atmospheres) provide a good compromise for generation of a thick surface layer 11', 13' which is depleted with vacancies, typically of between 40µm and 100µm, and a deep layer 12' which is very rich in vacancies. In addition, these conditions prevent, or at least limit, the creation of defects such as slip lines SL or pinmarks PM, in or on the initial substrate 10', which defects are detrimental to the future SOI structure.

In the sequence according to the invention, the first heat treatment is followed by a second heat treatment, defined by a plateau at a temperature of between 900°C and 1100°C, without a stage before this temperature. Preferably, the temperature of the plateau is between 950°C and 1000°C. The duration of the plateau is typically between 2 hours and several tens of hours, for example 40 hours. The temperature ramp-up the temperature ramp-down are advantageously between 0.5°C/min and 10°C/min, and can optionally be different from one another. The atmosphere of the second heat treatment can be neutral or oxidising. This second heat treatment is advantageously carried out in a conventional furnace (with a vertical or horizontal tube).

The second heat treatment assists the precipitation of oxygen on the vacancies distributed in the substrate 10' according to the profile set during the first heat treatment. The precipitation is made possible by the presence of interstitial oxygen, which emphasises the importance of the choice of the range of interstitial oxygen contents of the initial substrate 10' made in step a) of the method.

The second heat treatment is also defined such as not to passivate or recombine the vacancies before they have helped to create BMD micro defects.

This sequence of heat treatments is essential for forming the support substrate 10 concerned, a denuded surface layer 11, 13 of which (obtained from the surface layer 11', 13'), with a thickness of 40µm or more, has a concentration of BMD micro-defects lower than  $10^8/\text{cm}^3$ , and an enriched deep

layer 12 of which (obtained from the deep layer 12'), below the denuded surface layer 11, 13, has a concentration of BMD micro-defects of between  $2 \cdot 10^8/\text{cm}^3$  and  $5 \cdot 10^{10}/\text{cm}^3$ . It should be remembered that the density and potentially the size of the BMD micro-defects are conventionally measured by light-scattering tomography (LST) at the section (on the plane (y,z) in the figures) of the support substrate 10. The support substrate 10 obtained also has excellent mechanical quality, with a very low density of defects of the SL or PM type, or even none of these defects, upon completion of the sequence of heat treatments. The absence (or very low density) of these defects, and the concentration of BMD micro-defects of  $2 \cdot 10^8/\text{cm}^3$  or more, will provide the support substrate 10 with great mechanical strength during subsequent heat treatments at high temperatures, and prevent failures of the slip line SL type in the future SOI structure (both during its own production and that of the components). The denuded surface layer 11, 13, which can extend over a thickness of between  $40\mu\text{m}$  and  $100\mu\text{m}$ , is particularly suitable for the formation of V-grooves or vias, during the production of components on and/or in the SOI structure 100.

According to a particular embodiment of the method, the atmosphere of the second heat treatment is oxidising, at least during the plateau, in order to form on the support substrate 10 all or part of a silicon oxide dielectric layer, the said dielectric layer 20 being designed to be positioned between a useful layer 30 and the support substrate 10 in the SOI structure 100. This embodiment is advantageous in that it makes it possible to combine two functions of the second heat treatment, and rationalise the thermal steps applied to the support substrate 10.

By way of example, in order to form a dielectric layer of  $2\mu\text{m}$  on the support substrate 10, the second heat treatment can be defined by temperatures ramp-up of a few degrees per minute, up to  $1000^\circ\text{C}$ , under an argon atmosphere with a low oxygen content, a plateau at a temperature of  $1000^\circ\text{C}$  under an oxidising atmosphere, and a temperature ramp-down of a few degrees per minute.

According to another embodiment, after the step b) of implementation of the sequence of heat treatments, the manufacturing method comprises a step c) of oxidation of the support substrate 10, in order to form on the said support substrate all or part of a silicon oxide dielectric layer; the dielectric layer 20 is designed to be positioned between a useful layer 30 and the support substrate 10 in the SOI structure 100. The step c) of oxidation does not have a negative effect on the denuded surface layer 11, 13 and the enriched deep layer 12, since the precipitation of oxygen on the vacancies has taken place during the second heat treatment. The step c) can thus induce an increase in the size of the BMD micro-defects.

It should be remembered that photonic applications on silicon in general require SOI structures comprising a thick embedded dielectric layer, typically of between 500nm and 2000nm. Since this thickness is significant, the dielectric layer 20 is grown preferably (or at least by far mostly) on the support substrate 10, since a large thickness of dielectric layer on the front face of the donor substrate (with reference to the Smart Cut method) makes it difficult to form the embedded fragile plane by means of ionic implantation.

Figure 3 shows two examples of a support substrate 10 produced in accordance with a method according to the invention. In particular, the sequence of step b) has consisted of a first heat treatment defined by a plateau at a temperature of between 1220°C and 1260°C, with a duration of between 1 second and 60 seconds, and by a temperature ramp-down of between 10°C/s and 70°C/s, followed by a second heat treatment defined by a plateau at a temperature of between 950°C and 1000°C, without a stage before this temperature, under an oxidising atmosphere. The images were obtained by LST. In both cases, there can be seen a denuded surface layer 11 and a deep layer 12 enriched with BMD; the thickness of the denuded surface layer 11 can be greater thanks to the implementation of an Ar/H atmosphere during the first heat treatment: in the left-hand image of figure 3, the thickness of the denuded surface layer 11 is approximately 70µm for an Ar atmosphere, whereas in the right-hand image, the thickness of the denuded layer 11 is approximately 90µm for an Ar/H atmosphere, with a hydrogen concentration lower than 30%. In both cases, the support substrate 10 has good mechanical quality, with no or very few SL and PM defects.

Figure 4 shows two examples of a support substrate, the manufacturing method of which is not in conformity with the present invention. A plateau temperature at the first heat treatment of 1200°C (or less), even under an Ar/H atmosphere and using a temperature ramp-down of between 10°C/s and 70°C/s does not make it possible to generate the required profile of vacancies: upon completion of the sequence of heat treatments, the support substrate (not according to the invention) does not have a denuded surface layer (example on the left in figure 4). In addition, by using a first heat treatment defined by a plateau at a temperature of between 1220°C and 1280°C, with a duration of between 1 second and 60 seconds, even under an Ar/H atmosphere, it is found that an excessively slow temperature ramp-down during the first heat treatment is detrimental to the preservation of a distinctive profile of vacancies: for example with a temperature ramp-down of 5°C/s, the support substrate upon completion of the sequence of heat treatments does not have an enriched deep layer (example on the right in figure 4).

After obtaining the support substrate 10, the manufacturing method according to the invention also comprises a step d) corresponding to the formation of an intermediate structure comprising the useful monocrystalline silicon layer 30 positioned on the dielectric layer 20, which itself is positioned on a front face 10a of the said support substrate 10, by a thin-layer transfer technique such as the Smart Cut™ method.

A monocrystalline silicon donor substrate is implanted via its front face, such as to define an embedded fragile plane substantially parallel to the said front face, and delimiting with this face the thin layer to be transferred thereto. The implantation is habitually carried out with light species such as ions of hydrogen, helium, or a combination of these two species. The fragile plane is so named because it comprises nano-cracks in lenticular form generated by the implanted light species.

According to a preferential option, previously referred to, a dielectric layer 20 is formed at least on the front face 10a of the support substrate 10. It is however not excluded for a part of the embedded dielectric layer of the future SOI structure to be produced on the donor substrate.

The donor substrate and the support substrate 10 are then assembled, by direct bonding between the front faces of the said substrates, to form a bonded assembly. Cleaning operations and/or surface activations, which are well known in the field of bonding by molecular adhesion, can be applied to the substrates before the assembly, in order to obtain an excellent quality of bonding. Assembly in a controlled atmosphere is also possible.

The separation at the embedded fragile plane is preferably carried out by application of heat treatment at an average temperature typically of between 350°C and 500°C, as a result of the increase of micro-cracks by coalescence and putting under pressure of the gaseous species. Alternatively or jointly, the separation can be caused by the implementation of mechanical stress to the bonded assembly.

Upon completion of this separation, an intermediate structure of the SOI type is obtained on the one hand, and the remainder of the donor substrate on the other hand. Finishing sequences, comprising cleaning operations, surface treatments (etching, polishing, etc.) and/or heat treatments, are habitually applied on the intermediate SOI structure, and are intended to remove a surface part of the transferred useful layer 30. This makes it possible to restore a good surface state (defectiveness and roughness) and good crystalline quality to the useful silicon layer 30. The useful layer 30 typically has a thickness of between 50nm and 500nm.

The manufacturing method then comprises a step e) of implementation of a third heat treatment to the intermediate structure, at a temperature of between 900°C and 1250°C, under a neutral or reductive atmosphere, in order to form the SOI structure. A heat treatment of this type does not affect the denuded surface layer 11, 13 and the deep layer 12 enriched with BMD, induced by the sequence of the first and second heat treatments. It can advantageously induce an increase in the size of the BMD micro-defects.

Following this, the SOI structure 100 is available.

The invention also concerns a monocrystalline silicon support substrate 10, which is particularly suitable for SOI structures intended in particular for photonic applications, the support substrate 10 having:

- resistivity lower than 200 ohm.cm;
- a denuded surface layer 11, 13, having a thickness greater than 40µm, with a concentration of micro-defects (BMD) lower than  $10^8/\text{cm}^3$ ;
- an enriched layer 12 below the surface layer, having a concentration of micro-defects (BMD) of between  $2.10^8/\text{cm}^3$  and  $5.10^{10}/\text{cm}^3$ .

The support substrate 10 can also comprise a silicon oxide dielectric layer on its front face 10a and/or on its rear face 10b. Preferably, the said dielectric layer has a thickness of between 500nm and 2000nm.

Finally, the invention concerns an SOI structure comprising a c-Si useful layer 30 positioned on the dielectric layer 20, which itself is positioned on the aforementioned support substrate 10. This SOI structure is particularly suitable for the production of photonic components on and/or in the useful layer 30, as well as in the support substrate 10 (in particular V-grooves and conductive vias).

It will be appreciated that the invention is not limited to the embodiments described or to the field of photonic applications, and variants of implementation or use can be made to it without departing from the context of the invention.

## CLAIMS

1. Manufacturing method of an SOI structure (100) comprising the following steps:
  - a) supply of an initial monocrystalline silicon substrate (10'), with an interstitial oxygen content of between 15 and 27 ppma, in accordance with the standard ASTM'79, and resistivity lower than 200 ohms.cm, with the initial substrate (10') being designed to form a support substrate (10) for the SOI structure (100) after having undergone the subsequent step b);
  - b) implementation of a sequence of heat treatments to the initial substrate (10') while, at least on a front face (10a), it is without a layer of silicon oxide, other than optionally a layer of native oxide, the said sequence consisting of:
    - a first heat treatment defined by a plateau at a temperature higher than 1200°C and lower than 1280°C, and with a duration of between 1 second and 60 seconds, by a temperature ramp-down of between 10°C/s and 70°C/s, and by an atmosphere of an argon or argon-hydrogen type, followed by:
    - a second heat treatment defined by a plateau at a temperature of between 900°C and 1100°C, without a stage before this temperature, under a neutral or oxidising atmosphere, in order to form a support substrate (10) comprising:
      - a denuded surface layer (11), with a thickness greater than 40µm, and having a concentration of micro-defects (BMD) lower than 10<sup>8</sup>/cm<sup>3</sup>; and
      - an enriched deep layer (12), below the denuded surface layer (11), with a concentration of micro-defects (BMD) of between 2.10<sup>8</sup>/cm<sup>3</sup> et 5.10<sup>10</sup>/cm<sup>3</sup>.
2. Manufacturing method according to claim 1, wherein the temperature of the plateau of the first heat treatment is between 1220°C and 1260°C.
3. Manufacturing method according to one of claims 1 and 2, wherein the second heat treatment is defined by temperature ramp-up and temperature ramp-down of between 0.5°C/min et 10°C/min.
4. Manufacturing method according to one of claims 1 to 3, wherein the temperature of the plateau of the second heat treatment is between 950°C and 1000°C.
5. Manufacturing method according to one of claims 1 to 4, wherein the atmosphere of the second heat treatment is oxidising, at least during the plateau, in order to form, on the support substrate

(10), all or part of a silicon oxide dielectric layer, the said dielectric layer (20) being designed to be positioned between a useful layer (30) and the support substrate (10) in the SOI structure (100).

6. Manufacturing method according to one of claims 1 to 5, comprising, after the step b) of implementation of the heat treatments sequence, a step c) of oxidation of the support substrate (10), in order to form on the support substrate (10) all or part of a silicon oxide dielectric layer, the said dielectric layer (20) being designed to be positioned between a useful layer (30) and the support substrate (10) in the SOI structure (100).
7. Manufacturing method according to one of claims 5 and 6, also comprising the following steps:
  - d) formation of an intermediate structure comprising the useful crystalline silicon layer (30) positioned on the dielectric layer (20), which itself is positioned on a front face (10a) of the support substrate (10), by means of a thin-layer transfer technique;
  - e) implementation of a third heat treatment to the intermediate structure, at a temperature of between 900°C and 1250°C, under a neutral or reductive atmosphere, in order to form the SOI structure (100).
8. Monocrystalline silicon support substrate (10) with:
  - resistivity lower than 200 ohm.cm;
  - a denuded surface layer (11, 13), with a thickness greater than 40µm, and having a concentration of micro-defects (BMD) lower than  $10^8/\text{cm}^3$ ;
  - an enriched deep layer (12), below the denuded surface layer (11,13), with a concentration of micro-defects (BMD) of between  $2.10^8/\text{cm}^3$  et  $5.10^{10}/\text{cm}^3$ .
9. Support substrate (10) according to claim 8, comprising a silicon oxide dielectric layer (20) at least on its front face (10a).
10. SOI structure (100) comprising a useful layer (30) positioned on the dielectric layer (20), which itself is positioned on a support substrate (10) according to claim 9.
11. Structure (100) according to the preceding claim, wherein the dielectric layer (20) has a thickness of between 500nm and 2000nm.