

Description

The invention relates to a receiver provided with a frequency control loop for automatic fine tuning, consecutively incorporating a controllable oscillator which is tunable in frequency by means of a variable capacitance diode, a mixer stage to which the signal from the controllable oscillator is applied for converting an RF receiver signal into an IF signal, a frequency voltage converter tuned to a fixed intermediate frequency for converting frequency deviations of the IF signal relative to the fixed intermediate frequency into amplitude variations of the frequency voltage converter output signal relative to a reference value, a control signal generating circuit for deriving a control signal for the variable capacitance diode of the controllable oscillator from the output signal of the frequency voltage converter, said controllable oscillator at least partly compensating its asymmetrical capacitance-voltage characteristic.

A frequency control loop for automatic fine tuning for use in a receiver of this type is known from the document DE-A-1 260 558.

The control signal generating circuit of the known frequency control loop comprises a transistor which amplifies on the one hand the output voltage of a frequency discriminator functioning as a frequency voltage converter in order to increase the control slope and on the other hand drives the variable capacitance diode in such a manner that its capacitance varies linearly with the said frequency deviations of the IF signal in the case of normally occurring field strengths.

This variation is achieved in the known frequency control loop by operating and choosing the working point of the transistor such that positive and negative frequency deviations for normally occurring field strengths result in an amplitude limitation of the control signal supplied by the transistor at first and second fixed values, respectively, which are located asymmetrically around the said reference value corresponding to the intermediate frequency. Under certain circumstances the asymmetry thus obtained in the control signal compensates the asymmetry of the capacitance-voltage characteristic of the variable capacitance diode of the controllable oscillator. As a result the capture and hold range of the frequency control loop, hereinafter briefly referred to as the control range, is to a certain extent located symmetrically around the correct tuning point, that is to say, the tuning position at which the carrier of the IF signal coincides with the said fixed intermediate frequency.

In the tuning ranges where amplitude limitation of the control signal occurs, the control signal does not vary with possibly occurring frequency deviations of the IF signal and the automatic fine tuning is therefore not operative. Consequently a stable tuning position on the edges of the RF filter of the receiver preceding the frequency-voltage converter, also referred to as sided tuning, becomes possible. This results in a considerably audible signal distortion.

In addition a linear amplification of the principally symmetrical discriminator voltage is effected for small field strengths in the transistor of the known frequency control loop so that also the control signal is symmetrical. The asymmetrical capacitance voltage characteristic of the variable capacitance diode is then not compensated so that also the control range of the known frequency control loop is asymmetrical (cf. the document DE-A-2 311 621).

It is an object of the invention to symmetrize the control range of a frequency control loop for automatic fine-tuning in a receiver relative to the correct tuning point independently of the field strength and without the possible occurrence of the undesired stable side-tuning effects.

According to the invention a receiver of the type described in the opening paragraph is characterized in that the control signal generating circuit comprises a threshold attenuation circuit arranged between the frequency voltage converter and the variable capacitance diode, the threshold voltage of said attenuation circuit mainly corresponding to the said reference value and its transfer factor decreasing by a substantially constant and finite dB value when the frequency voltage converter output signal exceeds the threshold voltage.

The invention is based on the recognition that for an asymmetrical amplitude adaptation of the control signal for compensating the asymmetrical capacitance-voltage characteristic of the variable capacitance diode amplitude limitation of the control signal and hence the occurrence of stable side-tuning effects is prevented by linearly amplifying or attenuating the frequency voltage converter output signal above the reference value relative to the output signal below the reference value.

When the measure according to the invention is used, the control signal has a positive or negative amplitude variation dependent on the direction of the frequency deviation relative to the reference value the variation initially increasing gradually to a given maximum positive or negative value with the value of the frequency deviation and thereafter decreasing gradually. The maximum positive and the maximum negative amplitude variations of the control signal are inversely proportional to the capacitance deviations of the variable capacitance diode relative to a reference capacitance corresponding to the reference value, caused by these amplitude deviations. In addition these maximum positive and negative amplitude deviations each mainly occur only in one given positive or negative frequency deviation relative to the correct tuning point, or in other words: the frequency-dependent amplitude variation of the control signal is curved in the vicinity of these maximum amplitude deviations so that stable side-tuning effects are prevented and the symmetrisation obtained is independent of the amplitude of the IF signal or the field strength.

A preferred embodiment of a receiver according to the invention, which can easily be realised, is characterized in that the threshold attenuation

circuit comprises a voltage comparator for comparing the frequency voltage converter output voltage with the threshold voltage, and a voltage divider coupled to the voltage comparator and arranged between the frequency voltage converter and the variable capacitance diode, said voltage comparator increasing the dividing factor of the voltage divider when the last-mentioned output voltage exceeds the threshold voltage.

In a further preferred embodiment, which is characterized in that the voltage divider comprises a series arrangement of first and second resistors, which first resistor is also coupled between the frequency voltage converter and the variable capacitance diode and which second resistor is coupled to the emitter of a first transistor incorporated in the voltage comparator, said first transistor being connected to ground *via* its collector and to a first bias voltage *via* the base, said first bias voltage being substantially equal to the difference between the threshold voltage and the voltage across the base-emitter junction of the first conducting transistor, the first transistor realises a comparison function and also controls the dividing factor of the potential divider.

Still another preferred embodiment of a receiver of this type is characterized in that the first resistor constitutes a further voltage divider with a third resistor and its coupled *via* this third resistor to the emitter of a second transistor, which second transistor is of a conductivity type opposite to that of the first transistor and is connected *via* its collector to a supply voltage and *via* its base to a second bias voltage, said second bias voltage being substantially equal to the sum of the threshold voltage and the voltage across the base-emitter junction of the second conducting transistor, the ratio between the dividing factor of the first-mentioned voltage divider and that of the further voltage divider being opposed to the asymmetry of the capacitance-voltage characteristic of the variable capacitance diode relative to a reference capacitance corresponding to the reference value.

When this measure is used a bilateral asymmetrical amplitude adaptation of the control signal is obtained.

The invention will be further described by way of example with reference to the accompanying Figures shown in the drawing.

In this drawing:

Figure 1 shows a receiver according to the invention.

Figure 2 shows the capacitance-voltage characteristic of the variable capacitance diode incorporated in the controllable oscillator, as well as some characteristics of the control signal to illustrate the operation of the invention.

Figure 3 shows a threshold attenuation circuit for bilateral amplitude adaptation of the control signal.

Figure 4 shows a further, more general embodiment of a threshold attenuation circuit for use in a receiver according to the invention.

Figure 1 shows a receiver 1—9 according to the

invention comprising an RF input stage 1 provided with an aerial input A, which stage is coupled to a frequency control loop 2—6 and through this loop to a signal processing unit 7 (for example, a stereo decoder and/or audio output stages) and loudspeakers 8 and 9. The frequency control loop 2—6 incorporates: a mixer stage 2 coupled to the RF input stage 1, an intermediate frequency (IF) part 3, a frequency-voltage converter 4 which may be, for example, an FM quadrature detector, FM—PLL-detector, ratio detector, etc., a control signal generating circuit 5 which is coupled to a variable capacitance diode D which diode D is a tuning element of a controllable oscillator 6, which oscillator 6 applies a frequency-tunable oscillator signal to the mixer stage 2.

Signal processing in such a receiver is known per se: a radio frequency (RF) receiver signal is applied *via* the RF input stage 1 to the mixer stage 2 wherein this RF signal is converted with the aid of the oscillator signal into an intermediate frequency (IF) signal. Selection of the IF signal is effected in the IF part 3. In the case of an FM receiver frequency detection is subsequently effected in the frequency voltage converter 4, succeeded by signal processing (for example, stereo decoding) in a signal processing unit 7 coupled thereto and reproduction by means of the loudspeakers 8 and 9. In the case of an AM receiver an AM detection is effected in an AM detector (not shown) at the output of the IF part 3, succeeded by further audio signal processing in an audio output stage (likewise not shown).

The IF part 3 and the frequency voltage converter 4 are mutually tuned to the same fixed intermediate frequency. In both FM and AM receivers the frequency voltage converter 4 converts frequency deviations of the carrier of the IF signal relative to the fixed intermediate frequency into signal amplitude variations relative to a reference value corresponding to the fixed intermediate frequency which variations are determined in magnitude and direction by these frequency deviations. Automatic fine tuning is achieved by deriving in the manner to be described hereinafter a control signal for the variable capacitance diode D from the output signal of the frequency voltage converter 4 — hereinafter briefly referred to as detector voltage — in the control signal generating circuit 5, which control signal controls the frequency of the controllable oscillator 6 in such a manner that a negative feedback and hence a reduction of said frequency deviations in the frequency control loop 2—6 is produced.

Since the detector output voltage for positive and negative frequency deviations of equal magnitude varies symmetrically relative to the reference value, while the voltage-capacitance characteristic of the variable capacitance diode D relative to this reference value is considerably asymmetrical, the control range, in the case of a control signal varying symmetrically with the frequency around this reference value, will also

be asymmetrical. To illustrate this, reference is made to Figure 2 in which curve K_1 shows the last-mentioned diode characteristic (diode capacitance C_d as a function of the diode cut-off voltage V_D) and curve K_2 shows the frequency-dependent amplitude variation of said symmetrical detector voltage or at least the DC component thereof varying in amplitude with the frequency deviations.

Starting from a reference capacitance C_r at a diode cut-off voltage $V_D = V_s - V_r$, wherein V_s is the supply voltage applied to the cathode of the diode D and V_r is the reference value, occurring in the case of correct tuning, when the carrier of the IF signal coincides with the fixed intermediate frequency, a control signal V_c corresponding to the d.c. component of the detector voltage and varying symmetrically over K_2 around V_r between $V_r + \Delta V$ and $V_r - \Delta V$ will result in a capacitance variation in a range which is located asymmetrically around C_r between maximum and minimum capacitance values C_1 and C_2 the range between C_1 and C_r being considerably larger than that between C_r and C_2 . By reducing the maximum, in this case positive amplitude (Q) of the control signal V_c , occurring at the frequency f_2 , relative to the maximum negative amplitude (S) occurring at the frequency f_1 , for example, up to $V_r + \frac{1}{2} \Delta V$, the maximum capacitance value C_1 can be reduced to C_3 , the capacitance difference between C_3 and C_r then being substantially equal to that between C_r and C_2 . The loop gain of the frequency control loop 2-6 is then equal for positive frequency deviations to that for negative frequency deviations resulting in a symmetrical control range.

When such an amplitude reduction is obtained by an amplitude limitation of the control signal V_c , as in the prior art and as is shown by the flat portion between the points R and P in Figure 2, an undesired side-tuning may be produced in the range between said frequency f_2 and a frequency f_4 corresponding to the point P.

In the receiver according to the invention such an amplitude limitation of the control signal V_c is prevented in the amplitude reduction by attenuating the control signal by a constant and finite dB value (in the given case 3 dB) for values which are exceeding V_r relative to values lower than V_r . Consequently the curvature around point T, which corresponds in frequency to point Q, is maintained. In the ranges outside f_1 and f_2 there is therefore a positive feedback of frequency deviations in the frequency control loop resulting in an instability which prevents the occurrence of stable side-tuning effects.

Such an amplitude reduction which is direction-dependent relative to the reference value V_r is obtained with the control signal generating circuit 5 of the receiver of Figure 1. It comprises a voltage divider R_1, R_2 , which is coupled at one end via an input terminal 10 to the output of the frequency voltage converter 4 and at the other end to the emitter of a first PNP transistor T_1 . The base of this transistor T_1 is connected to a first bias voltage and its collector is connected to ground.

The first bias voltage is obtained at an output of a voltage divider R_4, R_5 arranged between the supply voltage V_s and ground. The junction between resistors R_1 and R_2 of the voltage divider R_1, R_2 is connected to ground for signal frequencies via an earthed capacitor C and coupled via a resistor R_6 and an output 11 of the control signal generating circuit 5 to the variable capacitance diode D.

The first bias voltage is adjusted to a value via the voltage divider R_4, R_5 , which value is lower than the reference value V_r of the detector voltage by mainly one diode voltage (approximately 600 mV) i.e. the voltage across the base-emitter diode of the transistor T_1 in the conducting state. The threshold voltage of the voltage divider R_1, R_2 and transistor T_1 , functioning as a threshold attenuation circuit is therefore equal to the reference value V_r ; for detector voltages above the reference voltage V_r (broken line portion O, P, Q, R of curved K_2) transistor T_1 is conducting, the resistor R_2 being connected to ground through the emitter-collector path of T_1 and the detector voltage being attenuated by the dividing factor of the voltage divider R_1, R_2 . The frequency-dependent control voltage V_c then follows the solid line portion of the curve K_2' via point T.

When the detector voltage decreases to below the reference value V_r , the conduction of transistor T_1 decreases. Although the voltage divider R_1, R_2 is still operative to some extent in this range, the attenuation effect is negligibly small in practice and the frequency-dependent control voltage V_c mainly follows the solid line portion of curve K_2 via the point S.

An amplitude adaptation of the detector voltage to the asymmetrical diode characteristic for values above and below the reference value V_r is possible with the control signal generating circuits of Figures 3 and 4 in which elements corresponding to those of Figure 1 have the same reference numerals. This so-called bilateral amplitude adaptation is achieved in the circuit of Figure 3 by incorporating, in addition, to the threshold first PNP transistor T_1 , a threshold second NPN transistor T_2 whose emitter is connected via a third resistor R_3 to the junction between the first and second resistors R_1 and R_2 , which first and third resistors R_1 and R_3 constitute a so-called further voltage divider, the collector of T_2 being connected to a supply voltage and the base being connected to a second bias voltage. The first and second bias voltages are obtained by a suitable voltage division of the supply voltage V_s via the partial resistors R_4' and R_4'' of the original resistor R_4 and the resistor R_5 . By choosing the ratio between the dividing factor determined by R_1 and R_2 and the dividing factor determined by R_1 and R_3 to be mainly inversely proportional to the capacitance asymmetry of the diode characteristic around the reference capacitance C_r , a symmetrical control range is obtained in the case of suitably chosen bias voltages. The amplitude of the detector voltage variation does not need to have a given value in order to give the

control signal the frequency-dependent variation through the points S and T indicated by curve K_2' , but it may also be larger than that of the circuit of Figure 1.

Figure 4 shows a general embodiment of a control signal generating circuit 5 for use in a receiver according to the invention in which a voltage comparison is effected in first and second comparators COMP1 and COMP2 which upon exceeding first and second threshold voltages V_1 and V_2 close switches S_1 and S_2 and therefore produce a bilateral amplitude adaptation of the detector voltage, likewise as the circuit of Figure 3.

In a practical embodiment the resistors R_1 — R_6 had the following values: 30 K Ω ; 39 K Ω ; 60 K Ω ; 15 K Ω ; 4.3 K Ω ; 10 K Ω , respectively, and the resistors R_4' and R_4'' had values of 4.3 K Ω and 10.7 K Ω , respectively, the supply voltage V_s was 1600 mV; the reference value V_r was 800 mV and the capacitor C had a value of 4.7 μ F.

It is evident that the inventive idea may also be realised in different manners, for example, by using a threshold amplifier which amplifies the detector voltage at values below the reference value V_r relative to those above V_r , by applying the control voltage V_c to the cathode of the diode so that the above-described amplitude adaptation is to be exactly reversed to obtain a suitable compensation of the asymmetrical diode characteristic and/or by realising a reversal in the frequency or voltage-dependent transfer function elsewhere in the circuit of the control loop 2—6.

Claims

1. A receiver provided with a frequency control loop for automatic fine tuning, consecutively incorporating a controllable oscillator (6) which is tunable in frequency by means of a variable capacitance diode, a mixer stage (2) to which the signal from the controllable oscillator is applied for converting an RF receiver signal into an intermediate frequency signal, a frequency voltage converter (4) tuned to a fixed intermediate frequency for converting frequency deviations of the intermediate frequency signal relative to the fixed intermediate frequency into amplitude variations of the frequency voltage converter output signal relative to a reference value (V_r), a control signal generating circuit (5) for deriving control signal for the variable capacitance diode of the controllable oscillator from the output signal of the frequency voltage converter, said controllable oscillator at least partly compensating its asymmetrical capacitance-voltage characteristic, characterized in that the control signal generating circuit (5) comprises a threshold attenuation circuit arranged between the frequency voltage converter (4) and the variable capacitance diode, the threshold voltage of said attenuation circuit mainly corresponding to the said reference value and its transfer factor decreasing by a substantially constant and finite dB value when the frequency voltage converter output signal exceeds the threshold voltage.

2. A receiver as claimed in Claim 1, characterized

in that the threshold attenuation circuit comprises a voltage comparator for comparing the output voltage of the frequency voltage converter with the threshold voltage, and a voltage divider (R1, R2) coupled to the voltage comparator and arranged between the frequency voltage converter and the variable capacitance diode, said voltage comparator increasing the dividing factor of the voltage divider when the last-mentioned output voltage exceeds the threshold voltage.

3. A receiver as claimed in Claim 2, characterized in that the voltage divider comprises a series arrangement of first and second resistors, which first resistor (R1) is also coupled between the frequency voltage converter and the variable capacitance diode and which second resistor (R2) is coupled to the emitter of a first transistor (T1) incorporated in the voltage comparator, said first transistor being connected to ground via its collector and to a first bias voltage via its base, said first bias voltage being mainly equal to the difference between the threshold voltage and the voltage across the base-emitter junction of the first conducting transistor.

4. A receiver as claimed in Claim 3, characterized in that the first resistor (R1) constitutes a further voltage divider with a third resistor (R3) and is coupled via said third resistor to the emitter of a second transistor (T2), which second transistor is of a conductivity type opposite to that of the first transistor (T1) and is connected via its collector to a supply voltage and via its base to a second bias voltage, said second bias voltage being substantially equal to the sum of the threshold voltage and the voltage across the base-emitter junction of the second conducting transistor, the ratio between the dividing factor of the first-mentioned voltage divider (R1, R2) and that of the further voltage divider (R1, R3) being opposed to the asymmetry of the capacitance-voltage characteristic of the variable capacitance.

Patentansprüche

1. Empfänger mit einer Frequenzregelschleife zur automatischen Feinabstimmung, in der hintereinander die folgenden Elemente vorgesehen sind; ein mittels einer veränderlichen Kapazitätsdiode in der frequenz abstimmbarer, regelbarer Oszillator (6), eine Mischstufe (7), der das Signal von dem regelbaren Oszillator zur Umwandlung eines HF-Empfangssignals in ein ZF-Signal zugeführt wird, und ein auf eine feste Zwischenfrequenz abgestimmter Frequenz-Spannungswandler (4) zum Umwandeln von Frequenzabweichungen des ZF-Signals gegenüber der festen Zwischenfrequenz in Amplitudenschwankungen des Ausgangssignals des Frequenz-Spannungswandlers gegenüber einem Bezugswert (V_r), eine Regelsignalerzeugungsschaltung (5); zum aus dem Ausgangssignal des Frequenz-Spannungswandlers Ableiten eines Regelsignals für die veränderliche Kapazitätsdiode des regelbaren Oszillators, der seine asymmetrische Kapazität-Spannungskennlinie wenigstens teilweise ausgleicht,

control signal the frequency-dependent variation through the points S and T indicated by curve K_2' , but it may also be larger than that of the circuit of Figure 1.

Figure 4 shows a general embodiment of a control signal generating circuit 5 for use in a receiver according to the invention in which a voltage comparison is effected in first and second comparators COMP1 and COMP2 which upon exceeding first and second threshold voltages V_1 and V_2 close switches S_1 and S_2 and therefore produce a bilateral amplitude adaptation of the detector voltage, likewise as the circuit of Figure 3.

In a practical embodiment the resistors R_1 — R_6 had the following values: 30 K Ω ; 39 K Ω ; 60 K Ω ; 15 K Ω ; 4.3 K Ω ; 10 K Ω , respectively, and the resistors R_4' and R_4'' had values of 4.3 K Ω and 10.7 K Ω , respectively, the supply voltage V_s was 1600 mV; the reference value V_r was 800 mV and the capacitor C had a value of 4.7 μ F.

It is evident that the inventive idea may also be realised in different manners, for example, by using a threshold amplifier which amplifies the detector voltage at values below the reference value V_r relative to those above V_r , by applying the control voltage V_c to the cathode of the diode so that the above-described amplitude adaptation is to be exactly reversed to obtain a suitable compensation of the asymmetrical diode characteristic and/or by realising a reversal in the frequency or voltage-dependent transfer function elsewhere in the circuit of the control loop 2—6.

Claims

1. A receiver provided with a frequency control loop for automatic fine tuning, consecutively incorporating a controllable oscillator (6) which is tunable in frequency by means of a variable capacitance diode, a mixer stage (2) to which the signal from the controllable oscillator is applied for converting an RF receiver signal into an intermediate frequency signal, a frequency voltage converter (4) tuned to a fixed intermediate frequency for converting frequency deviations of the intermediate frequency signal relative to the fixed intermediate frequency into amplitude variations of the frequency voltage converter output signal relative to a reference value (V_r), a control signal generating circuit (5) for deriving control signal for the variable capacitance diode of the controllable oscillator from the output signal of the frequency voltage converter, said controllable oscillator at least partly compensating its asymmetrical capacitance-voltage characteristic, characterized in that the control signal generating circuit (5) comprises a threshold attenuation circuit arranged between the frequency voltage converter (4) and the variable capacitance diode, the threshold voltage of said attenuation circuit mainly corresponding to the said reference value and its transfer factor decreasing by a substantially constant and finite dB value when the frequency voltage converter output signal exceeds the threshold voltage.

2. A receiver as claimed in Claim 1, characterized

in that the threshold attenuation circuit comprises a voltage comparator for comparing the output voltage of the frequency voltage converter with the threshold voltage, and a voltage divider (R1, R2) coupled to the voltage comparator and arranged between the frequency voltage converter and the variable capacitance diode, said voltage comparator increasing the dividing factor of the voltage divider when the last-mentioned output voltage exceeds the threshold voltage.

3. A receiver as claimed in Claim 2, characterized in that the voltage divider comprises a series arrangement of first and second resistors, which first resistor (R1) is also coupled between the frequency voltage converter and the variable capacitance diode and which second resistor (R2) is coupled to the emitter of a first transistor (T1) incorporated in the voltage comparator, said first transistor being connected to ground via its collector and to a first bias voltage via its base, said first bias voltage being mainly equal to the difference between the threshold voltage and the voltage across the base-emitter junction of the first conducting transistor.

4. A receiver as claimed in Claim 3, characterized in that the first resistor (R1) constitutes a further voltage divider with a third resistor (R3) and is coupled via said third resistor to the emitter of a second transistor (T2), which second transistor is of a conductivity type opposite to that of the first transistor (T1) and is connected via its collector to a supply voltage and via its base to a second bias voltage, said second bias voltage being substantially equal to the sum of the threshold voltage and the voltage across the base-emitter junction of the second conducting transistor, the ratio between the dividing factor of the first-mentioned voltage divider (R1, R2) and that of the further voltage divider (R1, R3) being opposed to the asymmetry of the capacitance-voltage characteristic of the variable capacitance.

Patentansprüche

1. Empfänger mit einer Frequenzregelschleife zur automatischen Feinabstimmung, in der hintereinander die folgenden Elemente vorgesehen sind; ein mittels einer veränderlichen Kapazitätsdiode in der frequenz abstimmbarer, regelbarer Oszillator (6), eine Mischstufe (7), der das Signal von dem regelbaren Oszillator zur Umwandlung eines HF-Empfangssignals in ein ZF-Signal zugeführt wird, und ein auf eine feste Zwischenfrequenz abgestimmter Frequenz-Spannungswandler (4) zum Umwandeln von Frequenzabweichungen des ZF-Signals gegenüber der festen Zwischenfrequenz in Amplitudenschwankungen des Ausgangssignals des Frequenz-Spannungswandlers gegenüber einem Bezugswert (V_r), eine Regelsignalerzeugungsschaltung (5); zum aus dem Ausgangssignal des Frequenz-Spannungswandlers Ableiten eines Regelsignals für die veränderliche Kapazitätsdiode des regelbaren Oszillators, der seine asymmetrische Kapazität-Spannungskennlinie wenigstens teilweise ausgleicht,



dadurch gekennzeichnet, daß die Regelsignalerzeugungsschaltung (5) eine zwischen dem Frequenz-Spannungswandler (4) und der veränderlichen Kapazitätsdiode vorgesehene Schwellendämpfungsschaltung aufweist, deren Schwellenspannung dem genannten Bezugswert im wesentlichen entspricht und deren Übertragungsfaktor mit einem im wesentlichen konstanten und endgültigen dB-Wert abnimmt, wenn das Ausgangssignal des Frequenz-Spannungswandlers die Schwellenspannung überschreitet.

2. Empfänger nach Anspruch 1, dadurch gekennzeichnet, daß die Schwellendämpfungsschaltung eine Spannungsvergleichsschaltung aufweist zum Vergleichen der Ausgangsspannung des Frequenz-Spannungswandlers mit der Schwellenspannung, sowie einem mit der Spannungsvergleichsschaltung gekoppelten, zwischen dem Frequenz-Spannungswandler und der veränderlichen Kapazitätsdiode geschalteten Spannungsteiler (R_1 , R_2), wobei die Spannungsvergleichsschaltung bei Überschreitung der Schwellenspannung durch die letztgenannte Ausgangsspannung den Teilungsfaktor des Spannungsteilers vergrößert.

3. Empfänger nach Anspruch 2, dadurch gekennzeichnet, daß der Spannungsteiler eine Reihenschaltung aus ersten und zweiten Widerständen aufweist, wobei der erste Widerstand (R_1) ebenfalls zwischen dem Spannungswandler und der veränderlichen Kapazitätsdiode liegt und der zweite Widerstand (R_2) mit dem Emitter eines in die Spannungsvergleichsschaltung aufgenommenen ersten Transistors T_1 gekoppelt ist, der über den Kollektor an Masse und über die Basis an einer ersten Vorspannung liegt, die der Differenz zwischen der Schwellenspannung und der Spannung an dem Basis-Emitter-Übergang des ersten leitenden Transistors nahezu entspricht.

4. Empfänger nach Anspruch 3, dadurch gekennzeichnet, daß der erste Widerstand (R_1) mit einem dritten Widerstand (R_3) einen weiteren Spannungsteiler bildet und über diesen dritten Widerstand mit dem Emitter eines zweiten Transistors gekoppelt ist, dessen Leitungstyp dem des ersten Transistors (T_1) entgegengesetzt ist, über den Kollektor mit einer Speisespannung, und über die Basis mit einer zweiten Vorspannung verbunden ist, die der Summe der Schwellenspannung und der Spannung an dem Basis-Emitter-Übergang des zweiten leitenden Transistors nahezu entspricht, wobei das Verhältnis zwischen dem Teilungsfaktor des erstgenannten Spannungsteilers (R_1 , R_2) und dem des weiteren Spannungsteilers (R_1 , R_3) der Asymmetrie der Kapazität-Spannungskennlinie der veränderlichen Kapazitätsdiode entgegengesetzt ist.

Revendications

1. Récepteur pourvu d'une boucle de commande de fréquence pour un accord fin automatique, comprenant consécutivement un oscillateur pouvant être commandé (6) qui peut être accordé en

fréquence à l'aide d'une diode à capacité variable, un étage mélangeur (2) auquel le signal de l'oscillateur pouvant être commandé est appliqué pour convertir un signal de récepteur RF en un signal de fréquence intermédiaire, un convertisseur de fréquences-tension (4) accordé sur une fréquence intermédiaire fixe pour convertir des déviations de fréquence du signal de fréquence intermédiaire par rapport à la fréquence intermédiaire fixe en variations d'amplitude du signal de sortie du convertisseur de fréquence-tension par rapport à une valeur de référence (V_r), un circuit générateur de signal de commande (5) pour dériver un signal de commande pour la diode à capacité variable de l'oscillateur pouvant être commandé à partir du signal de sortie du convertisseur de fréquence-tension, l'oscillateur pouvant être commandé compensant au moins partiellement sa caractéristique de capacité-tension asymétrique, caractérisé en ce que le circuit générateur de signal de commande (5) comprend un circuit d'atténuation à seuil disposé entre le convertisseur de fréquence-tension (4) et la diode à capacité variable, la tension de seuil du circuit d'atténuation correspondant principalement à ladite valeur de référence, et son facteur de transfert diminuant d'une valeur en dB en substance constante et finie lorsque le signal de sortie du convertisseur de fréquence-tension excède la tension de seuil.

2. Récepteur suivant la revendication 1, caractérisé en ce que le circuit d'atténuation à seuil comprend un comparateur de tension pour comparer la tension de sortie du convertisseur de fréquence-tension à la tension de seuil, et un diviseur de tension (R_1 , R_2) couplé au comparateur de tension et disposé entre le convertisseur de fréquence-tension et la diode à capacité variable le comparateur de tension augmentant le facteur de division du diviseur de tension lorsque la tension de sortie mentionnée en dernier lieu excède la tension de seuil.

3. Récepteur suivant la revendication 2, caractérisé en ce que le diviseur de tension comprend un montage en série d'une première et d'une seconde résistance, la première résistance (R_1) étant également couplée entre le convertisseur de fréquence-tension et la diode à capacité variable et la seconde résistance (R_2) étant couplée à l'émetteur d'un premier transistor (T_1) incorporé dans le comparateur de tension, le premier transistor étant connecté à la masse par l'intermédiaire de son collecteur et à une première tension de polarisation par l'intermédiaire de sa base, la première tension de polarisation étant en substance égale à la différence entre la tension de seuil et la tension présente dans la jonction base-émetteur du premier transistor conducteur.

4. Récepteur suivant la revendication 3, caractérisé en ce que la première résistance (R_1) constitue un autre diviseur de tension avec une troisième résistance (R_3) et est couplée, par l'intermédiaire de cette troisième résistance, à l'émetteur d'un second transistor, (T_2) ce second transistor étant d'un type de conductivité opposé à celui du



premier transistor (T_1) et étant connecté, par l'intermédiaire de son collecteur, à une tension d'alimentation et, par l'intermédiaire de sa base, à une seconde tension de polarisation, la seconde tension de polarisation étant en substance égale à la somme de la tension de seuil et de la tension

présente dans la jonction base-émetteur du second transistor conducteur, le rapport entre le facteur de division du premier diviseur de tension (R_1 , R_2) et celui de l'autre diviseur de tension (R_1 , R_3) étant opposé à l'asymétrie de la caractéristique de capacité-tension de la capacité variable.

10

15

20

25

30

35

40

45

50

55

60

65

7



* C L M S *