CLAIMS

1. A metal oxide semiconductor (MOS) integrated circuit (IC), comprising:

a plurality of fiducial standard cells, wherein the plurality of fiducial standard cells include a plurality of cell sizes, the plurality of cell sizes are non-equally utilized among the plurality of fiducial standard cells, and the plurality of fiducial standard cells are placed to have a random offset from a uniform global placement pattern, wherein each cell size of the plurality of cell sizes of the plurality of fiducial standard cells has one or more openings in a diffusion layer of an active region to allow for reflections of a laser beam from a metal layer.

2. The MOS IC of claim 1, wherein each cell size of the plurality of cell sizes of the plurality of fiducial standard cells differ in at least one of an x-direction and a y-direction.

3. The MOS IC of claim 1, wherein the metal layer is not connected to the active region for each cell size of the plurality of cell sizes of the plurality of fiducial standard cells.

4. The MOS IC of claim 1, wherein each cell size the plurality of cell sizes differs in the openings in the diffusion layer of the active region.

5. The MOS IC of claim 1, wherein the plurality of fiducial standard cells are further placed to allow a reduced number of fiducial standard cells to be viewable within a viewing window aperture positioned at a plurality of positions on the MOS IC.

6. The MOS IC of claim 1, wherein each cell size of the plurality of cell sizes is non-equally utilized among the plurality of fiducial standard cells so that the fiducial standard cell having a largest cell size has a highest utilization.

7. The MOS IC of claim 1, wherein the plurality of fiducial standard cells are placed to have a random offset from a uniform global placement pattern by a placement of each of the plurality of fiducial standard cells to have a random dithering in distance from the uniform global placement pattern along at least one of an x-direction and a y-direction.

8. The MOS IC of claim 1, wherein the uniform global placement pattern comprises one of a non-rotated square pattern, a rotated square pattern, a non-rotated hexagonal pattern, and a rotated hexagonal pattern.

9. The MOS IC of claim 1, wherein the uniform global placement pattern is scaled to allow a reduced number of fiducial standard cells to be viewable within a viewing window aperture.

10. The MOS IC of claim 1, wherein the plurality of cell sizes of the plurality of fiducial standard cells comprises:

at least four power rails extending in a first direction across the fiducial standard cells, wherein each of the at least four power rails is coupled to a first voltage source or a second voltage source different than the first voltage source;

and wherein the active region includes one or more sets of active regions adjacent each of the at least four power rails, wherein each set of the one or more sets of active regions is collinear in the first direction, wherein at least one set of active regions includes at least two disjoint active regions, and wherein each set of the one or more sets of the active regions is disconnected from contacts and interconnects to the metal layer.

11. The MOS IC of claim 10, wherein the at least two disjoint active regions of the at least one set of the active regions are separated by less than 300 nm.

12. The MOS IC of claim 10, wherein each set of the one or more sets of active regions are aligned in a second direction orthogonal to the first direction.

13. The MOS IC of claim 10, wherein the at least two disjoint active regions of the at least one of the active regions comprises an active region on a first side of the fiducial standard cells and an active region on a second side of the fiducial standard cells.

14. The MOS IC of claim 10, wherein at least one of the active regions comprises one active region extending in the first direction across the fiducial standard cells.

15. The MOS IC of claim 10, wherein each cell size of the plurality of cell sizes of the plurality of fiducial standard cells further comprises a plurality of floating gate interconnects extending in a second direction across the fiducial standard cells, the second direction being orthogonal to the first direction.

16. The MOS IC of claim 10, wherein at least one of the active regions include at least three disjoint active regions.

17. The MOS IC of claim 16, wherein adjacent pairs of active regions of the at least three disjoint active regions are separated by less than 300 nm.

18. The MOS IC of claim 16, wherein the at least three disjoint active regions of the at least one of the active regions comprise an active region on a first side of the fiducial standard cells, an active region in a central portion of the fiducial standard cells, and an active region on a second side of the fiducial standard cells.

19. A method of placing a plurality of fiducial standard cells in a metal oxide semiconductor (MOS) integrated circuit (IC), comprising:

determining a region of the MOS IC for placing the plurality of fiducial standard cells, wherein the region has an x-direction and a y-direction;

subtracting a dither range in the x-direction from one half of a maximum distance in the x-direction between a non-fiducial standard cell and one of the plurality of fiducial standard cells to generate an x-direction half-stepping distance;

subtracting a dither range in the y-direction from one half of a maximum distance in the y-direction between a non-fiducial standard cell and one of the plurality of fiducial standard cells to generate a y-direction half-stepping distance;

determining a random dither in the x-direction, wherein the random dither in the x-direction ranges from a minus half to a positive half times the dither range in the x-direction;

determining a random dither in the y-direction, wherein the random dither in the y-direction ranges from a minus half to a positive half times the dither range in the y-direction;

stepping through the x-direction of the region by successively adding twice the x-direction half-stepping distance by the random dither in the x-direction to determine a plurality of placement positions in the x-direction;

stepping through the y-direction of the region by successively adding twice the y-direction half-stepping distance by the random dither in the y-direction to determine a plurality of placement positions in the y-direction; and

placing the plurality of fiducial standard cells at locations based on the plurality of placement positions in the x-direction and the plurality of placement positions in the y-direction.

20. The MOS IC of claim 1, wherein a total area of the plurality of fiducial standard cells is less than 0.1% of an area of the MOS IC.