

PROCESS AND CIRCUIT ARRANGEMENT FOR RECOGNIZING TOPOLOGICALLY CONTIGUOUS IMAGE STRUCTURES IN LINE FORM

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Description

5 The invention concerns recognition in video real-time of topologically contiguous image structures in the form of lines in which groups of image dots or image points having identical characteristics within a line are given identification numbers which differ from one another, the identification number of the image point group of the line first adjoined by an image point group of a following line in the line direction by at least one image point in the column direction being adopted in adjoining groups of the following line.

10 The invention is used for automated inspection of structured surfaces, in particular in masks, LCD's, printed circuit boards and semiconductor wafers, during their manufacture.

15 One objective in image evaluation is to select image point groups according to given criteria (characteristics) from an arrangement of image points mainly in the form of a matrix or array and to process them for further evaluation in compressed form for subsequent evaluation units.

For the purpose of data compression, it is known to assemble image points within a line and then to eliminate the line boundaries.

20 In EP 279 157 A2, characteristic features are extracted from run-length-coded image data. This results in a list of run-length-coded image data which are classified according to circular, trapezoidal, convergent and divergent regions. In so doing, horizontal and vertical intermediate spaces are filtered and disappear from the data record.

25 This process is not suitable for verifying defects on semiconductor wafers, since filtering of the intermediate spaces falsifies the defect image resulting in erroneous classification of the semiconductor in defect classes.

A more suitable solution consists in marking all run-length-coded image data describing a contiguous region with identical characteristics, e.g., identical gray values, as such in a uniform manner.

30 Identification numbers or counting numbers are introduced for contiguous image point groups within a line so that all image point groups starting in the first line receive a consecutive identification number. In the following line, a new counting number is given

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only when the image point group does not adjoin an image point group of identical characteristics on the preceding line. If the adjoining image point group on the following line has the same characteristics as the image point group in the preceding line, the same identification number is used.

5 Ambiguities, also known as equivalences, result when contiguous image point groups in the current line have connections with a plurality of contiguous image point groups having identical characteristics but different identification numbers. Accordingly, these equivalences result as pairs of distinct identification numbers and describe connections of image point groups which begin separately and flow together.

10 These ambiguities are resolved by using a computer-assisted search algorithm whose run time is dependent on the shape of image structures divided into image point groups. Occurring spiral-shaped or heavily interlaced image structures cause search algorithm run times which can no longer be processed in video real-time.

15 The object of the present invention is to shorten the processing times for resolving equivalences irrespective of the shape and characteristics of the image structures so as to ensure processing in video real-time.

20 According to the invention, this object is met by a process for recognizing topologically contiguous image structures arranged in line form in which image point groups formed by at least one image point and having identical characteristics within a line receive consecutive identification numbers and image point groups of a following line adopt already allocated identification numbers from the image point groups first adjoining them by at least one image point in the line direction in that, in a first process step, one identification number of a pair of identification numbers of adjoining image point groups with different identification numbers serves as an address value for a first addressed storage with a marked initial state for
25 each storage location and the other identification number becomes the data value of the storage location addressed by the first identification number when the storage location has the marked initial state; otherwise, in a second process step, the other identification number and the data value of the addressed storage location are used as address values for determining storage locations with a marked initial state for whose address values the first process step is
30 applied, wherein a respective data value determined for an address value once again serves as an address until a storage location with the marked initial state is found, and pairs of

identification numbers leading to identical address values in the second process step are ignored; and, in a third process step for forming an allocation table in the form of a second addressable storage, storage locations corresponding to the address values from the first process step receive the address value itself as a data value when the address value has the marked initial state; otherwise, when the address value does not have the marked initial state, a contained data value is used as address value until a storage location with the marked initial state is found whose address value becomes the data value for the address value without the marked initial state.

The invention is further directed to a circuit arrangement for recognizing topologically contiguous image structures arranged in line form by means of processing a pair of different identification numbers of image point groups which have at least one image point and adjoin one another within the image structures in adjoining lines, wherein the identification numbers for the image point groups in a line are allocated consecutively and image point groups of a following line adopt already allocated identification numbers of image point groups first adjoining them by at least one image point in the line direction, in which a first multiplexer and second multiplexer, one of whose inputs is connected in each instance with the count value output of a counter, an input of the second multiplexer being connected to fixed voltage, and a comparator have inputs for the identification numbers and, in addition, are connected to outputs of a first register and second register whose data inputs are connected to an output of a third register which is moreover coupled with an address input of a first storage and with a first address input of a second storage, the input of the third register being connected with the output of the first multiplexer.

A data input and data output of the first storage is coupled with an additional input of the first multiplexer, the data output of the second multiplexer, the input of a null indicator and a first data input of the second storage which also has a second address input and a second output, and connections on the output side of an operation control unit with inputs KN and RESET and outputs ENK and READY lead to control inputs of the first multiplexer and second multiplexer, to release inputs of the second multiplexer and first storage and to write inputs of the first storage and second storage. Further, there are connections proceeding from the operation control unit between clock outputs and the first register, second register and third register, the counter, to a load input of the counter and to enable or release inputs of

the first register and second register. Further, the operation control unit is connected on the input side with an end-message line of the counter, with two lines of the comparator and with a line of the null indicator.

Since the allocation table containing the identification number allocation for every addressed equivalence is created directly from a generated intermediate code, the equivalences can be evaluated already at the moment they are detected. This results in a shorter processing time in comparison to a computer-assisted search algorithm which can be started only when all equivalences are present. The number of steps for resolving an equivalence according to the invention is equal to the interlace factor of the equivalence, the number of steps with a computer-assisted search algorithm for the same task is equal to the maximum interlace factor for all equivalences.

An embodiment example of the invention is explained more fully in the following with reference to the schematic drawing.

Fig. 1 shows a circuit arrangement according to the invention;

Fig. 2 shows the allocation of identification numbers to groups of image points.

In the circuit arrangement shown in Fig. 1, a first multiplexer M1 and a second multiplexer M2, one of whose inputs is connected in each instance with the count value output of a counter Z, and a comparator C have inputs for identification numbers KN1 and KN2 and are connected, in addition, to an output of a first register R1 and to an output of a second register R2.

Connections lead from the output of a third register R3 to the data inputs of the first register R1 and second register R2, this third register R3 being coupled with the respective address input of a first storage RAM1 and second storage RAM2. The input of the third register R3 is connected with the output of the first multiplexer M1.

A data input and output D of the first storage RAM1 is coupled with another input of the first multiplexer M1, the data output of the second multiplexer M2, the input of a null indicator N and a data input D of the second storage RAM2. Another input of the second multiplexer is connected to fixed voltage.

The second storage RAM2 is constructed as a dual-port RAM and has a second address input A1 for an input signal AL and a second output D1 for an output signal DL.

Connections lead from the output side of an operation control unit ST with inputs KN and RESET and outputs ENK and READY to control inputs of the first multiplexer M1 and second multiplexer M2, to release inputs EN of the second multiplexer M2 and first storage RAM1 and to write inputs W of the first storage RAM1 and second storage RAM2. There are connections between clock outputs of the operation control unit ST, respectively, CLK-R1 and the first register R1, CLK-R2 and the second register R2, CLK-R3 and the third register R3, CLK-Z and the counter Z, to a load input L of the counter Z and to release inputs EN of registers R1 and R2. Further, the operation control unit ST is connected on the input side with an end-message line $\bar{U}$ of the counter Z, with two lines of the comparator C and with a line of the null indicator N.

Fig. 2 shows structures of a surface which are composed of image points and have different characteristics in the form of gray values. The numbers entered in the drawing are identification numbers which are allocated in a known manner to image point groups as part of data records, the image point groups having at least one image point.

Accordingly, the two figures on line zero, each of which is formed by one image point, can be described by means of the following run-length-coded data records:

Data record 1

line number: 0

starts in column: 4

run length: 1

identification number: 1

gray value: 10

Data record 2

line number: 0

starts in column: 10

run length: 1

identification number: 2

gray value: 10

Analogous data records are associated with the image point groups in the following lines, e.g., for the image point groups in line 2:

	<u>Data record 1</u>	<u>Data record 2</u>	<u>Data record 3</u>
	line number: 2	line number: 2	line number: 2
	starts in column: 5	starts in column: 16	starts in column: 37
	run length: 8	run length: 12	run length: 2
5	identification number: 1	identification number: 4	identification number: 4
	gray value: 10	gray value: 30	gray value: 30

10 Ambiguities resulting as equivalences, so called, which occur when image point groups of one line have connections to a plurality of image point groups of the preceding line which have identical characteristics but different identification numbers, occur, e.g., between the image point groups with identification number 1, identification number 3 or identification number 2.

The total number of equivalences from Fig. 2 which are in stored form for further processing is compiled in Table 1 by identification number. Table 2 and Table 3 anticipate the results achieved by the invention.

Table 1
equivalences

Table 2
intermediate code
in first storage
RAM1

Table 3
allocation table
according to classification
in second storage
RAM2

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No.	KN1	KN2	Address	data	Address	Data
10	1	3	1	0	1	1
	2	2	2	1	2	1
	3	4	3	1	3	1
	4	5	4	0	4	4
	5	6	5	4	5	4
	6	4	6	4	6	4
	7	8	7	0	7	7
15	8	12	8	4	8	4
	9	10	9	0	9	9
	10	15	10	8	10	4
	11	11	11	7	11	7
	12	7	12	4	12	4
20			13	0	13	13
			14	0	14	14
			15	11	15	7
			16	0	16	16
			17	15	17	7
			18	0	18	18

By means of a RESET signal at the operation control unit ST, the latter causes the counter Z to apply a null address to the first multiplexer M1. At the same time, the operation control unit ST controls the first multiplexer M1 and second multiplexers M2 via

control lines so that the counter value of counter Z is set at the third register R3 from the output of the multiplexer M1 and a null identification is present at the data input of the first storage RAM1. By means of a clock signal CLK-Z of the operation control unit ST, the counter value of counter Z is adopted in register R3 and is present at the first storage RAM1 as address.

The operation control unit ST then writes the null identification to the addressed storage location in the first storage RAM1 and increments the counter Z. This process is repeated in all storage locations of the first storage RAM1 until the entire first storage RAM1 is written with the null identification. After entering the null identification in all storage locations of the first storage RAM1, a change of state is effected as is required for processing the equivalences.

A signal KN from a storage, not shown, activated at the input of the arrangement indicates that equivalences have been stored in the storage.

As the result of a signal ENK of the operation control unit ST, a pair of identification numbers KN1 and KN2 describing an equivalence is applied to the respective inputs. The comparator C compares the two identification numbers KN1 and KN2. If the two identification numbers KN1 and KN2 are identical, no evaluation takes place. Otherwise, a control signal is applied to the operation control unit ST which, after evaluating this signal, switches through the identification number with the greater value to the multiplexer M1 as first identification number via its control lines. Of course, the process according to the invention can also be realized when the smaller of the two identification numbers is always used as the first identification number. Accordingly, this identification number is present at register R3 as input value and is stored in register R3 by a subsequent clock signal of the operation control unit ST. Since the output of register R3 is constantly enabled or released, the identification number is also present at the address inputs of the first storage RAM1 and second storage RAM2 as well as at registers R1 and R2. The operation control unit ST then actuates the read mode of the first storage RAM1 via its control lines.

The storage contents of the storage location of the first storage RAM1, which storage location is addressed with the first identification number, that is, in the present example, the larger identification number, are present at the data output of storage RAM1 and proceed from the latter to the input of the multiplexer M1, the output of the multiplexer M2,

the data input of the second storage RAM2 and the null indicator N. The null indicator N informs the operation control unit ST as to whether or not the storage contents have a null identification. If a null identification is present, the operation control unit ST causes the first storage RAM1 to switch off this null identification at its output and releases the second
 5 identification number, the smaller one in the present example, to the output of multiplexer M2 so that it is present at the data input of the first storage RAM1. The value of the smaller identification number is stored in the storage location of the first storage RAM1 addressed with the larger identification number for the null identification by means of a write pulse of the operation control unit ST.

10 If there is no null identification, a search process is initiated in the first storage RAM1 by the following operation sequence:

Via its control lines, the operation control unit ST switches the multiplexer M1 to a state in which the value present at the output of the first storage RAM1 is released to register R3 and enters this value in register R3 by a clock signal CLK-R3. In the manner already described,
 15 the null indicator N checks whether or not a null identification has been entered in the addressed storage location. This operation is repeated until a null identification is reported by the null indicator N to the operation control unit ST. The search process is then interrupted. The address in register R3 is stored in register R1 by the operation control unit ST in that the latter generates a clock signal CLOCK-R1. The smaller identification number is then applied
 20 to the first storage RAM1 by the operation control unit ST in the same way and a search process for a null identification is initiated in the manner described above. The address of the null identification of the smaller identification number is then stored in register R2. The source of the identification numbers is subsequently switched to inactive by means of control signal ENK and the outputs of registers R1 and R2 are applied to the inputs KN1 and KN2 so that
 25 the register values are now treated as identification numbers KN1 and KN2.

As soon as an entry has been made in the first storage RAM1 for all equivalences identifiable in the input signal KN, a change of state occurs in the circuit arrangement for the purpose of generating an allocation table. The counter Z is started and a value is transmitted as null address to the first storage RAM1. The storage contents of the
 30 addressed storage location are read by the null indicator N. If the null identification is still entered in the storage location, the operation control unit ST switches the first storage RAM1

into the inactive state via its control line and causes the multiplexer M2 to release the counter value at its output EN. The counter value is entered in storage RAM2 by a write pulse W. The counter state is then incremented and the process is repeated for all storage locations having a null identification in the first storage RAM1. If a storage location having no null
 5 identification in storage RAM1 is determined, the operation control unit ST sets the multiplexer M1 to a setting in which the storage contents of the first storage RAM1 are present at the output of the multiplexer M1 and accordingly at the input of register R3.

The address previously present at the first storage RAM1 is stored in register R1 by a signal CLK-R1 and CLK-R3 and the contents of the first storage RAM1 are entered
 10 in register R3 as a new address for the first storage RAM1. The first storage RAM1 is again checked by the null indicator N for the presence of a null identification. If there is no null identification, the contents of the addressed storage location of the first storage RAM1 are once again entered as subsequent address in register R3. This process is repeated until a storage location with a null identification has been found.

15 The address of this storage location is entered in register R2 by a control signal CLK-R2. At the same time, register R1 is released by operation control unit ST to input KN1 and, by controlling the multiplexer M1, input KN1 is released to register R3. The contents of register R1 are transferred to register R3 by a control signal CLK-R3 of the operation control unit ST.

20 The output of register R2 is then released to the input of the multiplexer M2 by means of the operation control unit ST and the multiplexer M2 is caused to release the contents of register R2 to its output. This value is entered in the second storage RAM2 by a write pulse of the operation control unit ST.

25 The counter value is then incremented and the test for null identification of the subsequent storage location in the first storage RAM1 is restarted in the manner described above until all storage locations of the allocation table are entered in the second storage RAM2. The operation control unit ST detects this state by means of a status signal $\bar{U}$ of counter Z, terminates the operation and reports this state with a READY signal via the READY line.



Patent Claims

1. Process for recognizing topologically contiguous image structures arranged in line form in which image point groups formed by at least one image point and having identical characteristics within a line receive consecutive identification numbers and image point groups of a following line adopt already allocated identification numbers from the image point groups first adjoining them by at least one image point in the line direction, characterized in that,
in a first process step, one identification number of a pair of identification numbers of adjoining image point groups with different identification numbers serves as an address value for a first addressed storage with a marked initial state for each storage location and the other identification number becomes the data value of the storage location addressed with the first identification number when the storage location has the marked initial state,
otherwise, in a second process step, the other identification number and the data value of the addressed storage location are used as address values for determining storage locations with a marked initial state whose address values become identification numbers to which the first process step is applied,
wherein a respective data value determined for an address value once again serves as an address until a storage location with the marked initial state is found, and pairs of identification numbers leading to identical address values in the second process step are ignored,
and in that, in a third process step for forming an allocation table in the form of a second addressable storage, storage locations corresponding to the address values from the first process step receive the address value itself as a data value when the address value has the marked initial state,
otherwise, when the address value does not have the marked initial state, a contained data value is used as address value until a storage location with the marked initial state is found whose address value becomes the data value for the address value without the marked initial state.



2. Circuit arrangement for recognizing topologically contiguous image structures arranged in line form by means of processing a pair of different identification numbers of image point groups which have at least one image point and adjoin one another within the image structures in adjoining lines, wherein the identification numbers for the image point groups in a line are allocated consecutively and image point groups of a following line adopt already allocated identification numbers of image point groups first adjoining them by at least one image point in the line direction, characterized in that
- a first multiplexer (M1) and second multiplexer (M2), one of whose inputs is connected in each instance with the count value output of a counter (Z), an input of the second multiplexer (M2) being connected to fixed voltage, and a comparator (C) have inputs for the identification numbers (KN1) and (KN2) and, in addition, are connected to outputs of a first register (R1) and second register (R2) whose data inputs are connected to an output of a third register (R3) which is further coupled with the respective address input of a first storage (RAM1) and a second storage (RAM2), the input of the third register (R3) being connected with the output of the first multiplexer (M1),
- in that a data input and data output (D) of the first storage (RAM1) is coupled with an additional input of the first multiplexer (M1), the data output of the second multiplexer (M2), the input of a null indicator (N) and a data input (D) of the second storage (RAM2) which also has an address input (A1) for an input signal (AL) and an output (D1) for an output signal (DL),
- and in that connections on the output side of an operation control unit (ST) with inputs (KN) and (RESET) and outputs (ENK) and (READY) lead to control inputs of the first multiplexer (M1) and second multiplexer (M2), to release inputs (EN) of the second multiplexer (M2) and first storage (RAM1) and to write inputs (W) of the first storage (RAM1) and second storage (RAM2), as well as connections between a clock output (CLK-R1) and the first register (R1), a clock output (CLK-R2) and the second register (R2), a clock output (CLK-R3) and the third register (R3), a clock output (CLK-Z) and the counter (Z), to a load input (L) of the counter (Z) and to release inputs (EN) of the first register (R1) and second register (R2), and the operation



control unit (ST) is connected on the input side with an end-message line ($\bar{U}$) of the counter (Z), with two lines of the comparator (C) and with a line of the null indicator (N).