

OPERATION ACCELERATOR

ABSTRACT

The present invention relates to the field of data calculation technologies, and discloses an operation accelerator, to reduce time for performing a multiplication operation on two $N \times N$ matrices. The operation accelerator includes: a first memory, a second memory, an operation circuit, and a controller. The operation circuit may perform data communication with the first memory and the second memory by using a bus. The operation circuit is configured to: extract matrix data from the first memory and the second memory, and perform a multiplication operation. The controller is configured to control, according to a preset program or instruction, the operation circuit to complete the multiplication operation. The operation accelerator may be configured to perform a multiplication operation on two matrices.

Figure 5