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(54) Title: VECTOR PROCESSING FOR IN-MEMORY COMPUTING

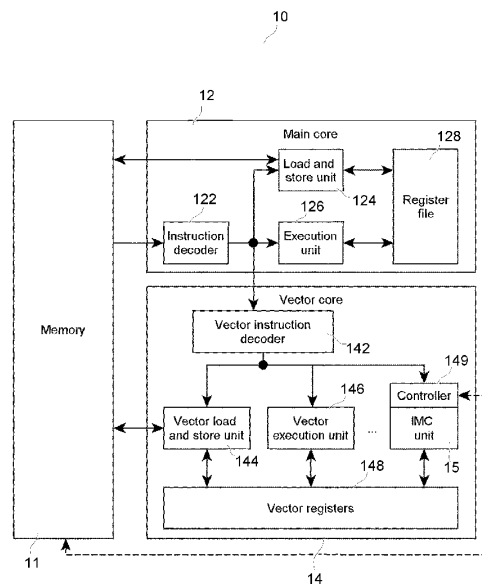


FIG. 1

(57) Abstract: The invention is notably directed to an information-processing apparatus (10), which basically includes a vector processing unit (VPU) and an in-memory compute unit (IMC unit). The VPU (14) has vector registers designed to store vector components. The IMC unit (15) has a crossbar array structure, which is adapted to store values (called weights). The IMC unit is connected to the vector registers (148) of the VPU. The information-processing apparatus is configured to perform several operations, including vector transit operations, vector feed operations, and vector readout operations. In operation, the vector transit operations cause to store vector components of input vectors in the vector registers of the VPU. Such components are typically fetched from a neighbouring memory (11), upon receiving corresponding instructions from a main processing unit (12), to which the VPU is connected. The vector feed operations feed the input vector components as input to the IMC unit, from the vector registers. This, in turn, causes the IMC unit to perform matrix-vector multiplications based on the weights and the input vector components, to accordingly obtain output vectors. Finally, the vector readout operations write output vector components of the output vectors in the vector registers. From this point on, the output vector components can be transferred to the memory or the main processing unit (for further processing), or further processed in the VPU, prior to being transferred to the memory or the main processing unit. The invention is further directed to related systems and methods.

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GQ, GW, KM, ML, MR, NE, SN, TD, TG).

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