

LIQUID-CRYSTAL-ON-SILICON DISPLAY WITH
PHOTOLITHOGRAPHIC ALIGNMENT POSTS
AND OPTICAL INTERFERENCE LAYERS

BACKGROUND OF THE INVENTION

(1) Field of the Invention

This invention relates to the method of fabrication of alignment posts and optical interference layers directly on silicon wafers with liquid crystal material and to the unique resulting device structure.

(2) Description of the Prior Art

The picture quality of liquid crystal displays from a simple seven segments to millions of pixels is determined by the structure used to control the variation of thickness and position leads after wafer processing. There are known processes for creating insulated alignment posts based on preformed glass microspheres and rods; relatively low series resistance posts can be obtained by means of selective deposition of polysilicon and metallic silicide. (Making of

metallic vias and contacts are a comparatively well known processing art.)

U. S. Patent 5,498,925 to Bell et al describes the formation of posts in flat panel displays using processes based on a heat-treated slurry or paste upon a glass plate. U. S. Patent 5,597,736 teaches the function of a light-blocking layer deposited upon a semiconductor substrate material that can emit light. Until now, it has been difficult to construct alignment posts using photolithography and also add optical interference layers simultaneously onto a semiconductor substrate material.

BRIEF SUMMARY OF THE INVENTION

A principal object of the present invention is to describe a new structure for building a flat-panel liquid-crystal display upon an integrated circuit (IC) die with inter-related alignment between the posts supporting the overlaying glass cover plate and optical interference layers (OIL) employed to improve image quality. The alignment posts are made of silicon nitride, and the OIL of silicon nitride/oxide multilayers.

Another object of this invention is to describe effective and very manufacturable methods of photolithographic formation of insulating alignment posts (also called studs or pillars). These methods can be used

in processing many different device types, and are described in this application for liquid crystal display devices as a way of illustrating their embodiment at a pixel density beyond that achievable with preformed micro-glass spheres and rods.

A further object of the present invention is to describe methods of deposition for both the posts and the optical interference layers that are independent of each other and retain their desired feature during deposition of subsequent features.

In accordance with the objects of this invention, a new method of forming insulating material alignment posts associated with active device structures is achieved. A silicon wafer having patterned active device therein and thereon is formed and the insulating material alignment posts are deposited in a pattern over the pattern of the active device structures. Furthermore a device structure that combines insulating materials for alignment posts and optical interference layers associated with an active device structure in a silicon body is achieved. A silicon semiconductor wafer having patterned active device structures and alignment posts is formed and the whole structure is covered with an optical interference layer;

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings, there is shown:

Figs. 1 through 3 schematically illustrate in cross-sectional representation a preferred embodiment of the device structure of the present invention. The process flow for making the alignment posts and the optical interference layers is shown in Figs. 4 to 10.

Fig. 10 schematically illustrates in cross-sectional representation the final embodiment of this invention for this liquid-crystal-on-silicon display device. The bonding pad is shown.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to Fig. 1, here is shown a portion of a partially completed integrated circuit liquid-crystal display. The glass cover plate 10 provides the transparent enclosure for the external incident light to be reflected back to an observer. The strength of reflected light is dependent on the light polarization, absorption and light scattering properties of each liquid-crystal display pixel, which is controlled by the electrical field established within the liquid crystal material 11. The IC die 12, separated from the glass plate by the alignment posts 14 generates these E-fields. The resultant space

between the glass plate and the silicon wafer is filled with the chosen liquid crystal material. Light, either provided or ambient, enters the open face of the liquid-crystal-on-silicon and is reflected from the underlying pixels to form a viewable pattern of polarized light, i.e. the image is viewed directly or projected through an optical polarized system. Such microdisplays may contain more than one-thousand columns by more than one-thousand rows (totally over one-million pixels) in a square surface area less than one inch diagonal; the pixel pitch can be made less than 10 micrometers (microns), and has been achieved as low as 5 microns with an interpixel gap of one micron or less. When alignment posts are placed between adjacent pixels, the interpixel gap has been fabricated at a typical distance of 0.6 microns with a range from 0.55 to 0.85 microns.

The glass cover has a transparent conductive coating on its inner surface, which is the common electrode for the entire pixel array.

Fig.2 illustrates the bonding pads 20 on the IC die to which the external wires 22 are attached. The silicon wafer contains the embedded control circuits that activate the pixel patterns in the viewable area 24. The refractive index anisotropy of the liquid crystal is influenced by the electric fields above the IC surface. A small change in voltage makes a large change in the optical transmission. Because this invention teaches the photolithographic making

of patterns of alignment posts, the ratio of pixels 30 to posts 14 is often fabricated in the range 20:1 to 50:1. As shown in Fig. 3, the photolithographic method permits these alignment posts to be constructed in the space between adjacent pixels.

The process steps for making the alignment posts and optical interference layers is shown in Figures 4 to 10. Starting with Fig. 4, the conductive metallic layer 30 is formed over the silicon oxide 40, which is formed on top of the metal layer 41 on the IC. A silicon semiconductor substrate 15 has active devices therein and an insulating layer 16 upon which metal layer 41 is formed. Then a photoresist layer is laid down over the metal 30 to construct the pixels. The photoresist is exposed and a portion removed to provide that each pixel retains a metallic layer, which shall act as a mirror reflector for the light incident upon said pixel. If aluminum were chosen as the metallic mirror, its 90% reflectivity would improve to near 100% with the addition of the overlaid optical interference layer. The remaining photoresist is stripped and the entire structure is covered with silicon nitride 50 by PECVD and to a thickness of between about five-thousand to ten-thousand Angstroms as in Fig. 5. Then the standard photoresist and etching methods are used to create the posts mask 60 shown in Fig. 6. The alignment posts 14 are

created by selection of a chemical removal process that stops at the metal 30 and the silicon oxide 40.

After the resist is stripped, as shown in Fig. 7, the device is ready to be covered with the optical interference layers 80. Optical interference layers are used to improve light reflections. Careful attention is required in constructing these optical interference layers so as not to disturb any underlying devices and posts. The OIL covering is considered to be an optional addition. The added expense of the OIL covering may be avoided in some cases of lower image quality. The LCD-on-silicon device could be completed and used functionally without adding the OIL after the formation of the alignment posts.

The optional optical interference layer coating is composed of multiple layers of insulating material with properties of varying optical indices of refraction, as shown in Fig. 8. Oxides and nitrides have been applied in the fabrication of these multilayer stacks. It is critical to have SiO_x as the bottom layer to match the index of refraction of the substrate.

Durable, uniform and reproducible amorphous silicon nitride multilayer coatings deposited by PECVD are known optical interference filters in the near infrared. Optical interference coatings for the visible spectrum made from

four or more layers of oxide/nitride/oxide/nitride formed for this application are considered to be novel and worthy for this patent application.

To attach the wires to the IC via bonding pads, a photoresist mask is formed with openings over the location of the bond pads and the material is removed to metallic layer 41. Then the photomask is removed, leaving the finished device structure shown in Fig. 10.

The existence of numerous alignment posts permits the usage of ultra-thin glass plate or cover over the liquid crystal. This implementation results in lightweight displays for portable applications. Glass covers supported by alignment posts are typically 0.5 millimeters in thickness, and can range from 0.2 to 0.8 millimeters.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. A method of forming insulating material alignment posts and optical interference layers associated with active devices comprising:

 providing a silicon semiconductor wafer having patterned said active devices therein and thereon;

 forming said insulating material alignment posts in a pattern over said pattern of active devices; and

 forming said optical interference multilayer stack over said alignment posts and said active devices.
2. The method of claim 1 wherein said alignment posts are composed of silicon nitride.
3. The method of claim 1 wherein said alignment posts have a height between about 5000 to 10,000 Angstroms.
4. The method of claim 1 wherein said alignment posts are formed by a process of photolithographic formation.
5. A method according to claim 1 wherein said optical interference layers have a total thickness of between 3000 and 3500 Angstroms.
6. The method of claim 1 wherein said optical interference multilayer stack is formed by the process of PECVD.
7. A method of forming a device structure that combines insulating materials for silicon nitride alignment posts and optical interference layers associated with active devices in a silicon body comprising:

 providing a silicon semiconductor wafer having a

pattern of said active devices therein and thereon;

forming a first metallic layer there over;

forming a silicon oxide insulating layer over the said first metallic layer;

forming a second metallic layer over the said silicon oxide layer;

forming a photoresist mask over the said second metallic layer having a covering over the location of each planned pixel of the device structure;

removing the said second metallic layer not covered by the said photoresist mask;

removing the said photoresist mask to provide that each said pixel retains said metallic layer, which shall act as a mirror reflector for the light incident upon said device structure;

forming a silicon nitride layer of thickness 5000 to 10,000 Angstroms to achieve desired height of the alignment posts;

forming a photoresist mask over the said silicon nitride layer to cover the location of each planned nitride post;

etching said silicon nitride layer to form said posts of silicon nitride and stopping said etch at the metallic pixels and the said silicon oxide layer;

removing the said photoresist mask; and

forming optical interference layers of silicon

oxide/silicon nitride/silicon oxide/silicon nitride over said silicon nitride posts, said second metallic layer and said silicon oxide layer.

8. A method according to claim 7 wherein said alignment posts have a height of between about 5000 to 10,000 Angstroms.

9. A method according to claim 7 wherein said optical interference layers have a total thickness of between 3000 and 3500 Angstroms.

10. A method according to claim 7 wherein said alignment posts are formed by a process of photolithographic formation.

11. The method of claim 7 wherein said optical interference multilayer stack is formed by the process of PECVD.

12. A device structure having a pattern of active devices comprising:

a silicon semiconductor substrate having active devices therein and thereon;

insulating material alignment posts in a pattern over said pattern of active devices; and

optical interference multilayer stack over said alignment posts and said pattern of active devices.

13. The device structure of claim 12 wherein said alignment posts are composed of silicon nitride.

14. The device structure of claim 12 wherein said alignment posts have a height of between about 5000 to 10,000 Angstroms.

15. The device structure of claim 12 wherein said alignment posts are formed by the process of photolithographic formation.

16. A method according to claim 12 wherein said optical interference layers have a total thickness of between 3000 and 3500 Angstroms.

17. The device structure of claim 12 wherein said optical interference layers are formed by the process of PECVD.

18. A device structure that combines insulating materials for alignment posts and optical interference layers associated with active devices in a silicon body comprised of:

a silicon semiconductor wafer having a pattern of said active devices therein and thereon;

said alignment posts located between the said pixels on said semiconductor wafer and the whole structure being covered with optical interference layers;

liquid crystal material located in valleys below peaks of the alignment posts;

bonding pads on the said silicon body, outside the area of liquid crystal material, having wire attached and said wire connected to external contacts for the control logic and power;

glass cover laid upon and supported by the alignment posts to encapsulate the said liquid crystal material, but not over the area outside the liquid crystal

material where the bonding pads are located.

19. The device structure of claim 18 wherein said alignment posts are composed of silicon nitride.

20. The device structure of claim 18 wherein said alignment posts have a height between about 5000 to 10,000 Angstroms.

21. The device structure of claim 18 wherein said alignment posts are formed by the process of photolithographic formation.

22. A method according to claim 18 wherein said optical interference layers have a total thickness of between 3000 and 3500 Angstroms.

23. The device structure of claim 18 wherein said optical interference layers are formed by the process of PECVD.

24. The device structure according to claim 18 comprising said optical interference layers over said alignment posts and active devices.

25. The device structure of claim 24 wherein said optical interference layer is composed of silicon oxide/silicon nitride/silicon oxide/silicon nitride.

26. The device structure of claim 24 wherein said optical interference layers provide the advantages of: 1) better field of view for projection optics; 2) greater direct viewing angle; 3) better color contrast ratios, saturation or balance from a pixel.