CLAIMS

What is claimed is:

1. A processor comprising:

a general purpose processor core;

one or more graphics processor cores to process instructions to perform graphics operations;

interconnect logic having at least one data channel, to interconnect the one or more graphics processor cores, and couple the graphics processor cores with a shared resource;

wherein the interconnect logic to enable data distribution between the graphics processor cores and the shared resource over a virtual channel; and

wherein the virtual channel to include a programmable traffic classification system having multiple traffic classifications.

2. The processor of claim 1, wherein the at least one data channel is a shared bus.

3. The processor of claim 1, wherein the interconnect logic includes multiple data channels.

4. The processor of claim 3, wherein each of the multiple data channels is a separately clock gated bus, and wherein each bus to use early indications to signal incoming activity.

5. The processor of claim 1, wherein the shared resource is a shared memory resource.

6. The processor of claim 5 wherein the shared memory resource is a shared cache.

7. The processor of claim 1, wherein the interconnect logic to enable the data distribution over multiple virtual channels.

8. The processor of claim 7, wherein the multiple virtual channels to be arbitrated based on a programmable priority system.

9. The processor of claim 7, wherein the programmable traffic classification system to assign at least one of the multiple traffic classifications to a single virtual channel of the multiple virtual channels.

10. The processor of claim 1, wherein the multiple traffic classifications include a programmable priority.

11. The processor of claim 10, wherein the programmable priority is relative to traffic classifications within a single virtual channel of the multiple virtual channels.

12. The processor of claim 1 wherein the interconnect logic operates at a higher frequency than the one or more graphics processor cores.

13. The processor of claim 1, wherein the one or more graphics processor cores comprise a three-dimensional (3D) integrated circuit stack including multiple graphics processor cores.

14. A system comprising:

a processor including a plurality of cores, at least one core including an instruction set for processing graphics instructions, wherein the at least one core couples with a shared resource on the processor via interconnect logic having at least one clock gated physical data channel and one or more virtual channels, each virtual channel to carry data having multiple programmable traffic classifications, wherein each the multiple programmable traffic classifications are assigned to one of multiple prioritized virtual channels; and

memory coupled to the processor.

15. The system of claim 14, wherein the processor includes a three-dimensional (3D) integrated circuit stack including multiple graphics processor cores.

16. An apparatus comprising:

means for determining a channel access status on a multiple node shared bus for a message from a source node to a target node, wherein at least one of the multiple nodes couples with a graphics processor core and at least one of the nodes couples with a shared resource;

means for transmitting a message from the source node to a target node over a first data channel, wherein the message includes a first traffic classification having a first priority;

means for receiving the message at a first data bus connector coupled with a first graphics processor core; and

means for based on at least the source node and the target node, switching the message from a first data channel to a second data channel.

17. The apparatus of claim 16, wherein the means for determining channel access comprises:

means for determining, using a channel access protocol, if a third data channel is available to transmit a message; and

means for transmitting a message over the first data channel after determining that transmission over the third data channel is blocked.

18. The apparatus of claim 17, wherein the first, second, and third data channel are virtual data channels.

19. The apparatus of claim 17, wherein the channel access protocol is a time division multiple access protocol.

20. The apparatus of claim 17, wherein the channel access protocol is a carrier sense multiple access protocol.

21. The apparatus as in any one of claims 16-20, further comprising at least one three-dimensional (3D) integrated circuit stack including multiple graphics processor cores.

22. A machine-implemented method comprising:

determining a channel access status on a multiple node shared bus of a three-dimensional (3D) integrated circuit stack including multiple graphics processor cores, the channel access status for a message from a source node to a target node, wherein at least one of the multiple nodes couples with at least one of the multiple graphics processor cores and at least one of the nodes couples with a shared resource;

transmitting a message from the source node to a target node over a first data channel, wherein the message includes a first traffic classification having a first priority;

receiving the message at a first data bus connector coupled with a first graphics processor core; and

based on at least the source node and the target node, switching the message from a first data channel to a second data channel.

23. The method of claim 22, wherein determining channel access comprises:

determining, using a channel access protocol, if a third data channel is available to transmit the message; and

transmitting the message over the first data channel after determining that transmission over the third data channel is blocked, wherein the channel access protocol includes one or more of time division multiple access and carrier sense multiple access.

24. The method of claim 23, wherein the first, second, and third data channel are virtual data channels.

25. A machine-readable medium having stored thereon data, which if performed by at least one machine, causes the at least one machine to fabricate at least one integrated circuit to perform a method as in any one of claims 22-24.

CLAIMS

What is claimed is:

1. A processor comprising:

a general purpose processor core;

one or more graphics processor cores to process instructions to perform graphics operations; and

interconnect logic having at least one data channel, to interconnect the one or more graphics processor cores, and couple the one or more graphics processor cores with a shared resource, wherein the interconnect logic is to enable data distribution between the one or more graphics processor cores and the shared resource over a virtual channel, and wherein the virtual channel is to include a programmable traffic classification system having multiple traffic classifications.

2. The processor of claim 1, wherein the at least one data channel is a shared bus.

3. The processor of claim 1, wherein the interconnect logic includes multiple data channels.

4. The processor of claim 3, wherein each of the multiple data channels is a separately clock gated bus, and wherein each bus is to use early indications to signal incoming activity.

5. The processor of claim 1, wherein the shared resource is a shared memory resource.

6. The processor of claim 5 wherein the shared memory resource is a shared cache.

7. The processor of claim 1, wherein the interconnect logic is to enable the data distribution over multiple virtual channels, the multiple virtual channels including the virtual channel and one or more additional channels.

8. The processor of claim 7, wherein the multiple virtual channels are to be arbitrated based on a programmable priority system.

9. The processor of claim 7, wherein the programmable traffic classification system is to assign at least one of the multiple traffic classifications to a single virtual channel of the multiple virtual channels.

10. The processor of claim 9, wherein each of the multiple traffic classifications of the programmable traffic classification system includes a programmable priority.

11. The processor of claim 10, wherein the programmable priority is relative to traffic classifications within a same virtual channel of the multiple virtual channels.

12. The processor of claim 1, wherein the interconnect logic operates at a higher frequency than the one or more graphics processor cores.

13. The processor of claim 1, wherein the one or more graphics processor cores comprise a three-dimensional (3D) integrated circuit stack including multiple graphics processor cores.

14. A system comprising:

a processor including a plurality of cores, at least one core including an instruction set for processing graphics instructions, wherein the at least one core is to be coupled with a shared resource on the processor via interconnect logic having at least one clock gated physical data channel and a set of virtual channels including one or more virtual channels, each virtual channel in the set of virtual channels to carry data having multiple programmable traffic classifications, wherein each of the multiple programmable traffic classifications are to be assigned to a single virtual channel in the set of virtual channels; and

memory coupled to the processor.

15. The system as in claim 14 wherein the shared resource on the processor is a shared memory resource.

16. The system as in claim 15, wherein the shared memory resource includes a shared cache memory.

17. The system of claim 14, wherein the set of virtual channels includes multiple virtual channels, wherein the multiple virtual channels in the set of virtual channels are to be arbitrated based on a programmable priority system.

18. The system of claim 17, wherein each of the multiple programmable traffic classifications is prioritized relative to other traffic classes assigned to the same virtual channel of the multiple virtual channels.

19. The system of claim 14, wherein the processor includes a three-dimensional (3D) integrated circuit stack including multiple graphics processor cores.

20. A machine-readable medium having stored thereon data, which if performed by at least one machine, causes the at least one machine to fabricate at least one integrated circuit to perform a method comprising:

determining a channel access status on a multiple node shared bus for a message from a source node to a target node, wherein at least one node of the multiple node shared bus couples with a graphics processor core and at least one node of the multiple node shared bus couples with a shared resource;

transmitting a message from the source node to the target node over a first data channel, wherein the message includes a first traffic classification having a first priority;

receiving the message at a first data bus connector coupled with the graphics processor core; and

based on at least the source node and the target node, switching the message from the first data channel to a second data channel.

21. The machine-readable medium of claim 20, wherein the at least one integrated circuit is a three-dimensional (3D) integrated circuit stack including multiple graphics processor cores.

22. The machine-readable medium of claim 20, wherein determining the channel access status comprises:

determining, using a channel access protocol, if a third data channel is available to transmit the message from the source node to the target node; and

after determining that transmission over the third data channel is blocked, transmitting the message over the first data channel.

23. The machine-readable medium of claim 22, wherein the first, second, and third data channel are virtual data channels.

24. The machine-readable medium of claim 22, wherein the channel access protocol is a time division multiple access protocol.

25. The machine-readable medium of claim 22, wherein the channel access protocol is a carrier sense multiple access protocol.