

PATENT SPECIFICATION

(11) 1322 516

DRAWINGS ATTACHED

- (21) Application No. 46439/70 (22) Filed 30 Sept. 1970
 (31) Convention Application No. 862759 (32) Filed 1 Oct. 1969
 (31) Convention Application No. 888391 (32) Filed 29 Dec. 1969 in
 (33) United States of America (US)
 (44) Complete Specification published 4 July 1973
 (51) International Classification H03F 1/34 3/04
 (52) Index at acceptance
 H3T 1A1 1A2 1N1 2J 2P 2T2Z 2T3F 2T3J 3J 3N 3P
 4A1 4A2 4A3 4C 4E1N 4E2N 4G 4M 4P 5E 5S



(54) SIGNAL TRANSLATING STAGE

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a signal translating stage which in the embodiments herein described is capable of accepting signals at various bias levels within the dynamic range for signal variations permitted by the voltage of an associated power supply, of amplifying or attenuating such signals, and of supplying output signals at a bias permitting full utilization of that dynamic range. Such signal translating stage can provide a highly linear transfer function for signals applied to either a low-impedance or a high-impedance input terminal thereof. Low-impedance input terminals of two such signal translating stages can be coupled together to provide a differential amplifier for signals applied to the high-impedance input terminals, giving a configuration which offers not only high input impedance but also high voltage gain and an output signal voltage range approximately equal to the amplifier power supply voltage.

These signal translating stages are well suited for use in monolithic integrated circuitry because they may employ transistors of the same conductivity characteristics, they can be entirely direct coupled, and they can be used to re-bias signals to supply utilise limited dynamic range for signal potential variations.

As used herein, the term monolithic integrated circuit refers to a solid state structure wherein a plurality of active semiconductor devices such as transistors and diodes, and passive circuit components such as capacitors and resistors, are constructed of common materials and interconnected by s

sequence of processing steps on a common substrate of semiconductor material. The invention, however is suited to implementation using various forms of electronic devices of discrete nature or of other integrated circuit technology. Thus vacuum tubes, bipolar transistors, or any of the various field effect transistors may be used as power gain devices in implementing those aspects of the present invention wherein specific forms of these devices are not particularised.

In accordance with one aspect of the present invention, a signal translating stage incorporates a plurality of three-terminal power gain devices, such as transistors. As herein meant, each such device has input, output and common electrodes such that application of an input signal between the input and common electrodes can provide an output signal between the output and common electrodes having higher power than the input signal. Terminals are provided by which input signals can be applied across the input and common electrodes of a first one of these power gain devices, the input signals normally being supplied from a source having an associated source impedance. The common electrode of the first power gain device is DC coupled (i.e. direct current conductively coupled) to the output electrode of a second of the power gain devices. The output electrode of the first power gain device is D.C. coupled through first impedance means to one of two operating potential supply terminals: it is also coupled by mutually similar couplings to the input electrodes of the second and a third power gain devices. The input electrodes of each of the three power gain devices are each arranged to be supplied with DC bias with respect to the other of the supply terminals, which can be at a reference potential (e.g. ground). The common electrodes of the second and third power gain devices are DC coupled to the last mentioned terminal by, for example, a resistive or direct connection. The output electrode of the third power gain device can provide

translated output signals to utilization means (e.g., a load resistor which also provides direct current bias for the third device).

Such a configuration, when constructed using transistor as the power gain devices, provides a low input impedance at the emitter electrode (common electrode) of the first transistor (power gain device), and therefore is useful as a current sampling circuit which may be coupled serially in the path of the sampled current. When utilized in a resonant circuit, undesirable lowering of the Q of the tuned circuit is therefore prevented. Such a circuit is described in detail in our Application No. 46438/70 (Serial No. 1317625). Furthermore, in such a current sampling circuit, the direct voltage at the base (input) electrode of the first transistor conveniently may be adjusted to be the same as the direct voltage level of the sampled circuit. The low impedance input further makes it possible to utilize a variation of this embodiment to algebraically combine input signals with isolation between the inputs.

In the design of electronic amplifier circuits, and particularly where such circuits are constructed in monolithic integrated form, it is advantageous to utilize differential amplifier arrangements. Differential amplifiers provide a large number of advantages including the use of a minimum number of capacitors, the avoidance of use of large value resistors, dependence of gain on resistor ratios rather than absolute values, wide frequency operating range, stability, push-pull or single-ended inputs and/or outputs and a wide range of functions which are facilitated by the plurality of input and output terminals of such an amplifier.

One widely used differential amplifier arrangement employs a pair of amplifier transistors having their emitters coupled to a common constant current source transistor. One or more inputs are supplied to the bases of the amplifier transistors and outputs may be derived across load impedances coupled to the collectors of the amplifier transistors. Signals may also be applied to the base of the current source transistor to provide such functions as automatic gain control, stabilization, mixing or demodulation. While such an arrangement is versatile and, in general, provides good performance, the available output signal voltage variations which may be developed across the collector load impedances are limited to a value substantially less than the total collector direct supply voltage. Typically, the available output signal voltage range is of the order of one-half the collector supply voltage. This undesirable limitation, which is also encountered in other differential amplifier arrangements utilizing transistors coupled in series across the direct voltage supply (i.e. stacked transistors), results from the fact that the amplifier transistors

are biased approximately at a voltage midway between the voltages provided at the direct voltage supply terminals associated with the differential configuration.

In the design of differential amplifiers, it is also desirable to provide an arrangement which is capable of linear reproduction of input signals which vary over a relatively wide range. In the widely used differential amplifier described immediately above, the output current (and therefore the output voltage across a resistive load) varies as an exponential function of the input difference voltage. The linear range of the transfer characteristic of such an amplifier is therefore limited to very low input voltages, unless substantial degenerative feedback is used to linearize the transfer characteristic, which feedback will also substantially reduce the voltage gain available from the amplifier. Such differential amplifiers also have input impedances which vary with applied signal levels and can therefore adversely affect the linearity of the source of applied signals.

In accordance with a further aspect of the present invention, a differential amplifier arrangement is provided capable of giving a relatively high voltage gain while preserving a linear relationship between input and output signals for a relatively wide range of input signals, the input signal level and voltage gain being sufficient to produce output signals up to a voltage comparable to the direct voltage difference between supply terminals associated with the amplifier.

Such a differential amplifier is constructed, according to another aspect of the invention, of two component signal translating stages, as previously described herein, each similar to the other, in which the common terminals of their respective first power gain devices are coupled to each other. Differential inputs for signal exist at the two input electrodes respectively of the first power gain device of each of the component configurations. Differential outputs for signal exist at the two output electrodes respectively of the third power gain device of each of the component configurations. The third power gain device in the second of the component configurations may be dispensed with and a single-ended output taken from the output of the first of the component configurations in the manner of the first described embodiment.

When constructed in integrated circuit form, for example, such differential amplifier can comprise first and second input transistors, first and second regulator transistors and at least a first output transistor. Each input transistor is arranged substantially as an emitter follower having its emitter direct coupled to the collector of the associated regulator transistor so that the latter forms part of an emitter load for the input transistor. The emitters of the input transistors are DC

coupled to each other while their collectors are coupled to voltage supply means via separate resistors. Direct current negative feedback is provided from the collector of each input transistor to the base of its associated regulator transistor so as to maintain substantially constant current in the input transistors. Input signals are applied between base and emitter of either or both of the input transistors and output signals may be derived across an impedance coupled to the output transistor. The base-emitter circuit of which is coupled in parallel with the base-emitter circuit of a corresponding one of the regulator transistors.

In an embodiment of this latter aspect of the invention, a resistance may be direct coupled between the emitters of the input transistors. Furthermore, an output transistor may be associated with each regulator transistor.

In many single stage transistor amplifiers, as the amplitude of an input signal varies, the base-to-emitter forward voltage drop also varies non-linearly because of the accompanying change of collector to emitter current in the transistor, and therefore produces distortion of the output signal. Also the input impedance of the transistor changes as the input signal modulates the collector to emitter current flow of the transistor which will cause distortion if the impedance of the signal source is not low. These effects are more pronounced when the magnitude of the input signal is increased.

In accordance with another aspect of the present invention, such non-linearities may be avoided by means of a signal translating stage wherein potential variations are applied to the base electrode of a first transistor while the emitter electrode of the transistor is coupled to a resistive load either directly or with a capacitor. In this signal translating stage, a second transistor (power gain device) functions as a regulator, e.g. a shunt regulator in parallel connection with the resistive load. The regulator second transistor acts to maintain a constant load upon the first transistor so the variation of base-to-emitter forward voltage drop and transistor input impedance caused by collector to emitter current variations of the first transistor are reduced. Input signal potential variations are coupled to the resistive load substantially without distortion, so the current variations in the resistive load are in proportion to the input signal potential variations. Since the second transistor is a regulator maintaining constant current flow through the collector-to-emitter path of the first transistor, its collector current flow varies in proportional dependence on the input signal variations. A third transistor (power gain device) is connected to have the same base-to-emitter signal variations as the second transistor. The second and third transistors exhibit similar characteristics so that the

collector current of the third transistor also varies in proportional dependence on the input signal potential variations. The third transistor can thereby provide an essentially distortion-free current at potentials close to a reference potential (ground). The output signals developed by this current across a load impedance coupled to a source of operating potential referred to the reference potential can swing over the full range of operating potential if the load is resistive or twice the full range of the operating potential if the load is a tuned circuit.

The invention in its various aspects may be better understood by reference to the various circuits shown in the drawings, in which:

FIGURE 1 illustrates in schematic diagram form an embodiment of the present invention utilized as a current sampler;

FIGURE 2 illustrates in schematic diagram form an embodiment of the present invention using three three-terminal power gain devices which are transistors;

FIGURE 3 is a schematic circuit diagram of a differential amplifier adapted for construction in integrated circuit form embodying the present invention, being composed of two component signal translating stages of the type shown in FIGURE 1 interconnected by resistive means; and

FIGURE 4 is a schematic circuit diagram of a differential amplifier adapted for construction in integrated circuit form embodying the present invention, being composed of two component signal translating stages of the type shown in FIGURE 1 interconnected by direct connection.

Referring to FIGURE 1, an input terminal 104 is coupled in the path of a current (I_i) to be sampled. A constant current stage comprising a transistor 102 includes an emitter electrode 102e coupled both to the input terminal 104 and to a collector electrode 106c of a variable conduction stage comprising a transistor 106. Operating power is coupled to the system via a B+ terminal which is coupled by means of a collector resistor 108 to a collector electrode 102c on transistor 102. A base electrode 102b on transistor 102 is coupled by means of terminal 110 to a direct voltage reference potential illustrated by the symbol V_{ref} in the figure. A feed-

back path from the collector electrode 102c of transistor 102 to a base electrode 106b of transistor 106 includes an avalanche diode 112 biased in avalanche mode by resistive means 108 and 114 serially coupled from B+ to a reference potential such as ground. This feedback path couples voltage variations appearing at the collector of transistor 102 to the base electrode 106b of transistor 106. Avalanche diode 112 provides the required direct voltage translation to bias transistor 106. This path may include other serially

coupled solid state devices (not shown) to provide signal coupling and direct voltage translation. Further, such an arrangement can provide temperature compensation for the biasing of the stage.

An emitter resistor 116 couples an emitter electrode 106e of transistor 106 to ground. An emitter resistor 118 is coupled from an emitter electrode 120e of an output stage comprising a transistor 120 to ground. Base electrode 120b on transistor 120 is coupled to base electrode 106b on transistor 106 and to a junction of avalanche diode 112 and resistor 114. A collector electrode 120c provides means for supplying the output current from the current sampler directly to a first current output terminal 122. Alternatively, the output current can be supplied via a further optional, output stage 140 illustrated by the circuit enclosed within the dashed lines in the figure.

The second output stage includes a transistor 142 having an emitter electrode 142e coupled to current output terminal 122. A base electrode 142b of transistor 142 is coupled to a second reference voltage. This voltage may be developed utilizing a resistor 144 and an avalanche diode 146 serially coupled from B+ to ground as shown. The regulated voltage present across the avalanche diode is coupled to the base electrode 142b. A second current output terminal 145 coupled to a collector electrode 142c on transistor 142 supplies the output current.

The above-described current sampling circuit operates in the following manner. Current in transistor 102 is held relatively constant, since a direct reference voltage is applied to its base, and further, since the feedback path to variable conduction stage 106 operates to oppose any tendency for emitter current flowing in transistor 102 to increase or decrease. If current flowing in transistor 102 tends to increase, current flowing through collector resistor 108 will produce a larger voltage drop across this resistor and therefore, the voltage at collector terminal 102c will tend to decrease. This voltage change is coupled by device 112 to the base terminal 106b of transistor 106 and is of a polarity to tend to reduce the conduction of the transistor 106.

Thus, transistor 102 will experience an effectively increased emitter resistance and its collector current will therefore tend to reduce to its fixed current level. If current in transistor 102 decreases, the opposite effect takes place, that is, a positive going signal is coupled to base terminal 106b of transistor 106 which increases conduction of this transistor and therefore reduces the effective emitter load resistance on transistor 102 thus tending to return the current flowing in transistor 102 to a constant level.

Defining signal input current as positive

when flowing in the direction illustrated by the arrows accompanying the symbol I_1 in FIGURE 1, emitter current in transistor 102 as positive when flowing as illustrated by the arrows accompanying the symbol I_2 in the figure, and active load current as positive when flowing in the direction illustrated by the arrow accompanying the symbol I_3 in the figure, it is possible to write a nodal current equation at junction point 124 in the figure. Thus,

$$I_1 + I_2 = I_3.$$

But I_2 is held relatively constant as explained above, therefore, variations in current I_1 must be effected by corresponding variations in I_3 . When I_1 is positive and increasing, I_3 must increase also. This regulation action utilizing negative feedback between the stages 102, 106 accomplishes the desired low input impedance at input terminal 104 which enables the circuit to be incorporated in current sampling applications.

Output current is generated by a parallelly coupled output device such as transistor 120. In an integrated circuit embodiment, transistors 120 and 106 are adjacent integrated on a single monolithic chip and therefore, are thermally coupled. Since base terminals 106b and 120b are coupled electrically and thermally, the base-emitter junction current density will be the same if the resistances of resistors 116 of transistor 106 and 118 of transistor 120 are in the inverse ratio as their representative base-emitter areas.

Thus, collector current flowing in transistor 120 will be in phase with and related to current I_3 as the relative base-emitter areas. For example, if the base-emitter area of transistor 120 is approximately four (4) times that of transistor 106, and the base-emitter current densities are equal, output current supplied to terminal 122 will be of a magnitude four (4) times as great as collector current flowing in transistor 106. Likewise, varying the emitter resistors 116 and 118 can accomplish a variable magnitude relationship between the two currents. In the embodiment shown in FIGURE 1, the resistances are chosen to equalize the base-emitter voltage drops across transistors 106 and 120, although this may not be required in all applications. In some circuits, the emitter resistors may be omitted entirely.

Output current can be extracted from first output terminal 122, but it may be desirable to provide a second output stage 140 to restrict the collector voltage of transistor 120 at some direct reference voltage. This may be accomplished using an output circuit 140 as shown within the dashed lines. Such an arrangement provides improved current matching between

transistors 106 and 120 since their respective collector voltages are more nearly the same. With resistance 144 and avalanche diode 146 coupled from B+ to ground to provide a reference direct voltage to a base terminal 142b of transistor 142, the emitter voltage of transistor 142 and, therefore, the collector voltage of transistor 120 will be fixed at this reference voltage value less the base to emitter forward voltage drop across the base-emitter junction of transistor 142. The collector current flowing in transistor 142 is coupled to current output terminal 145 to supply the output current. The reference voltage applied to base terminal 142b of transistor 142 may be developed in any suitable manner; the embodiment shown is merely illustrative.

The negative feedback path from the collector terminal 102c of transistor 102 to the base terminal 120b of transistor 120 may include signal coupling and direct voltage translating means other than avalanche diode 112 shown. For example, addition diodes, transistors and capacitors can be employed to obtain the required signal coupling, direct voltage translation and temperature compensation.

An important feature of the present invention exists in that input terminal 104 can be supplied with the required direct voltage level to voltage match the present circuit to the preceding input stage. This is accomplished by selecting the reference voltage illustrated as V_{ref} in the figure approximately

to the level desired at terminal 104. This terminal coupled to the reference voltage by transistor 102 will be fixed to voltage V_{ref}

less the forward voltage drop across the base-emitter junction of transistor 102. In some applications, this voltage thus obtained at terminal 104 can be employed to bias a preceding stage. See, for example, our co-pending Application referred to above.

The current sampling circuit of FIGURE 1 can further be utilized to generate a negative impedance useful, for example, as a Q-multiplier. Input terminal 104 can be serially coupled to a resistor which is parallelly coupled to a resonant circuit. The current through this resistance which is in phase with the voltage across the reactive elements of the resonant circuit will thereby provide the input signal for sampler transistor 102. The resultant output current from terminal 122 or 145 of output circuits 120 or 140 respectively can be returned to the opposite end of the resonant circuit by means of a current inverter. The magnitude of this inverted current can be adjusted to compensate for resistive losses in the resonant circuit thereby raising the Q of the system.

The present invention may further be uti-

lized as an amplifier and/or matrixing circuit. Such an embodiment is illustrated in FIGURE 2.

In FIGURE 2 as well as in the remaining FIGURES, those circuit elements performing the same or similar functions will be numbered so that their last two digits are the same while the first digit will correspond to the FIGURE number in which the circuit element appears.

Added are input resistances 228 and 229 and input terminals 226 and 227 which couple input signals to the circuit. Also a signal voltage can be applied to terminal 210 at the base of transistor 202 as is illustrated in FIGURE 2 by the symbol V_s . The collector resistor 230 of transistor 220 is responsive to collector current variations to develop an output voltage which can be extracted at terminal 222. The operation of the circuit with respect to inputs applied to terminals 226, 227 and 204 is essentially the same as the circuit of FIGURE 1.

The input current I_i comprises the sum of currents developed by an input voltage V_i applied to terminal 226 by an input voltage V_s applied to terminal 227, and current I_a applied to terminal 204. It is noted that the circuit may employ only one input terminal and corresponding resistance or it may employ several. The relative input impedance values can be varied for different matrixing effects. Further, current inputs can also be applied simultaneously to input terminal 204 as illustrated by the symbol I_a and associated arrow. The inherent low input impedance of the circuit allows matrixing of these various inputs with minimal interaction effects.

The operation of the constant current transistor 202, the variable conduction stage 206 and the output stage 220 is the same as corresponding stages 102, 106 and 120 in FIGURE 1, and the above description applies. It may be noted, however, that the voltage applied to the base terminal 202b of transistor 202 could comprise a signal voltage in addition to a bias supply for transistor 202. When a signal voltage is applied to base terminal 202b, it combines with the aforementioned input voltages. The base to emitter voltage of a transistor usually varies nonlinearly with changes in collector current. Therefore, a signal applied to a base terminal will appear distorted at the emitter terminal.

By maintaining the collector current of transistor 202 constant, its forward base-to-emitter voltage is held constant. Thus, the voltage present at terminal 202e as a result of the application of signal V_s is undistorted. As the input voltage V_s increases in a positive direction tending to increase current flowing in the collector terminal 202c of transistor 202, an increase in the voltage drop across collector resistor 208 will provide a decreasing signal

140 voltage to the base terminals 206b and 220b of transistors 206 and 220, respectively, via coupling means 212. This decreasing signal on these bases will reduce the collector currents flowing in transistors 206 and 220 to tend to maintain the collector current in transistor 202 constant. The decrease in collector current will reduce the voltage drop across collector impedance 230 associated with transistor 220 and therefore produce an output

voltage at terminal 222 which is in phase with applied voltage V_s .

It is noted that as input voltage V_1 or V_2 increase in a positive direction, a phase reversal takes place with respect to the output voltage at terminal 222 as is true when current input such as I_4 is applied.

The following equation illustrates the signal voltage relationships of FIGURE 2, assuming $R_{216} = R_{218} = 0$

$$V_{222} \cong \left[\frac{V_s}{R_{228} \parallel R_{220}} - \frac{V_1}{R_{228}} - \frac{V_2}{R_{229}} - I_4 \right] R_{230} \frac{A_{220}}{A_{206}}$$

where

$$\frac{A_{220}}{A_{206}}$$

25 is the ratio of the base-emitter junction area of transistors 220 and 206 and the current densities in these junctions are equal. The denominator of the V_s term is the resistance of the combination of parallel resistors 228 and 229.

30 Although the preferred embodiment of the present invention is integrated on a monolithic integrated circuit chip, the circuit may be constructed utilizing discrete components. Further, a variety of input and output means may be employed, the use of resistances in the figures is merely illustrative. The output circuit 140 of FIGURE 1 may also be employed in the circuit of FIGURE 2.

40 Referring to FIGURE 3, a differential amplifier capable of providing balanced push-pull output signals which are linearly related to one or more input signals is shown. The illustrated differential amplifier is particularly adapted for construction on an integrated circuit chip 300 indicated by the dashed outline. Input terminals T_1 and T_2 are provided on chip 300 and are adapted for connection to push-pull signal sources. Output terminals T_3 and T_4 are also provided on chip 300 and are adapted for coupling linearly amplified replicas of the push-pull input signals to appropriate utilization means (not shown). In addition, main (B+) supply terminals T_5 and T_6 , adapted for connection to, for example, plus ten volts and a reference (ground) potential, are provided on chip 300.

60 Each half of the differential amplifier configuration may be characterized as comprising an emitter follower transistor 302, 303, a shunt regulator transistor 306, 307 and an output transistor 320, 321. Referring to transistors 302, 306 and 320, input signals and bias are coupled via terminal T_1 to the base electrode of emitter follower transistor 302. The direct voltage supply (+10V) is coupled via terminal T_5 and a feedback resistor 308 to the collector electrode of follower transistor

302. The emitter electrode of follower transistor 302 is direct coupled to an emitter load comprising the parallel combination of the main conduction (collector-emitter) path of regulator transistor 306 and a load resistor 328 which is returned to ground via the collector-emitter path of regulator transistor 307.

75 The emitter of regulator transistor 306 is coupled directly to ground. An emitter degeneration resistor (not shown) may be provided if desired. Direct coupled negative feedback is provided from the collector electrode of follower transistor 302 to the base electrode of regulator transistor 306 by means of a direct voltage translation network comprising a feedback transistor 332, an avalanche diode 312 and a resistor 314. Resistor 314 is coupled between the base of regulator transistor 306 and ground. The collector electrode of feedback transistor 332 is coupled to the B+ supply terminal T_5 . The base electrode of transistor 332 is connected to the collector electrode of follower transistor 302 while the emitter electrode of transistor 332 is coupled via direct voltage translating avalanche diode 312 to the base electrode of regulator transistor 306.

95 Output signals are developed across an output load resistor 330 coupled between the B+ supply terminal T_5 and the collector electrode of output transistor 320. The input (base-emitter) circuit of output transistor 320 is connected in parallel with the base-emitter circuit of regulator transistor 306 and is similar to that of transistor 306 (i.e., if an emitter degeneration resistor is coupled to transistor 306, transistor 320 also would include an emitter degeneration resistor proportionally related to the resistor of transistor 306).

110 Transistor 306 and 320 are constructed so as to provide equal output current densities for equal input signals. Such a relationship is particularly realizable where transistors 306

and 320 are fabricated simultaneously in close proximity on a single integrated circuit chip. In that case, the output current densities produced by transistors 306 and 320 for a given input signal are related in the same proportion as the relative base-emitter areas of transistors 306 and 320. For equal areas, the currents of transistors 306 and 320 will be equal.

The second half of the differential amplifier is substantially identical to the first half described above. A feedback resistor 309 is coupled between B+ terminal T_3 and the collector of transistor 303. A feedback transistor 333, a voltage translating avalanche diode 313 and a base resistor 315 are coupled between the collector of follower transistor 303 and the base of regulator transistor 307. The input of output transistor 321 is coupled in parallel with the input of regulator transistor 307. A collector output load resistor 331 is associated with output transistor 321.

Bias voltage and input signals 180° out of phase with respect to those supplied to terminal T_1 are coupled via terminal T_2 to the base of follower transistor 303. Transistors 321 and 307 are related in the same manner as transistors 320 and 306. The emitter electrode of follower transistor 303 is direct coupled to the end of resistor 328 remote from the emitter of transistor 302.

The biasing voltage supplied to terminals T_1 and T_2 may, for example, be provided from a preceding amplifier or from a separate bias supply and typically would be of the order of +5 volts for the illustrated configuration.

The above described differential amplifier operated in the following manner. Under no signal conditions, equal bias voltages are provided to the base electrodes of input transistors 302 and 303. Substantially equal quiescent collector currents are produced in transistors 302 and 303 determined by the circuit parameters. The respective collector currents also flow in the collector-emitter circuits of the associated regulator transistors 306 and 307 such that substantially no quiescent current flows between the two halves of the amplifier through resistor 328.

Push-pull input signals which are to be amplified are applied via terminals T_1 and T_2 . Considering the half of the amplifier comprising transistors 302, 306, 320 and 332, positive- and negative-going input signals tend to increase and decrease conduction of input transistor 302. Changes in the collector current of transistor 302 are sensed by means of feedback resistor 308 and corresponding decreases and increases of collector voltage of transistor 302 appear at the base electrode of feedback transistor 332. A voltage translation to a lower level is accomplished by means of the base-emitter junction of

transistor 332 (e.g., 0.7 volt drop) and avalanche diode 312 (e.g., 5.6 volt drop).

The feedback arrangement causes conduction of regulator transistor 306 to decrease and increase, respectively, while the current in resistor 328 varies in an opposite sense. The total current supplied by input transistor 302 is therefore maintained substantially constant. Furthermore, the voltage of the emitter of transistor 302 substantially follows the input voltage variations at the base of transistor 302. The input circuit of output transistor 320 is connected in parallel with that of transistor 306 such that variations in collector current in transistor 306 are directly reflected in the collector current of transistor 320. Output voltage variations which are linearly related to input voltage variations supplied to terminal T_1 are produced across load resistor 330.

At the same time, a portion of the input voltage variations which appear at the emitter of input transistor 302 is also coupled to the emitter of input transistor 303. The collector current of transistor 303 therefore tends to vary in an opposite sense from the collector current of transistor 302. The feedback arrangement comprising resistor 309, transistor 333, avalanche diode 313 and resistor 315 serves to cause the collector current of regulator transistor 307 to vary so as to maintain the collector current of input transistor 303 substantially constant. Output voltage variations of opposite phase with respect to those produced across resistor 330 are produced across the load resistor 331 as the collector current of output transistor 321 follows the variations in the collector current of regulator transistor 307.

In the above-described operation of the circuit, the current in the resistor 328 is proportional to the voltage difference between the bases of input transistors 302 and 303. Signal induced changes in the currents of transistor 306 and 307 are equal and opposite to each other while corresponding changes in the currents of transistors 307 and 321 are equal and opposite to each other and opposite to the first-mentioned current changes. Thus, where the two halves of the differential amplifier arrangement are substantially the same and transistors 302, 303, 306, 307, 320 and 321 are substantially the same (as is readily realized with integrated circuit techniques), input signals supplied to terminal T_1 are linearly amplified and produce in opposite phases (i.e., push-pull relation) at the output terminals T_3 and T_4 .

In a similar manner, input signals supplied to terminal T_2 are reproduced in amplified push-pull fashion at terminals T_3 and T_4 . Output signals appearing at terminal T_3 are in phase with inputs supplied to terminal T_1 and 180° out of phase with inputs supplied to terminal T_2 . Output signals

appearing at terminal T_4 are in phase with inputs supplied to terminal T_2 and 180° out of phase with inputs supplied to terminal T_1 . It is possible, in different applications of the invention, to eliminate one or the other of the input terminals and/or one or the other of the output terminals. Furthermore, where one output only is desired, one output transistor and output load resistor (e.g., transistor 321 and resistor 331) may be eliminated.

It may also be desirable in certain applications to replace the load resistors by further transistors coupled in cascode relation to the output transistors.

The above-described differential amplifier arrangement provides a voltage gain determined substantially by the ratio between the resistance of an output load resistor (e.g. resistor 330) and the resistance of the resistor 328. Since resistance ratios may be controlled quite accurately on integrated circuits (e.g. $\pm 1\%$) the gain of the amplifier is readily controlled and is also quite stable. The above-described configuration also provides (as noted above) linear reproduction of input signals over substantially the entire range from saturation to cutoff of regulator transistors 306 and 307. This linearity characteristic may be demonstrated by the following explanation.

The feedback arrangements associated with input transistors 302 and 303 tend to maintain collector current of those transistors substantially constant. There is, therefore, substantially no variation of the base-emitter voltages of transistors 302 and 303. Since the voltages at the emitters of transistors 302 and 303 follow the voltages at their respective bases without V_{BE} modulation as signal varies, the voltage across resistor 328 also follows the signal without V_{BE} variation. The current variation in resistor 328 (a linear device) which results from a given input signal variation is reflected in equal current changes in regulator transistors 306 and 307 (the currents in transistors 306 and 307 vary oppositely for a given input signal). The output currents produced by transistors 320 and 321 are linearly proportional to (or in the case explained above, equal to) the currents in transistors 306 and 307. Output load resistors 330 and 331 are also linear devices. Therefore, the output voltage variations across resistors 330 and 331 are linearly related to input voltage variations.

Transistors 306, 307, 320, 321 may be driven from saturation to cutoff without disturbing the linear relationships set forth above. Therefore, the output voltages produced at terminals T_3 and T_4 may vary from $B+$ (10 volts in the illustrated case) to the saturation voltage of transistors 320, 321 (i.e. of the order of 0.1 volts), or a range substantially equal to the entire supply voltage associated with the amplifier.

It should also be noted that since the collector currents of input transistors 302 and 303 are maintained substantially constant, the input impedance of the amplifier is relatively high (i.e., at terminals T_1 and T_2).

Referring to FIGURE 4 of the drawing, an alternate embodiment of the invention is shown.

In the embodiment shown in FIGURE 4, equal emitter degeneration resistors 416, 417, 418 and 419 are associated with each of transistors 406, 407, 420 and 421, respectively. Bias coupling resistors 434 and 435 are associated with input transistors 402 and 403. Bias voltages may be supplied from means external to integrated circuit chip 400 via terminals T_7 and T_8 . A suitable bias supply arranged to provide a direct voltage of five volts (i.e., one-half the $B+$ voltage) may be provided by a circuit of the type described in our United States Patent No. 3,383,612. Input signals are supplied via capacitors 436 and 437 and terminals T_1 and T_2 to the bases of transistors 402 and 403, respectively.

In FIGURE 4, the emitters of input transistors 402 and 403 are coupled directly together. While the permissible input signal voltage range for linear operation of such a configuration is lower than where a resistor is coupled between the emitters of the input transistors, the available voltage gain is higher in the case of the FIGURE 4 arrangement. Specifically, in the illustrated case, the signal voltage gain is equal substantially to the ratio of the resistance of one of load resistors 430 or 431 to twice the impedance looking into the junction between the emitter of transistor 402 and the collector of transistor 406 (or 403 and 407 which is the same). A circuit constructed utilizing the circuit values shown in FIGURE 4 and transistors having a current gain (β) of the order of 30 to 50 provided a voltage gain of 300 with a maximum input signal voltage of 50 millivolts peak to peak.

Additional modifications may also be made to the circuit. For example, the feedback circuits may employ other direct voltage translating or blocking schemes. The transistors 432 and 433 may be omitted if desired. Furthermore, additional voltage gain may be provided by placing additional transistors in the output circuits with their electrodes coupled to corresponding electrodes with their electrodes of transistors 420 and 421 (i.e., parallel output transistors may be provided).

In the appended claims a plurality of terminals are recited and the functions performed thereby are indicated. It is to be understood that where a single terminal may perform a multiple function (for example the terminal T_6 in Figure 3 is both a supply terminal and one of two terminals (T_3 , T_6) by which an input signal can be applied in effect

between base and emitter of transistor 302) the use of such a single terminal rather than separate terminals for the several functions is to be understood as being within the scope of the claims.

WHAT WE CLAIM IS:—

1. Electronic apparatus comprising a signal translating stage incorporating a plurality of three-terminal power gain devices each having input, output and common electrodes, wherein the input and common electrodes of a first of said devices are coupled to first and second terminals for application of input signals between these two electrodes, the common electrode of said first power gain device is DC coupled to the output electrode of a second of said power gain devices, the output electrode of said first power gain device is DC coupled through first impedance means to a third terminal, the input electrodes of the second and a third of said power gain devices are coupled in like manner as each other to the output electrode of said first power gain device, the common electrodes of said second and third power gain devices are each DC coupled to a fourth terminal, said third and fourth terminals being operating potential supply terminals for the stage with the input electrodes of said power gain devices arranged for DC biasing thereof with respect to said fourth terminal, and the output electrode of the third device having an output connection therefrom for the stage.

2. Electronic apparatus as claimed in claim 1 together with utilizing means a direct current path through which is DC coupled between the output electrode of said third power gain device and said third terminal.

3. Electronic apparatus according to claim 1 or 2 including for said first device a direct current load impedance coupled between its said common electrode and said fourth terminal and shunted by said second device.

4. Electronic apparatus as claimed in Claim 1 or 2 wherein a second impedance means DC couples the output electrode of a fourth such power gain device to said third terminal, the output and common electrodes of a fifth such power gain device are respectively DC coupled to the common electrode of said fourth power gain device and to said fourth terminal, the input electrode of said fifth power gain device is coupled to the output electrode of said fourth power gain device, the input electrodes of said fourth and fifth power gain devices have connections permitting DC biasing thereof with respect to said source of operating potential, the common electrodes of said first and fourth power gain devices are coupled to each other, and a further terminal is provided for application of input signals to the input electrode of said fourth power gain device, with said first terminal providing for the application of input

signals to the input electrode of the first device.

5. Electronic apparatus as claimed in Claim 4 having also a sixth such power gain device whose input electrode is coupled to the output electrode of the fourth power gain device in like manner as the input electrode of said fifth power gain device, and from whose output electrode there is a second output connection.

6. Electronic apparatus as claimed in claim 5 together with utilizing means having a direct current path therethrough DC coupled between the output electrode of said sixth power gain device and said third terminal.

7. Electronic apparatus as claimed in claim 4, 5 or 6 wherein, with the input electrodes of said first and fourth power gain devices so arranged as to be biased at the same quiescent potential, the coupling of their said common electrodes to each other has a direct current path therethrough.

8. Electronic apparatus as claimed in any preceding claim, wherein said power gain devices which have their common electrodes DC coupled to said fourth terminal are similar devices having their common electrode so coupled by similarly-valued resistors.

9. Electronic apparatus as claimed in any of claims 1—7 wherein said power gain devices which have their common electrodes DC coupled to said fourth terminal are so coupled by direct connection.

10. Electronic apparatus as claimed in any preceding claim, wherein (each of) said impedance means comprises a resistor, an avalanche diode is included in (each) said coupling from the output electrode of one power gain device to the input electrode of another, a single avalanche diode being used in common for input electrodes coupled to the same output electrode, and a resistor coupled to said fourth terminal the end of (each) said avalanche diode remote from the end connecting with said output electrode, whereby also DC bias for the input electrode (s) recited in this claim is provided.

11. Electronic apparatus as claimed in any of Claims 1—9 wherein, with said power gain devices constituted by transistors, each of said impedance means comprises a resistor and each of said couplings from the output electrode of one power gain device to the input electrode of another (a common coupling being used for input electrodes coupled to the same output electrode) comprises a transistor in an emitter follower configuration in cascade with an avalanche diode having current drawings means coupled thereto to maintain it in avalanche conduction, whereby also DC bias for the input electrode(s) recited in this claim is provided.

12. Electronic apparatus as claimed in any preceding claim, wherein each of said power gain devices is a transistor having a base elec-

between base and emitter of transistor 302) the use of such a single terminal rather than separate terminals for the several functions is to be understood as being within the scope of the claims.

WHAT WE CLAIM IS:—

1. Electronic apparatus comprising a signal translating stage incorporating a plurality of three-terminal power gain devices each having input, output and common electrodes, wherein the input and common electrodes of a first of said devices are coupled to first and second terminals for application of input signals between these two electrodes, the common electrode of said first power gain device is DC coupled to the output electrode of a second of said power gain devices, the output electrode of said first power gain device is DC coupled through first impedance means to a third terminal, the input electrodes of the second and a third of said power gain devices are coupled in like manner as each other to the output electrode of said first power gain device, the common electrodes of said second and third power gain devices are each DC coupled to a fourth terminal, said third and fourth terminals being operating potential supply terminals for the stage with the input electrodes of said power gain devices arranged for DC biasing thereof with respect to said fourth terminal, and the output electrode of the third device having an output connection therefrom for the stage.

2. Electronic apparatus as claimed in claim 1 together with utilizing means a direct current path through which is DC coupled between the output electrode of said third power gain device and said third terminal.

3. Electronic apparatus according to claim 1 or 2 including for said first device a direct current load impedance coupled between its said common electrode and said fourth terminal and shunted by said second device.

4. Electronic apparatus as claimed in Claim 1 or 2 wherein a second impedance means DC couples the output electrode of a fourth such power gain device to said third terminal, the output and common electrodes of a fifth such power gain device are respectively DC coupled to the common electrode of said fourth power gain device and to said fourth terminal, the input electrode of said fifth power gain device is coupled to the output electrode of said fourth power gain device, the input electrodes of said fourth and fifth power gain devices have connections permitting DC biasing thereof with respect to said source of operating potential, the common electrodes of said first and fourth power gain devices are coupled to each other, and a further terminal is provided for application of input signals to the input electrode of said fourth power gain device, with said first terminal providing for the application of input

signals to the input electrode of the first device.

5. Electronic apparatus as claimed in Claim 4 having also a sixth such power gain device whose input electrode is coupled to the output electrode of the fourth power gain device in like manner as the input electrode of said fifth power gain device, and from whose output electrode there is a second output connection.

6. Electronic apparatus as claimed in claim 5 together with utilizing means having a direct current path therethrough DC coupled between the output electrode of said sixth power gain device and said third terminal.

7. Electronic apparatus as claimed in claim 4, 5 or 6 wherein, with the input electrodes of said first and fourth power gain devices so arranged as to be biased at the same quiescent potential, the coupling of their said common electrodes to each other has a direct current path therethrough.

8. Electronic apparatus as claimed in any preceding claim, wherein said power gain devices which have their common electrodes DC coupled to said fourth terminal are similar devices having their common electrode so coupled by similarly-valued resistors.

9. Electronic apparatus as claimed in any of claims 1—7 wherein said power gain devices which have their common electrodes DC coupled to said fourth terminal are so coupled by direct connection.

10. Electronic apparatus as claimed in any preceding claim, wherein (each of) said impedance means comprises a resistor, an avalanche diode is included in (each) said coupling from the output electrode of one power gain device to the input electrode of another, a single avalanche diode being used in common for input electrodes coupled to the same output electrode, and a resistor coupled to said fourth terminal the end of (each) said avalanche diode remote from the end connecting with said output electrode, whereby also DC bias for the input electrode (s) recited in this claim is provided.

11. Electronic apparatus as claimed in any of Claims 1—9 wherein, with said power gain devices constituted by transistors, each of said impedance means comprises a resistor and each of said couplings from the output electrode of one power gain device to the input electrode of another (a common coupling being used for input electrodes coupled to the same output electrode) comprises a transistor in an emitter follower configuration in cascade with an avalanche diode having current drawings means coupled thereto to maintain it in avalanche conduction, whereby also DC bias for the input electrode(s) recited in this claim is provided.

12. Electronic apparatus as claimed in any preceding claim, wherein each of said power gain devices is a transistor having a base elec-



trode as an input electrode, a collector electrode as an output electrode and an emitter electrode as a common electrode.

- 5 13. A differential amplifier comprising first and second input transistors respectively associated with first and second regulator transistors, each input transistor being arranged substantially as an emitter follower having its emitter direct coupled to the collector of the associated regulator transistor with the latter forming part of the emitter load for the input transistor, DC coupling between the emitter of the input transistors, separate resistors coupled to the collector of the input transistors for supplying operating potential thereto, direct current negative feedback connections from the collectors of the input transistors to the bases of their associated regulator transistors respectively, such as to maintain substantially constant current in the input transistors, means for applying input signals between the base and emitter of at least one of the input transistors, and output means including an impedance coupled to an output transistor the base-emitter circuit of which is coupled in parallel with the base-emitter circuit of one of the regulator transistors.

14. A differential amplifier according to claim 13 wherein the input transistor emitters are coupled by a resistance.

15. A signal translating stage comprising a first transistor with means for applying potential variations to its base electrode and having

its emitter electrode coupled to a resistive load, a second, regulating, transistor having its collector electrode coupled to the emitter electrode of the first transistor and being arranged to maintain substantially constant current flow through the collector-emitter path of the first transistor, and a third transistor connected to have the same base-to-emitter signal variation as the second transistor and exhibiting characteristics similar to those of the second transistor whereby the collector current of the third transistor will vary similarly to that in the second transistor and thereby in dependence on input signal variation.

16. Electronic apparatus comprising a signal translating stage or stages substantially as hereinbefore described with reference to any Figure of the accompanying drawings.

17. Electronic apparatus as claimed in any preceding claim, wherein all of the power gain devices are constructed within the confines of a monolithic semiconductor body (said devices being of a nature susceptible to being so constructed) together with each of such resistor and avalanche diode components as may also be comprised in the stage or stages.

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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1973.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

