

PATENT SPECIFICATION

(11) 1358 388

1358388

- (21) Application No. 48004/73 (22) Filed 20 July 1971
 (62) Divided out of No. 1358387
 (31) Convention Application No. 56610 (32) Filed 20 July 1970 in
 (33) United States of America (US)
 (44) Complete Specification published 3 July 1974
 (51) International Classification H01G 3/075
 (52) Index at acceptance

H1M 1B2A 1B2B3 1B2BX 1B2C14 1B2C1 1B2C7 1G9A
 1G9B 1J2 1K 1P12 1P13 1P15 1P2 1P5 1P6



(54) IMPROVEMENTS IN OR RELATING TO CIRCUITS HAVING THIN-FILM CAPACITORS

(71) We, HEWLETT-PACKARD COMPANY of 1501 Page Mill Road, Palo Alto, California, United States of America, a corporation organised and existing under the laws of the state of California, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention is concerned with improvements in or relating to circuits having thin-film capacitors, and is related to the invention disclosed in our copending patent application no. 34027/71.

The fabrication of electronic circuitry wherein resistors and capacitors and their interconnections are formed by thin-film techniques is growing rapidly in importance. With thin-film technology, complex circuits having precision capacitors and resistors may be tailored to meet specific circuit design requirements, resulting in microcircuitry of reduced size, weight, and cost and increased reliability. One form of thin-film circuit, along with the method of manufacture, is disclosed in United States Patent No. 3,616,282 issued on October 26, 1971 to George E. Bodway, entitled Method of Producing Thin-Film Circuit Elements.

One typical process for the manufacture of thin-film resistor-capacitor circuits of the type shown in U.S. Patent No. 3,616,282 comprises the following steps, performed sequentially:

1. Forming the under-electrodes of the various capacitors on an insulating substrate by
 - a) sputtering a layer of conductive metal such as tantalum (Ta) over the surface of the substrate,
 - b) forming a mask on the metal layer by a known photo-resist technique, and
 - c) etching through the mask to remove all the metal except for the desired capacitor under-electrodes and inter-

connections therebetween that serve to provide a single common electrical path for all the capacitor under-electrodes during a subsequent anodizing step;

2. Forming a dielectric layer over a portion of the surface of each of the capacitor under-electrodes by

- a) depositing an oxide layer over the entire surface of the substrate, capacitor under-electrodes, and interconnections, such as for example, by a silicon dioxide (SiO₂) deposition,
- b) forming a mask on the oxide layer by the photo-resist technique,
- c) etching through the mask to remove the oxide layer from areas of the capacitor under-electrodes to be anodized,
- d) electrochemically anodizing the exposed portions of the capacitor under-electrodes in an appropriate electrolyte for an appropriate period of time to form the desired dielectric layer (for example, Ta₂O₅) of each capacitor under-electrode, and
- e) removing the anodizing mask by an oxide etch, leaving the partially anodized under-electrodes and the interconnections therebetween;

3. Removing the interconnections between the capacitor under-electrodes by

- a) forming a mask by the photoresist technique leaving the interconnections exposed, and
- b) etching away the interconnections;

4. Forming the various resistors on the substrate by

- a) sputtering a layer of resistive material such as tantalum nitride (Ta₃N) over

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- the entire surface of the substrate and capacitor electrodes,
- b) depositing a first layer of conductive material such as chrome gold (CrAu), which adheres well to the resistive layer, over the resistive layer,
 - c) forming a mask, which covers those areas of the structure where the resistors are to remain, by the photo-resist technique and
 - d) etching away the exposed first conductive layer and the underlying resistive layer, leaving the desired resistors;
5. In order to increase the yield of these circuits, depositing an additional oxide layer on the dielectric (Ta_2O_5) layer of each capacitor under-electrode to cure pinholes therein and other imperfections produced therein during the various fabrication steps performed after the anodizing step, such as during the oxide etching step of 2(e) above and the resistive layer sputtering step of (a) above (this step is performed, for example, by depositing a layer of silicon dioxide (SiO_2) over the structure with a value of $.055 \text{ pf/mil}^2 \pm 5\%$ for the combined Ta_2O_5 and SiO_2 layers).
6. Forming the upper-electrodes of the various capacitors by
- a) depositing a second layer of conductive material such as chrome gold (CrAu) over the entire surface of the structure,
 - b) forming a mask which covers those areas of the structure where the capacitor upper-electrodes and the underlying additional oxide layer are to remain by the photoresist technique, and
 - c) etching away the exposed second conductive layer and then the underlying additional oxide layer, leaving the desired capacitor upper-electrodes;
7. Complete the upper-electrodes of the various capacitors and forming the interconnections between the various capacitors and resistors by
- a) depositing a third layer of conductive material such as chrome gold (CrAu) over the entire surface of the structure,
 - b) forming a mask on the third conductive layer by the photo-resist technique to define the capacitor upper-electrodes and interconnections,
 - c) plating a thick layer (.30—.40 mils) of gold to form the interconnections, and
 - d) etching away the second and then the third conductive layers where not

covered by the thick gold interconnections.

It is noted that, in the above process, certain difficult steps are performed. For example, the masking and anodizing steps of 2(b), (c), and (d) above are troublesome since, during anodizing, the mask has to withstand 200 volts in an electrolytic bath, and the mask oftentimes breaks down.

Other difficult steps in the process are the interconnection masking and etching steps of 3(a) and (b) above. Still other difficult steps in the process are the masking and etching steps of 6(b) and (c), particularly since the mask formed must be pinhole free to prevent pinholes from being etched in the capacitor dielectric layers. The etching step of 6(c) requires the use of a silicon dioxide in forming the additional oxide layer, since it is difficult or impossible to etch other forms of oxide layers, and only silicon dioxide has been found to be satisfactory.

Since a photoresist mask alone is not capable of withstanding the oxide etch needed to form the capacitors in the etching step of 6(c), the layer of CrAu deposited during the step of 6(a) is needed to serve as a mask, and thus the two layers of CrAu deposited during the steps of 6(a) and 7(a) and the two subsequent CrAu etching steps of 6(c) and 7(d) are needed.

Also, where silicon oxide layers are selectively etched and remaining portions thereof are subsequently gold plated through a masking, there is a tendency for an undesirable gold bead to form around the upper edges of the masked portions of the oxide layers, the mask being unable to adequately protect these edges.

Because of the high temperatures involved in the SiO_2 deposition step of 5 above; it is necessary that the first layer of CrAu deposited in the step of 4(b) above be fairly thick, so as not to be deleteriously affected by diffusion of chrome therefrom due to the heat. Consequently the etching step of 4(d) above is lengthened resulting in less than optimum resistor definition.

The above process requires seven masking steps, and the trips between the photoresist masking stages and the subsequent deposition and etching stages result in an overall fabrication period of approximately three weeks.

It is an object of the present invention to provide an improved thin film capacitor.

It is another object of the present invention to provide an improved method of manufacturing a thin film multicapacitor structure.

The present invention provides a thin film capacitor comprising a substrate of insulating material; a metallic film element on a surface of the substrate, the metallic film element having an oxidized upper surface; a dielectric layer extending entirely over the oxidized

upper surface of the metallic film element and the substrate; and a pair of spaced-apart conductors on the dielectric layer over the metallic film element forming two capacitor plates of a capacitor defined between the metallic film element and the two spaced-apart conductors.

Preferably the oxidized upper surface of the metallic film element is an anodized layer of the metallic film element.

Preferably the metallic film element is made of tantalum and has a tantalum pentoxide upper surface.

Preferably the dielectric layer is made of a material comprising an oxide of silicon; more preferably the oxide of silicon is silicon dioxide.

The present invention also provides a method of manufacturing a thin film multicapacitor structure, the method comprising the steps of forming a plurality of metallic film elements on a surface of an insulating substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer entirely over the surface of the substrate and the oxidized upper surfaces of the metallic film elements, and forming at least one pair of spaced-apart conductors on the dielectric layer over each metallic film element, each pair of spaced-apart conductors forming two plates of a capacitor defined between those conductors and a metallic film element.

Preferably the step of forming an oxidized upper surface on each of the metallic film elements comprises anodizing the upper surface of each of the metallic film elements.

Preferably the step of forming the metallic film elements comprises depositing a layer of tantalum on the surface of the substrate and selectively etching the layer of tantalum to form the metallic film elements, and the step of forming the oxidized upper surface on each of the metallic film elements comprises anodizing the upper surface of each of the tantalum metallic film elements.

Preferably the step of forming the dielectric layer comprises depositing a silicon dioxide layer on the oxidized upper surfaces of the metallic film elements and on the surface of the substrate.

There now follows a detailed description which is to be read with reference to the accompanying drawings of a thin film capacitor and a method of manufacturing a thin film multicapacitor structure according to the invention; it is to be clearly understood that these have been selected to illustrate the invention by way of example and not by way of limitation.

In the drawings:

Figure 1 is a schematic diagram of a thin film resistor and capacitor structure, the capacitor structure being made in accordance with the preferred embodiment of the present invention.

Figure 2 is a top view of the thin film struc-

ture of Figure 1 in an early stage of its fabrication.

Figure 3 is a cross-sectional side view of the thin film structure of Figure 2 taken along section line 3—3 therein.

Figure 4 is a top view of the thin film structure of Figure 1 in an advanced stage of its fabrication.

Figure 5 is a cross-sectional side view of the thin film structure of Figure 4 taken along section line 5—5 therein.

Figure 6 is a similar cross-sectional side view of the thin film structure of Figure 4 in a still later stage of its fabrication.

In order to more clearly describe the present invention, the step-by-step construction of a simple amplifier circuit shown in Figure 1 will be described in detail. This simple circuit comprises a transistor T1 coupled to a thin film resistor-capacitor structure comprising three resistors R1, R2, and R3 and five capacitors C1 through C5.

Referring now to Figures 2 and 3, the main body or support for the structure comprises a substrate 11 of good insulating material, such as sapphire, glass or ceramic, and of a suitable size, such as 1/2 inch wide, 1 inch long, and 25 mils thick. After proper cleaning, the upper surface of the substrate is deposited with a layer of good electrical conducting material on which a dielectric oxide layer may be anodically formed. This layer is preferably beta tantalum or hafnium of suitable thickness, for example 7,000 to 9,000 Å. Other suitable materials include aluminum, niobium, titanium and zirconium. This layer may be deposited by a number of suitable processes including cathodic sputtering and vacuum deposition.

The metallic layer deposited on substrate 11 is masked by a known photoresist technique and then etched to produce a plurality of metallic electrodes 12—16 which are to serve as the under-electrodes of the capacitors C1 through C5, respectively. These electrodes may be formed by techniques other than the photoresist masking technique. For example, ion beam machining may be employed. At the time these electrodes are formed, interconnecting strips 17 and a common metallic pad 18 are also formed, the pad 18 and the interconnecting strips 17 forming a common electrical connection for the electrodes during the subsequent anodizing process.

A layer of good dielectric material is then formed on the entire surface area of each electrode by anodizing the metallic electrodes in an appropriate electrolyte, such as about 0.01% solution of citric acid at about 200 volts for one hour, resulting in the formation of an oxide layer 19 on the upper surface of each electrode. In the case of a tantalum electrode, a layer of tantalum pentoxide (Ta_2O_5) is formed, and in the case of a hafnium electrode, a layer of hafnium oxide (HfO_2) is

formed. This layer is of the order of several thousand Angstrom units thick. Once the anodizing has been completed, the pad 18 and the interconnecting strips 17 for the electrodes 12—16 may be eliminated from the structure by sawing the substrate 11 along the lines 21 shown in Figure 2. This sawing step may be postponed until after the structure has been completely fabricated, if desired.

10 An oxide layer 22 is then formed over the entire surface of the substrate 11 and the anodized electrodes 12—16. For example, silicon dioxide (SiO_2) may be sputtered onto the surface to a selected thickness (for example 15 2500 Å) to give the desired capacitance density. Silicon dioxide will give a capacitance density of .055 pf/mil². The thickness of the silicon dioxide layer may be accurately controlled within $\pm 2\%$, and, thus, the value of 20 the capacitors formed may be very accurately controlled. Since, in this invention, it is not necessary to etch the oxide layer 22 during subsequent steps in the process, many oxides can be selected, for example, Hafnium dioxide, 25 aluminum oxide, yttrium oxide and tantalum pentoxide, to give different dielectric constants and different capacitance densities ranging from .05 to .55 pf/mil²; silicon nitride is another example of a material suitable for 30 providing the layer 22. The oxide layer 22 will generally have a thickness in the range of 2000 Å to 10,000 Å. The oxide layer 22 is preferably formed by sputtering, but may be applied by other techniques, such as gaseous 35 deposition and electron beam deposition.

A layer 23 of good resistive material is then applied over the oxide layer 22, for example, an 800 Å thick layer of tantalum nitride (Ta_2N) applied by reactive sputtering. Other 40 resistive materials, such as Nichrome (RTM); hafnium nitride, and rhenium, may be selected for use, and may be applied by suitable techniques, including sputtering and evaporation. When a circuit having thin-film capacitors, but 45 no thin-film resistors, is to be made, layer 23 of resistive material may be omitted.

An electrically conducting metal layer 24, preferably of chrome gold (CrAu) is then 50 applied to the layer 23 of resistive material, or if it is omitted, to oxide layer 22, by any suitable technique, such as sputtering or evaporation. The metal layer 24 may also be formed of moly gold, nickel gold, or copper and may be formed to a suitable thickness (for 55 example, several thousand Å) giving about .1 ohms/square.

At this stage in the fabrication, a form of standard, general purpose predeposited substrate structure has been fabricated. In our 60 example, only five capacitor under-electrodes have been provided, but a much larger number are fabricated on the general purpose substrate, the electrodes being of various area sizes and ranging around the periphery of the sub- 65 strate.

The large central portion of the substrate is available for creating the various resistors and the circuit interconnections, as well as providing room for bonding transistors to the structure. Any desired ones of the various 70 capacitor under-electrodes may be used in the subsequent circuit fabrication.

These general purpose structures are given to circuit designers for their use in creating 75 innumerable circuits. Since the process apparatus necessary to perform the remaining steps in the fabrication of such circuits is generally available to circuit designers, custom design is greatly facilitated.

The next operation in the fabrication of the 80 illustrative structure of Figure 1 is to define the width of the resistor elements by a photo-resist masking and an etch of both the CrAu layer 24 and the Ta_2N resistive layer 23 down 85 to the surface of the SiO_2 layer 22 to form openings 25, 26, 27, and 28 (see Figures 4 and 5). Openings 25 and 26 define the width of resistor R1 therebetween; openings 27 and 28 define the width of resistor R3 there- 90 between; and openings 26 and 28 define the width of resistor R2 therebetween.

As a next stage of fabrication, the upper-electrodes of the capacitors, the desired inter-connections between the circuit and the external connection pads are then plated through 95 a suitable mask onto the CrAu layer 24. A conductive material, such as gold or copper, is used and deposited to a desired thickness (for example, 1/4 mil). As seen in Figure 4, con- 100 ductors 29, 30, 31, and 32 serve as external connectors for the capacitors C1, C3, C4, and C5, respectively; conductor 33 serves as the external connector for resistor R2; conductor 34 interconnects one side of capacitor C2 with 105 capacitor C1 and resistor R1; conductor 35 interconnects the other side of capacitor C2 with capacitor C3 and resistor R3; conductor 36 interconnects capacitor C4 and resistor R1; conductor 37 interconnects capacitor C5 and resistor R3; and conductor 38 serves as the 110 connector between resistor R2 and the transistor T1 to be thereafter bonded to the structure.

The value of each capacitor is established by the extent of the two regions sandwiched 115 directly between the two upper-electrodes and the under-electrode, for example, in the case of capacitor C1, the region directly between the under-electrode 12 and the two upper-electrodes 29 and 34. The overlaid area of upper- 120 electrode 13 of capacitor C2 is smaller than that for the other capacitors, and the capacitance of capacitor C2 is therefore substantially smaller than that of the other four capacitors. Each capacitor is formed, in effect, by two 125 capacitors connected in series. For example, capacitor C1 is formed by the capacitance between upper-electrode 29 and under-electrode 12 plus the capacitance between upper-electrode 34 and under-electrode 12. The elec- 130

trical connections to this capacitor are both made to the upper-electrodes 29 and 34, and no external connections are made with the under-electrode 12.

- 5 As a next stage of fabrication the CrAu layer 24 and then the resistive Ta₂N layer 23 are removed from all areas 39 between and around the various circuit elements by employing photoresist and etching techniques. There-
10 after, the layer 24 of CrAu is removed, by etching, from the areas 40, 41, and 42, leaving the layer of resistive material (Ta₂N) to form the resistors R1, R3, and R2, respectively, in these areas (see Figure 6).
15 After final test of the circuit, the transistor T may be bonded to the interconnect 35 so that the collector electrode is coupled to the junction of C2, C3, and R3. Electrical lead 43 is added to connect the base electrode to interconnect 34 between capacitors C1 and C2
20 and resistor R1 while electrical lead 44 is added to connect the emitter electrode with interconnect 38 to the resistor R2.

WHAT WE CLAIM IS:—

- 25 1. A thin film capacitor comprising a substrate of insulating material; a metallic film element on a surface of the substrate, the metallic film element having an oxidized upper surface; a dielectric layer extending entirely
30 over the oxidized upper surface of the metallic film element and the substrate; and a pair of spaced-apart conductors on the dielectric layer over the metallic film element forming two capacitor plates of a capacitor defined between
35 the metallic film element and the two spaced-apart conductors.
2. A thin film capacitor according to claim 1, wherein the oxidized upper surface of the metallic film element is an anodized layer of
40 the metallic film element.
3. A thin film capacitor according to either one of claims 1 and 2, wherein the metallic film element is made of tantalum and has a tantalum pentoxide upper surface.
45 4. A thin film capacitor according to any one of claims 1, 2, and 3, wherein the dielec-

tric layer is made of a material comprising an oxide of silicon.

5. A thin film capacitor according to claim 4 wherein the oxide of silicon is silicon di-
oxide. 50

6. A method of manufacturing a thin film multicapacitor structure, the method comprising the steps of forming a plurality of metallic film elements on a surface of an insulating substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer entirely over the surface of the substrate and the oxidized upper surfaces of the metallic film elements, and forming at least one pair of spaced-apart conductors on the dielectric layer over each metallic film element, each pair of spaced-apart conductors forming two plates of a capacitor defined between those conductors and a metallic film
65 element. 55

7. A method according to claim 6, wherein the step of forming an oxidized upper surface on each of the metallic film elements comprises anodizing the upper surface of each of the metallic film elements. 70

8. A method according to claim 6, wherein the step of forming the metallic film elements comprises depositing a layer of tantalum on the surface of the substrate and selectively etching the layer of tantalum to form the metallic film elements, and the step of forming the oxidized upper surface on each of the metallic film elements comprises anodizing the upper surface of each of the tantalum metallic film elements. 80

9. A method according to any one of claims 6, 7, and 8, wherein the step of forming the dielectric layer comprises depositing a silicon dioxide layer on the oxidized upper surfaces of the metallic film elements and on the surface of the substrate. 85

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trical connections to this capacitor are both made to the upper-electrodes 29 and 34, and no external connections are made with the under-electrode 12.

5 As a next stage of fabrication the CrAu layer 24 and then the resistive Ta_2N layer 23 are removed from all areas 39 between and around the various circuit elements by employing photoresist and etching techniques. There-
10 after, the layer 24 of CrAu is removed, by etching, from the areas 40, 41, and 42, leaving the layer of resistive material (Ta_2N) to form the resistors R1, R3, and R2, respectively, in these areas (see Figure 6).

15 After final test of the circuit, the transistor T may be bonded to the interconnect 35 so that the collector electrode is coupled to the junction of C2, C3, and R3. Electrical lead 43 is added to connect the base electrode to interconnect 34 between capacitors C1 and C2
20 and resistor R1 while electrical lead 44 is added to connect the emitter electrode with interconnect 38 to the resistor R2.

WHAT WE CLAIM IS:—

25 1. A thin film capacitor comprising a substrate of insulating material; a metallic film element on a surface of the substrate, the metallic film element having an oxidized upper surface; a dielectric layer extending entirely
30 over the oxidized upper surface of the metallic film element and the substrate; and a pair of spaced-apart conductors on the dielectric layer over the metallic film element forming two capacitor plates of a capacitor defined between
35 the metallic film element and the two spaced-apart conductors.

40 2. A thin film capacitor according to claim 1, wherein the oxidized upper surface of the metallic film element is an anodized layer of the metallic film element.

45 3. A thin film capacitor according to either one of claims 1 and 2, wherein the metallic film element is made of tantalum and has a tantalum pentoxide upper surface.

4. A thin film capacitor according to any one of claims 1, 2, and 3, wherein the dielec-

tric layer is made of a material comprising an oxide of silicon.

5. A thin film capacitor according to claim 4 wherein the oxide of silicon is silicon di- 50
oxide.

6. A method of manufacturing a thin film multicapacitor structure, the method comprising the steps of forming a plurality of metallic
55 film elements on a surface of an insulating substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer entirely over the surface of the substrate and the oxidized upper surfaces
60 of the metallic film elements, and forming at least one pair of spaced-apart conductors on the dielectric layer over each metallic film element, each pair of spaced-apart conductors
65 forming two plates of a capacitor defined between those conductors and a metallic film element.

7. A method according to claim 6, wherein the step of forming an oxidized upper surface on each of the metallic film elements comprises
70 anodizing the upper surface of each of the metallic film elements.

8. A method according to claim 6, wherein the step of forming the metallic film elements comprises depositing a layer of tantalum on
75 the surface of the substrate and selectively etching the layer of tantalum to form the metallic film elements, and the step of forming the oxidized upper surface on each of the metallic film elements comprises anodizing the
80 upper surface of each of the tantalum metallic film elements.

9. A method according to any one of claims 6, 7, and 8, wherein the step of forming the dielectric layer comprises depositing a silicon
85 dioxide layer on the oxidized upper surfaces of the metallic film elements and on the surface of the substrate.

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