

READING METHOD, RESPONDER, AND INTERROGATOR

ABSTRACT

The conventional technique in which transmission and reception of the identification number to/from an interrogator is repeated on one bit unit has problems that it requires a complicated command, a large number of operation stages, a complicated flip-flop, switching control between transmission and reception, control of a memory address counter, and a complicated logical circuit such as a data comparison circuit, which increases the chip size. The present invention provides an interrogator for reading a recognition number from a responder by radio and the responder. When a clock pulse is modulated on a high-frequency carrier and transmitted to the responder from the antenna of the interrogator, there are a first case when the clock pulse interval is short and a second case when the clock pulse interval is long. By combining the clock pulse of the first case and the clock pulse of the second case so as to control the read of the recognition number from the interrogator, it is possible to realize reduction of the semiconductor chip size of the responder and suppress the cost of the semiconductor chip.

FIGURE 10