(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 March 2006 (09.03.2006)

PCT

(10) International Publication Number
WO 2006/026699 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2005/031094

(22) International Filing Date: 26 August 2005 (26.08.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/934,778 2 September 2004 (02.09.2004) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

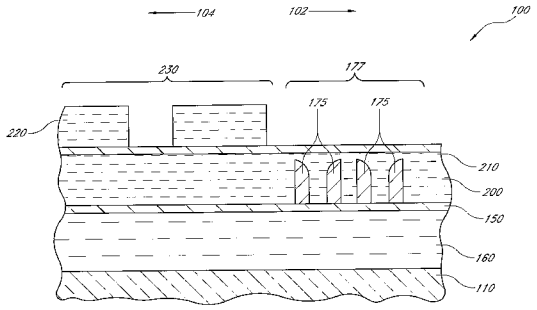
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** METHOD FOR INTEGRATED CIRCUIT FABRICATION USING PITCH MULTIPLICATION



(57) **Abstract:** Different sized features in the array 102 and in the periphery 104 of an integrated circuit 100 are patterned on a substrate 110 in a single step. In particular, a mixed pattern, combining two separately formed patterns 177, 230, is formed on a single mask layer 160 and then transferred to the underlying substrate 110. The first of the separately formed patterns, 177, is formed by pitch multiplication and the second of the separately formed patterns, 230, is formed by conventional photolithography. The first of the separately formed patterns, 177, includes features 175 that are below the resolution of the photolithographic process used to form the second of the separately formed patterns, 230. These lines are made by forming a pattern on photoresist and then etching that pattern into an amorphous carbon layer. Sidewall pacers 175 having widths less than the widths of the un-etched parts of the amorphous carbon are formed on the sidewalls of the amorphous carbon. The amorphous carbon is then removed, leaving behind the sidewall spacers 175 to form the mask pattern 177. Thus, the spacers 175 form the mask 177 having feature sizes less than the resolution of the photolithography process used to form the pattern on the photoresist. A protective material 200 is deposited around the spacers 175. The spacers 175 are further protected using a hard mask 210 and then photoresist 220 is formed and patterned over the hard mask 210. The photoresist pattern 230 is transferred through the hard mask 210 to the protective material 200. The combination of the patterns 177 and 230 made out by the spacers 175 and the protective material 200 is then transferred to an underlying amorphous carbon hard mask layer 160. The combined pattern, having features of difference sizes, is then transferred to the underlying substrate 110.

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