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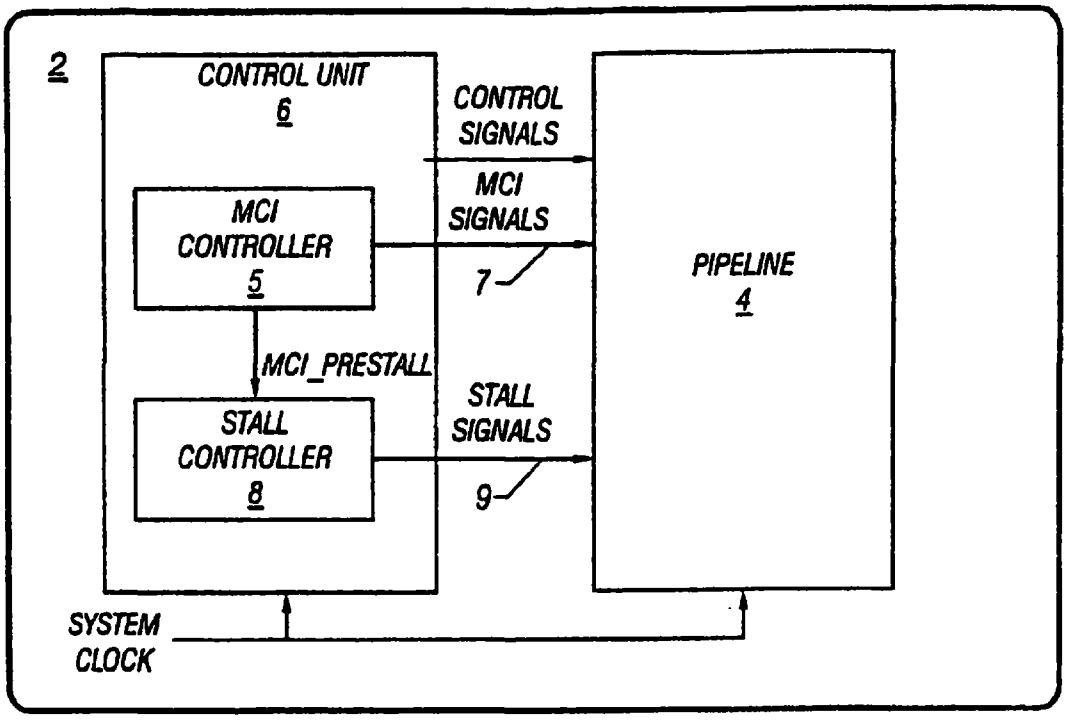
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(54) Title: MULTI-CYCLE INSTRUCTIONS

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(57) Abstract: In one embodiment, a pipelined processor is described that includes an execution pipeline having a plurality of stages and a multi-cycle instruction (MCI) controller adapted to assert a stall signal to stall the multi-cycle instruction within one of the stages of the execution pipeline. The MCI controller is adapted to issue a plurality of instructions to subsequent stages in the pipeline while the multi-cycle instruction is stalled.

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