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METHOD OF AND APPARATUS FOR RECORDING AND REPRODUCING DATA AND TRANSMITTING DATA

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to a method of and an apparatus for recording and reproducing data, and transmitting data.

Description of the Related Art:

Optical disks which have heretofore been proposed include a magnetooptical disk, an optical disk as a phase-change medium, a write-once disk, a read-only optical disk, etc. These optical disks can roughly be classified into writable disks and read-only disks.

If a defective sector is detected on a magnetooptical disk as a writable disk in a disk certifying process at the time it is manufactured, then a sector positioned adjacent to the defective sector is used as a replacement sector for the defective sector, and information as to the replacement sector is recorded in a given area on the magnetooptical disk. When the magnetooptical disk is played back, the replacement sector is used instead of the defective sector. If a new defective sector is produced on the magnetooptical disk after it is shipped, a replacement sector for the defective sector is established in a region dedicated for the replacement sector, and data to be recorded in the defector sector is recorded in the replacement

sector, and its information is recorded in a given area on the magnetooptical disk.

No data are recorded on a read-only optical disk by an optical disk drive. As well known in the art, when a read-only optical disk is manufactured, data are recorded on the read-only optical disk, and after it is shipped, the data recorded on the read-only optical disk at the time it is manufactured are read only.

When data are recorded on a magnetooptical disk by an optical disk drive or data are recorded on a read-only optical disk when it is manufactured, parity bits such as error-correcting parity bits and error-checking parity bits such as CRC (cyclic redundancy check) bits are added to the data. When the recorded data are reproduced from the magnetooptical disk or the read-only optical disk, the data are subjected to an error-checking process and an error-correcting process using the parity bits.

One known parity system is a Reed-Solomon code. According to the Reed-Solomon code, if one symbol is composed of eight bits and data of k symbols, then a parity bit is added to the k symbols, resulting in a code of n symbols. The term which represents the correcting ability of the error-correcting code is "minimum distance".

For example, if one symbol is represented by one bit, then the n symbols are represented by n bits, and hence there are 2^n binary data strings available for the n symbols to assume. Without the parity bits, there are 2^k binary data

strings available for the k symbols to assume. The 2^k binary data strings are taken from the 2^n binary data strings, and if there are different d bits between any two data strings, then "d" is referred to as a "distance". A minimum one of the distances determined with respect to all the 2^k binary data strings is referred to as a "minimum distance". The term "minimum distance" will hereinafter be referred to as a "distance".

The distance d of a code for correcting t1 errors is generally required to satisfy the following formula (1):

$$d \geq 2t1 + 1. \quad \cdots(1)$$

If the distance d is "17", for example, then t1 is 8. That is, the code can correct up to 8 symbols.

The code is also capable of detecting errors as well as correcting errors. If the number of errors that can be detected by the error-detecting capability of the code is t2, then the number t2 of detectable errors is expressed by the following equation (2):

$$t2 = d - (2t1 + 1) \ (t2 \geq 0). \quad \cdots(2)$$

For example, the number t1 of correctable errors and the number t2 of detectable errors in the case where the distance d is "17" are given in the following table 1:

0 symbol correction···t1 = 0, t2 = 16

1 symbol correction···t1 = 1, t2 = 14

2 symbol correction···t1 = 2, t2 = 12

3 symbol correction···t1 = 3, t2 = 10

4 symbol correction···t1 = 4, t2 = 8

5 symbol correction···t1 = 5, t2 = 6

6 symbol correction···t1 = 6, t2 = 4

7 symbol correction···t1 = 7, t2 = 2

8 symbol correction···t1 = 8, t2 = 0···(Table 1)

As can be seen from the table 1 above, since the number of detectable errors is "0" for the 8 symbol correction, it will not be able to detect errors properly if errors of 9 symbols or more are generated for the 8 symbol correction. If the distance d is of an increased value, then the number of detectable errors is increased while keeping the ability to detect errors. The Reed-Solomon code thus constructed is also referred to as an (n, k, d) LDC (long-distance code), which is so called because the distance d is relatively large.

On magnetooptical disks, read-only optical disks, or the like, data are recorded after the above Reed-Solomon code has been constructed. When the recorded data are reproduced, random errors or a burst of errors having a length depending on the distance d, the number t1 of correctable errors, and the number t2 of detectable errors can be corrected by the Reed-Solomon code.

As can be understood from the table 1 above, if the distance d is "17", then the number of correctable errors is 8 at maximum. Therefore, if a burst of 9 successive errors or more occurs, then the errors cannot be corrected, and data with the errors are reproduced as they are.

Various error-correcting processes have been employed for writable disks such as magnetooptical disks. According to one process, if there is a defective sector on a writable disk, it is replaced with a replacement sector, and data are recorded in the replacement sector so that they will be reproduced properly. According to another process, in order to cope with a burst of errors, a parity sector is included in each circumferential track or every set of circumferential tracks on a writable disk, and parity data produced when data in other sectors in each circumferential track or every set circumferential tracks are exclusive-ORed are recorded in the parity sector. When a burst of errors occurs in data, the burst of errors is corrected based on the parity data read from the parity sector.

When data to be processed on a real-time basis, such as moving-image data, are handled, the former process which uses replacement sectors poses a problem in that the processing speed is slowed by the use of replacement sectors. The latter process of correcting errors on the writable disk with parity sectors is also disadvantageous in that the time required to correct a burst of errors is long because when a burst of errors occurs in an area composed of sectors in a circumferential track or every set of circumferential tracks, it is necessary to read again the data from the area, and correct the burst of errors based on the data read again and the parity data recorded in the parity sector.

On read-only optical disks, no replacement sectors can be employed. If large errors such as a burst of errors occur when data are reproduced from a read-only optical disk, then the errors need to be corrected with an increased distance d or parity sectors insofar as only a prerecorded error-correcting code is relied upon. The increased distance d has problems in that it increases the redundancy of the code and the processing time. The increased redundancy of the code results in a corresponding reduction in the capacity of the read-only optical disk to record data. Correcting errors on the read-only optical disk with parity sectors is also disadvantageous in that the time required to process a burst of errors is long because when a burst of errors occurs in an area composed of sectors in a circumferential track or every set of circumferential tracks, it is necessary to reproduce again the data from the area, and correct the burst of errors based on the data reproduced again and the parity data recorded in the parity sector.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method of and an apparatus for recording and reproducing data and transmitting data efficiently to allow data to be reproduced and transmitted without reducing the capacity to record data even if a burst of errors occurs.

According to an aspect of the present invention, there is provided a method of recording and reproducing data, comprising the steps of (a) generating first error-processing data with respect to a predetermined amount of data, and generating second error-processing data with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, (b) generating data of record units from the predetermined amount of data, the first error-processing data, and the second error-processing data, (c) recording the data of record units on a recording medium, (d) reproducing the data of record units on the recording medium, (e) correcting errors in the predetermined amount of data in the reproduced data of record units with the first error-processing data with respect to each of the record units, (f) if errors cannot be corrected in the step (e), at least detecting errors in the predetermined amount of data in each of the blocks with the second error-processing data, and (g) when errors are detected in N (N is a positive integer) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with the first error-processing data, thus producing reproduced data.

According to another aspect of the present invention, there is provided a method of transmitting data, comprising the steps of (a) generating first error-processing

data with respect to a predetermined amount of data, and generating second error-processing data with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, (b) generating transmission data of units from the predetermined amount of data, the first error-processing data, and the second error-processing data, (c) transmitting the transmission the data of units, (d) correcting errors in the transmission data of units which have been transmitted with the first error-processing data with respect to each of the transmitted units, (e) if errors cannot be corrected in the step (d), at least detecting errors in the transmitted data in each of the blocks with the second error-processing data, and (f) when errors are detected in N (N is an integer of at least 3) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the transmitted units with the first error-processing data.

According to still another aspect of the present invention, there is provided an apparatus for recording and reproducing data, comprising error-processing data generating means for generating first error-processing data with respect to a predetermined amount of data, and second error-processing data with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, record unit data generating means for generating data

of record units from the predetermined amount of data, the first error-processing data, and the second error-processing data, recording and reproducing means for recording the data of record units on a recording medium and reproducing the data of record units on the recording medium, and error correcting means for correcting errors in the predetermined amount of data in the data of record units reproduced by the recording and reproducing means with the first error-processing data with respect to each of the record units, and if errors cannot be corrected, at least detecting errors in the predetermined amount of data in each of the blocks with the second error-processing data, and when errors are detected in N (N is a positive integer) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with the first error-processing data.

According to yet still another aspect of the present invention, there is provided an apparatus for transmitting data, comprising error-processing data generating means for generating first error-processing data with respect to a predetermined amount of data, and second error-processing data with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, transmission data generating means for generating transmission data of units from the predetermined amount of data, the first er-

ror-processing data, and the second error-processing data, transmitting means for transmitting the transmission the data of units, and error correcting means for correcting errors in the transmission data of units which have been transmitted with the first error-processing data with respect to each of the transmitted units, and if errors cannot be corrected, at least detecting errors in the transmitted data in each of the blocks with the second error-processing data, and when errors are detected in N (N is an integer of at least 3) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the transmitted units with the first error-processing data.

According to a further aspect of the present invention, there is provided a method of reproducing data, comprising the steps of (a) reproducing data of record units from a recording medium on which there are recorded a predetermined amount of data, first error-processing data generated with respect to the predetermined amount of data, and second error-processing data generated with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, making up the data of record units, (b) correcting errors in the predetermined amount of data in the reproduced data of record units with the first error-processing data with respect to each of the record units, (c) if errors cannot be corrected in the step (b), at least

detecting errors in the predetermined amount of data in each of the blocks with the second error-processing data, and (d) when errors are detected in N (N is a positive integer) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with the first error-processing data, thus producing reproduced data.

According to a still further aspect of the present invention, there is provided a method of transmitting data, comprising the steps of (a) transmitting transmission data of units which are composed of a predetermined amount of data, first error-processing data generated with respect to the predetermined amount of data, and second error-processing data generated with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, (b) correcting errors in the transmission data in the units which are transmitted with respect to each of the transmitted units, (c) if errors cannot be corrected in the step (b), at least detecting errors in the transmission data in each of the blocks with the second error-processing data, and (d) when errors are detected in N (N is an integer of at least 3) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the transmitted units with the first error-processing data.

According to a yet still further aspect of the present invention, there is provided an apparatus for reproducing data, comprising reproducing means for reproducing data of record units from a recording medium on which there are recorded a predetermined amount of data, first error-processing data generated with respect to the predetermined amount of data, and second error-processing data generated with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, making up the data of record units, error correcting means for correcting errors in the predetermined amount of data in the data of record units reproduced by the reproducing means, with the first error-processing data with respect to each of the record units, and if errors cannot be corrected, at least detecting errors in the predetermined amount of data in each of the blocks with the second error-processing data, and when errors are detected in N (N is a positive integer) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with the first error-processing data.

According to another aspect of the present invention, there is provided an apparatus for recording and reproducing data, comprising error-processing data generating means for generating first error-processing data with respect to a predetermined amount of data, and second error-

processing data with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, record unit data generating means for generating data of record units from the predetermined amount of data, the first error-processing data, and the second error-processing data, recording and reproducing means for recording the data of record units on a recording medium and reproducing the data of record units on the recording medium, error detecting means for detecting an error status, in each of the blocks, of a reproduced signal indicative the data of record units which are reproduced by the recording and reproducing means, based on a video level of the reproduced signal, and error correcting means for correcting errors in the predetermined amount of data in the data of record units reproduced by the recording and reproducing means, with the first error-processing data with respect to each of the record units, and if errors cannot be corrected with the first error-processing data with respect to each of the record units, determining blocks as errors based on the error status detected by the error detecting means, and when N (N is a positive integer) successive blocks are determined as errors, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with the first error-processing data.

According to still another aspect of the present invention, there is provided an apparatus for reproducing data, comprising reproducing means for reproducing data of record units from a recording medium on which there are recorded a predetermined amount of data, first error-processing data generated with respect to the predetermined amount of data, and second error-processing data generated with respect to each of a plurality of blocks produced by dividing the predetermined amount of data, making up the data of record units, error detecting means for detecting an error status, in each of the blocks, of a reproduced signal indicative the data of record units which are reproduced by the reproducing means, based on a video level of the reproduced signal, and error correcting means for correcting errors in the predetermined amount of data in the data of record units reproduced by the reproducing means, with the first error-processing data with respect to each of the record units, and if errors cannot be corrected, determining blocks as errors based on the error status detected by the error detecting means, and when N (N is a positive integer) successive blocks are determined as errors, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with the first error-processing data.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an optical disk drive according to the present invention;

FIG. 2 is a block diagram of a drive controller in the optical disk drive shown in FIG. 1;

FIG. 3 is a block diagram of a controller in the optical disk drive shown in FIG. 1;

FIG. 4 is a view showing a format of an optical disk according to the present invention;

FIG. 5 is a diagram showing areas on the optical disk shown in FIG. 4 and data clock frequencies used in the areas;

FIGS. 6A, 6B, and 6C are diagrams showing a sector format of the optical disk shown in FIG. 4;

FIG. 7 is a diagram illustrative of addition of parity data as a second ECC in a pattern of 7 lines - 8 lines - 7 lines on an optical disk according to the present invention;

FIG. 8 is a diagram showing how to process a burst of errors which occurs in a sector;

FIG. 9 is a diagram showing how to process a plurality of bursts of errors occur in a sector;

FIG. 10 is a flowchart of a process of operation of the controller shown in FIG. 3, for processing data upon reproduction thereof by the optical disk drive shown in FIG. 1;

FIG. 11 is a flowchart of subroutines of the process shown in FIG. 10;

FIGS. 12 and 13 are flowcharts of a subroutine of the process shown in FIG. 10;

FIG. 14 is a block diagram of a level detector according to another embodiment of the present invention;

FIG. 15 is a block diagram of a controller according to the other embodiment of the present invention; and

FIG. 16 is a flowchart of operation of the controller shown in FIG. 15.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows, by way of example, an arrangement of an optical disk drive according to the present invention. The optical disk drive is capable of recording data on and reproducing data from a magnetooptical disk and a write-once disk, reading data from a read-only optical disk, writing data in and reading data from a writable/readable area on a so-called partial ROM, and reading data from a read-only area on such a partial ROM.

As shown in FIG. 1, the optical disk drive includes a drive 1 for recording data on and reading data from an optical disk 4, a drive controller 2 for controlling the drive 1, and a host computer 3 connected to the drive controller 2 through a SCSI (Small Computer Systems Interface) input/output terminal io1, for accessing the optical disk 4 through the drive controller 2.

The optical disk 4 may comprise a magnetooptical disk, an optical disk as a phase-change medium, a write-once

disk, a partial disk having a writable area (RAM) and a read-only area (ROM), a read-only optical disk, or the like.

The drive 1 comprises a loading mechanism 5 for loading the optical disk 4, a spindle motor 6 for rotating the optical disk 4 which has been loaded by the loading mechanism 5, a driver 7 for energizing the spindle motor 6, an optical block 8, a driver 14 for energizing a laser diode 13 in the optical block 8, an I-V/matrix amplifier 16 for converting a reproduced signal from the optical block 8 from a current signal into a voltage signal, and supplying the voltage signal to a plurality of systems, a magnetic head 17 for applying a magnetic field to the optical disk 4, and a driver 18 for energizing the magnetic head 17. The I-V/matrix amplifier 16 produces an RF signal and an MO (magnetooptical) signal by combining a plurality of output signals from a photodetector 15 in the optical block 8.

The optical block 8 comprises an objective 9 for applying a laser beam to the optical disk 4 and applying a laser beam reflected from the optical disk 4 to a photodetector 15, a slide motor 10 for moving the optical block 8 radially with respect to the optical disk 4, a galvanometer motor 11 for tracking the optical block 8, a focus actuator 12 for focusing the laser beam on the optical disk 4, a laser diode 13 for emitting the laser beam to be applied to the optical disk 4 by the objective 9, and a photodetector 15 for detecting the laser beam emitted from the laser diode 13.

The driver 18 for energizing the magnetic head 17 is connected through an input terminal 1i1 to an output terminal 2o1 of the drive controller 2. The driver 14 for energizing the laser diode 13 is connected through input terminals 1i2, 1i3 to output terminals 2o2, 2o3 of the drive controller 2. The I-V matrix amplifier 16 is connected through output terminals 1o1, 1o2, 1o3, 1o4, 1o5 to input terminals 2i1, 2i2, 2i3, 2i4, 2i5 of the drive controller 2. The focus actuator 12 is connected through an input terminal 1i4 to an output terminal 2o4 of the drive controller 2. The galvanometer motor 11 is connected through an input terminal 1i5 to an output terminal 2o5 of the drive controller 2. The slide motor 10 is connected through an input terminal 1i6 to an output terminal 2o6 of the drive controller 2. The driver 7 for energizing the spindle motor 6 is connected through an input/output terminal 1io7 to an input/output terminal 2io7 of the drive controller 2. The loading mechanism 5 is connected through an input terminal 1i7 to an output terminal 2o7 of the drive controller 2.

A process for transmitting and receiving commands and data is carried out by the drive controller 2. For recording data, the drive controller 2 adds CRC bits and an error-correcting code to data from the host computer 3, and transmits the data to the drive 1. For reproducing data, the drive controller 2 corrects errors in data from the drive 1, and transfer only user data to the host computer 3. When the data are recorded and reproduced, the drive con-

troller 2 issues commands to a servo control system and the various blocks in the drive 1.

FIG. 2 illustrates, by way of example, an arrangement of the drive controller 2 shown in FIG. 1.

As shown in FIG. 2, the drive controller 2 has an input/output circuit 31 for supplying bias data for the laser diode 13, which have been supplied from a digital signal processor 53 through a bus 43, through a D/A converter 32 and the output terminal 2o2 to the driver 14 shown in FIG. 1. The drive controller 2 also has a selector/clamp circuit 33 for selecting output signals supplied from the I-V/matrix amplifier 16 (FIG. 1) through the input terminals 2i1, 2i2 based on a timing signal from a servo control system timing generator 40, and clamping a selected output signal. An A/D converter 34 converts an output signal from the selector/clamp circuit 33 into digital data based on a servo system clock signal or a data system clock signal selected by and supplied from a clock selector 41.

A data system clock generator 35 generates a data system clock signal based on a servo system clock signal from a servo system clock generator 39. A data system timing generator 36 generates a data system timing signal based on the data system clock signal. Based on reference phase data extracted from reproduced data from the A/D converter 34, a data phase control circuit 37 controls the phase of the data system clock signal from the data system clock generator 35, supplies the phase-controlled data system clock

signal as a reading clock signal to a reading/writing circuit 38, controls the phase of a writing position control signal from the reading/writing circuit 38, and outputs the phase-controlled writing position control signal through the output terminal 2o1.

When data are reproduced, the reading/writing circuit 38 responds to a request signal from a controller 44 to supply output data from the A/D converter 34 to the controller 44 based on the data system clock signal from the data system clock generator 35 and the data system timing signal from the data system timing generator 36, outputting an acknowledgment signal. When data are recorded, the reading/writing circuit 38 responds to a request signal from the controller 44 to supply data from the controller 44 through the output terminal 2o1 and the input terminal 1i1 shown in FIG. 1 to the driver 18.

The servo system clock generator 39 generates a servo system clock signal from the output data from the A/D converter 34, and supplies the generated servo system clock signal to the servo system timing generator 40, the clock selector 41, and an address decoder 42. The servo system timing generator 40 generates a servo system timing signal based on the servo system clock signal supplied from the servo system clock generator 39, supplies the generated servo system timing signal to the clock selector 41, the address decoder 42, and the selector/clamp circuit 33, and also supplies the generated servo system timing signal

through the output terminal 2o3 and the input terminal 1i3 (FIG. 1) to the driver 14 for the laser diode 13.

The drive controller 2 further includes a multiplexer 45 for supplying a front APC (automatic power control) signal, a focus error signal, and a pull-in signal supplied through the respective input terminals 2i3, 2i4, 2i5 from the I-V/matrix amplifier 16 to an A/D converter 46. An input/output circuit 47 supplies output data from the A/D converter 46 through the bus 43 to the digital signal processor 53. A PWM (pulse-width-modulation) circuit 48 serves to modulate data for actuating the optical block 8 which have been supplied from the digital signal processor 53 through the bus 43.

The drive controller 2 also has drivers 49, 50, 51 for energizing the focus actuator 12 (FIG. 1), the galvanometer motor 10 (FIG. 1), and the slide motor 11 (FIG. 1), respectively, based on the modulated data from the PWM circuit 48. The driver 49 is connected to the focus actuator 12 through the output terminal 2o4 and the input terminal 1i4 shown in FIG 1. The driver 50 is connected to the galvanometer motor 10 through the output terminal 2o5 and the input terminal 1i5 shown in FIG 1. The driver 51 is connected to the slide motor 10 through the output terminal 2o6 and the input terminal 1i6 shown in FIG 1.

An input/output circuit 52 supplies a drive signal supplied from the digital signal processor 53 to the spindle motor 6 (FIG. 1) through the input/output terminal

1io7, 2io7 and the driver 7 (FIG. 1). The digital signal processor 53 serves to control and energize the various blocks described above through the bus 43, and is connected to the controller 44 through a bus indicated by the thick solid line shown in FIG. 2.

In response to a request from the host computer 3 with the optical disk 4 mounted on the spindle motor 6 by the loading mechanism 5, or when the optical disk 4 is loaded by the loading mechanism 5 in an automatic spin-up mode, the digital signal processor 53 issues a command through the input/output circuit 52 to the driver 7 to energize the spindle motor 6.

When the rotational speed of the spindle motor 6 reaches a predetermined rotational speed, the driver 7 outputs a lock signal to indicate to the digital signal processor 53 that the rotational speed of the spindle motor 6 is stabilized. During this time, the digital signal processor 53 causes the PWM circuit 48 to control the driver 50 to position the laser beam from the laser diode 13 outside of a user area of the optical disk 4, and also causes the PWM circuit 48 to control the driver 51 to move the optical block 8 radially inwardly or outwardly of the optical disk 4.

If the laser beam were focused in the user area, the data of the optical disk 4 which is highly sensitive would possibly be erased in error. Since the optical block 8 is moved out of the user area and the laser beam is fo-

cused outside of the user area, such erroneous data erasure is prevented.

When the spindle motor 6 rotates at a constant speed and the optical block 8 is moved radially outwardly of the optical disk 4, the digital signal processor 53 supplies a bias current for the laser diode 13 through the input/output circuit 31 and the D/A converter 32 to the driver 14, and outputs a command to the servo system timing generator 40 to turn on the laser diode 13 to emit a laser beam.

The laser beam emitted from the laser diode 13 is applied to the photodetector 15 in the optical block 8, and the photodetector 15 converts the laser beam into a corresponding electric signal. The electric signal from the photodetector 15 is supplied as a detected output signal to the I-V/matrix amplifier 16, which converts the detected output signal into a voltage signal that is then supplied as a front APC signal to the multiplexer 45.

The front APC signal applied to the multiplexer 45 is time-division-multiplexed thereby, and then converted by the A/D converter 46 into a digital signal, which is supplied through the input/output circuit 47 and the bus 43 to the digital signal processor 53. The digital signal processor 53 recognizes the intensity of the laser beam emitted from the laser diode 13 based on the digital front APC signal, and sends back intensity control data calculated by a digital filter (not shown) through the input/output circuit 31 and the D/A converter 32 to the driver 14 to enable the

driver 14 to control the laser diode 13 to produce a constant laser beam power.

Then, the digital signal processor 53 controls the PWM circuit 48 to supply a current to the driver 49 for thereby energizing the focus actuator 12 in a vertical direction to bring the focus actuator 12 into a focus search mode. At this time, the laser beam reflected by the optical disk 4 is applied to a light-detecting surface of the photodetector 15. The laser beam detected by the photodetector 15 is converted into an electric signal, which is supplied as a detected output signal to the I-V/matrix amplifier 16. The I-V/matrix amplifier 16 converts the supplied signal into a voltage signal and amplifies the voltage signal. The amplified voltage signal is then supplied from the I-V/matrix amplifier 16 as a focus error signal to the multiplexer 45.

The focus error signal is time-division-multiplexed together with the front APC signal by the multiplexer 45, and then converted by the A/D converter 46 into a digital signal. The digital focus error signal is supplied through the input/output circuit 47 and the bus 43 to the digital signal processor 53. The digital signal processor 53 digitally filters the digital focus error signal thereby to produce focus control data and feed the focus control data from the PWM circuit 48 back to the driver 49, thereby providing a focus control servo loop. When the focused condition of the laser beam is stabilized in the focus search

mode, an RF signal outputted from the photodetector 15 and produced through the I-V/matrix amplifier 16 has a substantially constant amplitude. After the RF signal has been clamped to a certain potential by the selector/clamp circuit 33, the RF signal is converted into a digital signal by the A/D converter 34.

A clock signal at this time has a free-running frequency of the servo system clock generator 39. Timing pulses for clamping signals with the selector/clamp circuit 33 are produced by frequency-dividing the free-running frequency of the servo system clock generator 39.

The servo system clock generator 39 checks a pattern of pits formed on the optical disk 4 by determining an amplitude difference of the digital RF signal produced by the A/D converter 34, for thereby searching for a pattern which is the same as a pit train in a servo area. When the pattern is found, the servo system clock generator 39 controls the clock selector 41 to open a window in a position where a next pattern is to appear, and confirms whether patterns agree with each other again in the window.

If the above operation is confirmed successively in a certain number of times, then it is determined that the servo system clock generator 39 is locked to the pattern of pits on the optical disk 4. Phase information is produced by determining the difference between the amplitudes at both sides of wobble pits in the servo area. By adding phase information produced from both of two wobble pits, a gain

variation caused by a change in amplitude depending on the tracking position is absorbed.

When the servo system clock generator 39 is locked, the positions of segment units are made clear and the positions of segment mark pits on the optical disk 4 can be recognized. RF signals are sampled at a plurality of positions Ar1, Ar2, Ar3, Ar4 with respect to segment mark pits, address mark pits, sector flag 1 pits, and sector flag 2 pits, and one of the positions where the amplitude of the sampled RF signal is maximum is searched for.

If the position is Ar1, then it represents an address mark, and its segment is an address segment, making it possible to recognize the starting end of a frame. Therefore, frames can be synchronized by clearing a frame counter. If one frame is composed of 14 segments, then the clock selector 41 is controlled to open a window in every 14 segments, and frame synchronization is judged as being locked when the segments can be successively recognized as an address mark.

When frames are synchronized, the positions where addresses are recorded on the optical disk 4 can be recognized. Consequently, track addresses and frame codes are decoded by the address decoder 42. The address decoder 42 decodes track addresses and frame codes by checking agreement between patterns in the form of gray codes each of 4 bits and a gray code table. Since the entire patterns, not just 4 bits, are converted into gray codes, not simple

agreement with the table is checked, but comparison is made with the table inverted depending on whether LSB in high-order 4 bits is "1" or "0".

Rotational synchronization is regarded as being achieved when a frame code that is decoded first is loaded into the frame counter, a numerical value obtained by incrementing the frame counter for each frame is compared with an actually reproduced frame, and it is confirmed that numerical values agree successively with actually reproduced frames. Thereafter, numerical values produced by the frame counter are returned as frame codes to the digital signal processor 53 for preventing frame positions from being recognized in error even when certain defects are present.

The digital signal processor 53 calculates the speed of the optical block 8 while reading the track addresses in the form of gray codes, and causes the PWM circuit 48 to control the slide motor 10 of the optical block 8 through the driver 51 for thereby moving the optical block 8 to a desired track on the optical disk 4.

When the optical block 8 positionally reaches the desired track on the optical disk 4, the optical block 8 enters a tracking mode. A tracking error signal is produced by determining the difference between the amplitudes of RF signals from two wobble pits in the servo area. The digital signal processor 53 digitally filers the tracking error signal to produce tracking control data, and supplies the tracking control data to cause the PWM circuit 48 to control

the driver 50 for thereby energizing the galvanometer motor 11 in the optical block 8 to control variations in low-frequency components and also to effect tracking control to position the spot of the laser beam emitted from the laser diode 13 at the center of the track on the optical disk 4.

While the optical block 8 is being thus under tracking control, the digital signal processor 53 detects the position of the start of a desired track. The segment at the start of each sector and a segment preceding the segment are associated with sector marks. The clock selector 41 is controlled to open a window in each of the above four positions Ar1, Ar2, Ar3, Ar4, and when the position with the maximum amplitude among RF signals sampled at the four positions Ar1, Ar2, Ar3, Ar4 is the position Ar2, each sector mark represents the segment at the start of a sector, and when the position with the maximum amplitude is the position Ar3, each sector mark represents the segment that precedes the start of a sector. Basically, the segment at the start of a sector is determined by converting an sector address given by the host computer 3 into a physical sector and calculating which segment of which track the sector belongs to. The probability that the sector marks of the above two types will simultaneously be defective is very small, and hence the probability that defective sectors will be produced thereby is also very small.

The data system clock generator 35 generates a data clock signal by multiplying, by M/N, a frame-

synchronized servo clock signal produced from the servo system clock generator 39, and imparts the generated data clock signal to the data system timing generator 36 and the reading/writing circuit 38.

In a recording mode, the reading/writing circuit 38 is supplied with data to be recorded from the host computer 3 through the controller 44. The reading/writing circuit 38 then adds random numbers over 127 periods, for example, to the supplied data by exlusive-ORing them, thereby scrambling the data in each sector according to $Y = X^7 + X + 1$, and modulates the scrambled data into NRZI data in synchronism with a data clock signal. At this time, the reading/writing circuit 38 sets an initial value to "0" for each segment, and supplies the modulated signal through the driver 18 to the magnetic head 17.

The magnetic head 17 generates a magnetic field depending on the modulated signal, and applies the magnetic field to a data area of the optical disk 4 which has been heated to the Curie temperature by the laser beam emitted from the laser diode 13, for thereby recording the NRZI data on the optical disk 4.

In a reproducing mode, an MO signal or an RF signal produced by the I-V/matrix amplifier 16 based on a detected output signal from the photodetector 15 is clamped to a predetermined potential by the selector/clamp circuit 33, and thereafter converted by the A/D converter 34 into a digital signal that is supplied to the reading/writing cir-

cuit 38. The reading/writing circuit 38 digitally filters the digital reproduced signal from the A/D converter 34 according to a partial response, and reproduces NRZI data based on Viterbi decoding. After having converted the NRZI data into NRZ data in each segment, the reading/writing circuit 38 descrambles the NRZ data in each sector, converts the descrambled data into reproduced data, and transfers the reproduced data through the controller 44 to the host computer 3. The MO signal and the RF signal are produced by combining a number of output signals from the photodetectors 15 in different combinations.

FIG. 3 shows, by way of example, an arrangement of the controller 44 shown in FIG. 2.

As shown in FIG. 3, the controller 44 has a CPU 60, a bus 61 connected to the CPU 60 and composed of an address bus, a data bus, and a control bus, a ROM 62 for storing various program data, parameter data, etc. for effecting various processes in the reproducing mode, a RAM 63 for use as a work storage area for storing program data, parameter data, etc. which are stored in the ROM 62, and an input/output port 64. The controller 44 also has a decoder 67 for effecting error correction and error checking on reproduced data, an encoder 68 for generating parity data with respect to data supplied from the host computer 3 and adding the generated parity data to the supplied data, a buffer 70, and an interface 71. The ROM 62, the RAM 63, the in-

put/output port 64, the decoder 67, the encoder 68, the buffer 70, and the interface 71 are connected to the bus 61.

The controller 44 also has an input/output terminal 65 connected to the reading/writing circuit 38 shown in FIG. 2 and a movable contact "c" of a switch 66. The switch 66 has a fixed contact "a" connected to an input terminal of the decoder 67, and another fixed contact "b" connected to an output terminal of the encoder 68.

The decoder 67 has a data output terminal connected to a fixed terminal "a" of a switch 69, and the encoder 68 has an input terminal connected to another fixed terminal "b" of the switch 69. The switch 69 has a movable contact "c" connected to an input/output terminal of the buffer 70 whose another input/output terminal is connected to an input/output terminal of the interface 71. The interface 71 has another input/output terminal connected through the input/output terminal io1 to the input/output terminal of the host computer 3 shown in FIG. 1.

The decoder 67 effects error detection on reproduced data supplied through the switch 66 using a first ECC, effects error checking using the CRC when the number of detected errors reaches a number of errors that cannot be corrected, and effects error detection using a second ECC when errors are detected.

The decoder 67 comprises RAMs 67a, 67b and a RAM controller 67c for controlling reproduced data stored in the RAMs 67a, 67b to effect error correction using the LDC, er-

ror checking using the CRC, and error detection using the second ECC upon occurrence of a burst of errors for which the error correction and the error checking are ineffective. Each of the RAMs 67a, 67b has a storage capacity for storing one sector (composed of 2352 bytes in this embodiment) of reproduced data, and various data generated in an error detecting process and an error checking process described later on.

The decoder 67 supplies output data through the switch 69 to the buffer 70. The second ECC is parity data recorded in a given area of a sector next to the sector being recorded, among ECC parity data generated by the data in the sector being recorded. The second ECC is also parity data which is used upon decoding to detect the position of an error in data in a sector when error correction on the data is impossible to carry out using parity data as the first ECC or an error is detected as occurring upon error checking using the CRC.

As shown in FIG. 3, the encoder 68 comprises RAMs 68a, 68b each having a storage capacity for storing one sector, and a RAM controller 68c for controlling input data stored in the RAMs 68a, 68b to generate parity data as the first ECC, parity data as the CRC, parity data as the second ECC, and add these parity data. However, the encoder 68 adds only the parity data generated as the second ECC with respect to the user data in a certain area to the user data in a next area.

The encoder 68 adds these parity data to the data transferred from the host computer 3 and also adds the parity data as the second ECC in the preceding sector to the data.

The parity data for error checking and the parity data for error correction can be recorded in a writable area on a magnetooptical disk, a write-once disk, and a partial disk by the optical disk drive shown in FIG. 1. These parity data are recorded in a read-only area on a read-only optical disk or a partial disk when the disk is manufactured.

An input/output terminal 72 connected to the input/output port 64 is connected to the bus 43 of the digital signal processor 53 shown in FIG. 2. An input/output terminal 73 connected to the input/output port 64 is connected to an acknowledgment signal input terminal of the reading/writing circuit 38 shown in FIG. 2. An input/output terminal 74 connected to the input/output port 64 is connected to an request input signal of the reading/writing circuit 38 shown in FIG. 2.

A process of recording data transferred from the host computer 3 on the optical disk 4 will be described below.

The CPU 60 supplies a switching control signal through the input/output port 64 to the switches 66, 69 to connect the movable contacts "c" of the switches 66, 69 to the fixed contacts "b" thereof. Data to be recorded which

are transferred from the host computer 3 are read from the buffer 70, and thereafter supplied through the switch 69 to the encoder 68 which adds error-detecting and error-correcting codes to the data. Thereafter, the data are supplied through the switch 66 and the input/output terminal 65 to the reading/writing circuit 38 shown in FIG. 2, by which the data are recorded in the user area of the optical disk 4.

At this time, the encoder 68 adds parity data to data of a certain sector (Nth sector) stored in the RAM 68a. When data processing for recording is finished, the encoder 68 supplies the data of the Nth sector with the parity data added thereto through the switch 63 to the input/output terminal 65, and supplies a signal indicative of the outputting of the data to the CPU 60 through the input/output port 64 and the bus 61. The CPU 60 now instructs the reading/writing circuit 38 shown in FIG. 2 to record the data, and controls the buffer 70 and the interface 71 to receive next input data. In this manner, all data of the Nth sector are supplied to the drive 1 and recorded on the optical disk 4, during which time next input data are stored as data of a next sector ((N+1)th sector) in the RAM 68b.

To reproduce data recorded on the optical disk 4, the CPU 60 supplies a switching control signal through the input/output port 64 to the switches 66, 69 to connect the movable contacts "c" to the fixed contacts "a". Reproduced data read from the optical disk 4 and supplied through the

reading/writing circuit 38, the input/output terminal 65, and the switch 66 are supplied to the decoder 67. The decoder 67 detects and corrects errors in the reproduced data, and supplies the reproduced data through the switch 69, the buffer 70, the interface 71, and the input/output terminal io1 to the host computer 3 shown in FIG. 1.

At this time, when the decoder 67 corrects errors with parity data as first ECC, check errors with CRC parity data, or fails to correct errors because of a burst of errors, in the data of the Nth sector stored in the RAM 67a, the decoder 67 reads parity data as second ECC from the data of the (N+1)th sector stored in the RAM 67b, and detects the position of errors using the parity data as the second ECC. After having recognized the position of errors, the decoder 67 corrects the errors with the parity data as the first ECC to correct the data of the Nth sector, and then checks errors with the CRC parity data.

When the above reproducing process is finished, the decoder 67 outputs the data of the Nth sector, and supplies a signal indicative of the finishing of the reproducing process to the CPU 60 through the input/output port 64 and the bus 61. The CPU 60 now instructs the reading/writing circuit 38 shown in FIG. 2 to reproduce data of a next sector. In this manner, all data of the sector are supplied to the buffer 70, after which reproduced data of an (N+2)th sector read from the optical disk 4 are supplied to the RAM 67a.

The optical disk drive shown in FIGS. 1 through 3 may comprise a read-only optical disk, a disk having only a read-only area such as a partial disk or the like, a disk having a writable area in addition to a read-only area, a disk having only a read-only area such as a magnetooptical disk, a write-once disk, or the like, or a disk having a readable area in addition to a write-only area.

FIG. 4 shows, by way of example, a format of the optical disk 4.

As shown in FIG. 4, the optical disk 4 has a GCP (gray code part) area in which disk type data, etc. are recorded, a CTL (control) area, a TEST area, a BAND 0, BAND 1, ···, BAND 15, a TEST area, a CTL area, and a GCP area which are arranged successively radially inwardly from the outermost circumferential zone to the innermost circumferential zone. The GCP area is an area in which additional information and address information are recorded, and in which pit patterns are represented by gray codes. The information recorded in the GCP area can be read even in a seek mode. The CTL area is an area in which information indicative of the medium type is recorded, and the TEST area is an area for writing data therein on a trial basis.

FIG. 5 shows, by way of example, a specific format of the optical disk 4 shown in FIG. 4. In FIG. 5, the GCP area in the uppermost row corresponds to the GCP area on the outermost circumferential zone of the optical disk 4 shown in FIG. 4, and the bands and areas arranged succes-

sively from the uppermost row toward the lowermost row correspond respectively to the areas arranged successively radially inwardly from the outermost circumferential zone to the innermost circumferential zone on the optical disk 4 shown in FIG. 4.

In this example, the optical disk 4 is a zone CAV disk. Therefore, as shown in FIG. 5, the data clock frequency varies from zone to zone.

FIGS. 6A, 6B, and 6C show, by way of example, a sector format of the optical disk 4. The contents of one sector are illustrated in FIGS. 6A, 6B, and 6C.

In FIGS. 6A, 6B, and 6C, i denotes a code word ("line" in FIGS. 6A, 6B, and 6C), and j denotes a byte. The solid-line arrow represents the direction in which data are written. Data indicated by D0 ~ D2047 represent user data, data indicated by (P1, P2) ~ (P35, P36) represent parity data with respect to the user data D0 ~ D127, ··· D1920 ~ D2047 indicated respectively by i = 130 ~ 123, ··· i = 10 ~ 3, data indicated by (Q1, Q2) represent parity data with respect to the parity data P1 ~ P36, data indicated by (Q3, Q4) represent parity data with respect to the parity data P1 ~ P36 and the parity data (Q1, Q2), and data indicated by CRC1 ~ CRC8 represent error-checking parity data with respect to the user data D0 ~ D2047.

Data indicated by (E1, 1) ~ (E16, 16) represent parity data of the Reed-Solomon code with respect to the user data D0 ~ D2047 indicated respectively by j = 0 ~ j =

15, the parity data P1 ~ P36, and the parity data CRC1 ~ CRC8. Specifically, the parity data j = 0 composed of the parity data (E1, 1) ~ (E1, 16) are parity data with respect to the data D0, D16, ··· D2032, and the data indicated by j = 0, i = 130 ~ 0, and the data indicated by j = 1, i = - 1 ~ - 16 composed of the parity data (E2, 1) ~ (E2, 16) are parity data with respect to the data indicated by j = 1, i = 130 ~ 0. Similar parity data are given to the other lines.

As described above with reference to FIGS. 6A, 6B, and 6C, if Reed-Solomon codes are constructed with respect to the data of the lines indicated by i = 147 ~ - 16, each of the distances is 17. Therefore, as can be seen from Table 1 above, up to 8 successive errors can be detected and corrected, but 9 or more successive errors cannot be corrected.

In this example, the parity data P1 ~ P36 as the second ECC for error checking and correction with respect to the data indicated by i = 130, j = 0 ~ i = 3, j = 15, i = 0, j = 15 ~ i = - 16, j = 15 are generated and used when data are reproduced.

Since the parity data (E1, 1) ~ (E16, 16) each have a vertical length of 147 bytes, the data length in the vertical direction of the user data D0 ~ D2047 to which the parity data are added is of 131 bytes, and the data length in the vertical direction of the parity data is of 16 bytes, the distance is 17, and hence they make up a (147, 131, 17)

Reed-Solomon code. One code word is of one byte. As described above, one sector is of 16 bytes × 147 = 2352 bytes.

The pattern of 7 lines - 8 lines - 7 lines with respect to the data of the sector shown in FIGS. 6A, 6B, and 6C will be described with reference to FIG. 7.

As can be seen from FIG. 7, parity data P1, P2 are generated with respect to all the data composed of 7 lines ranging from i = 130 to 124 shown in FIGS. 6A, 6B, and 6C, parity data P3, P4 are generated with respect to all the data composed of 8 lines ranging from i = 123 to 116 shown in FIGS. 6A, 6B, and 6C, and parity data P5, P6 are generated with respect to all the data composed of 7 lines ranging from i = 115 to 109 shown in FIGS. 6A, 6B, and 6C. Similarly, parity data are generated successively in the order of 7 lines, 8 lines, and 7 lines.

Upon generation of the parity data P1 ~ P40, three sets of Reed-Solomon codes composed of (114, 112, 3), (130, 128, 3), and (114, 112, 3) are successively produced.

According to this example, as described above, when data are recorded on the optical disk 4, parity data as the first ECC for error-correcting the data, parity data as the CRC for checking the data, and the parity data as the second ECC are generated in the pattern of 7 lines - 8 lines - 7 lines. If the optical disk 4 comprises a read-only disk, only the parity data as the second ECC are recorded in a particular area in an (n+1)th sector following an nth sector on the optical disk 4.

There is a possibility for uncorrectable data to be produced depending on the manner in which a burst of errors occurs upon reproduction of data. The reasons for such a possibility, and a procedure of coping with such a burst of errors will be described below.

FIG. 8 shows how to process a burst of successive errors which occurs in a certain sector.

In FIG. 8, the reference characters SEC represent a sector, and the reference characters SEC' represent details of the sector. The sector SEC, SEC' is based on the use of the pattern of 7 lines - 8 lines - 7 lines which has been described above with reference to FIG. 7. Groups of data composed of 7 lines and 8 lines will hereinafter referred to as blocks.

It is assumed that all the data contained in an area, shown hatched, in the sector SEC shown in FIG. 8 suffer a burst of errors. When such a burst of errors occurs in the sector SEC, it cannot be detected using the parity data LDC as the first ECC because the parity data LDC as the first ECC can detect up to errors of 8 bytes since its distance d is "17". However, errors in a certain block can be detected using the parity data P1 ~ P40 as the second ECC, and can be erasure-corrected by regarding the block containing the errors as being erased. For the pattern of 7 lines - 8 lines - 7 lines, the data that can be erasure-corrected are a maximum of 15 lines when the burst of errors extends exactly over the 7 lines and the 8 lines. For a pattern

composed of only 8 lines, the data that can be erasure-corrected are composed of 15 lines.

If the burst of errors extends over the 7-line block, the 8-line block, and the 7-line block, is composed of 11 lines, then it is necessary that the data of 22 lines (= 7 + 8 + 7 lines) be erasure-corrected. In this case, the data cannot be erasure-corrected even with the parity data P1 ~ P40 as the second ECC.

According to the present invention, it is possible to correct such a burst of errors that extends over 3 successive blocks, e.g., the 7-line block, the 8-line block, and the 7-line block. In the above example, specifically, the errors are detected using the parity data P1 ~ P40 as the second ECC, and thereafter, 8 lines are erasure-corrected using the parity data LDC as the first ECC by regarding the central 8 lines of data as being erased, and the errors are detected and corrected with the remaining 4 bytes. Alternatively, the errors are detected using the parity data P1 ~ P40 as the second ECC, and thereafter, (8+L) lines are erasure-corrected using the parity data LDC as the first ECC by regarding the central 8 lines of data and the N lines of data, above and below the central 8 lines of data, as being erased, and the errors are detected and corrected with the remaining M bytes. The patterns of the above error correction are given below.

8-line erasure correction and 4-line detection correction ...12 lines,

10(8 + 1 line, above and below)-line erasure correction and 3-line detection correction ···13 lines,

12(8 + 2 lines, above and below)-line erasure correction and 2-line detection correction ···14 lines,

14(8 + 3 lines, above and below)-line erasure correction and 1-line detection correction ···15 lines, and

16(8 + 4 lines, above and below)-line erasure correction ···16 lines.

If the central block is composed of 7 lines, the patterns of the error correction are as follows:

7-line erasure correction and 4-line detection correction ···11 lines,

9(7 + 1 line, above and below)-line erasure correction and 3-line detection correction ···12 lines,

11(7 + 2 lines, above and below)-line erasure correction and 2-line detection correction ···13 lines,

13(7 + 3 lines, above and below)-line erasure correction and 1-line detection correction ···14 lines, and

15(7 + 4 lines, above and below)-line erasure correction ···15 lines.

Any of the above patterns is based on the assumption that the distance d is "17" and the data that can be corrected do not exceed "17" lines.

FIG. 9 shows how to process a plurality of bursts of errors occur in a sector.

In FIG. 9, the reference characters SEC represent details of a sector. The sector SEC is based on the use of the pattern of 7 lines - 8 lines - 7 lines which has been described above with reference to FIG. 7.

In the example shown in FIG. 9, a burst of errors in excess of 8 lines occurs in a position which contains a block of 8 lines, and bursts of errors occur in respective two positions each in a block of 7 lines, both spaced from the position in which the burst of errors in excess of 8 lines occurs. Therefore, three bursts of errors occur in spaced positions, respectively.

When three bursts of errors occur in spaced positions, respectively, the errors are detected using the parity data P1 ~ P40 as the second ECC, and if the number of error flags obtained as a result of the error detection is "3" and the error flags are detected as being successive, then it is assumed that three bursts of errors occur in spaced positions, respectively, and the data of any one of the blocks are regarded as being erased and hence erasure-corrected, and the errors in the data in the other blocks are detected and corrected.

In this example, the data in the block of 8 lines suffering the burst of errors are regarded as being erased, and subjected to 8-line erasure correction, and the data in the two blocks each of 7 lines suffering the other bursts of errors are subjected to 4-line detection correction.

The blocks which contain bursts of errors may not comprise 3 successive blocks, but may comprise 2 successive blocks and 1 independent block.

FIGS. 10 through 13 show a process of operation of the controller shown in FIG. 3, for processing data upon reproduction thereof by the optical disk drive shown in FIG. 1. The process of operation of the controller for processing data upon reproduction thereof will be described below with reference to FIGS. 10 through 12 as well as FIGS. 1 through 3. The flowchart shown in FIG. 10 contains subroutines SUB1 ~ SUB3. These subroutines SUB1 ~ SUB3 are included for illustrative purpose only, and will not be generated as subroutines in an actual program.

It is determined in a step S1 whether there is a command or not, i.e., whether a command composed of a sector number, sector length data, etc. is supplied from the host computer 3 to the controller 2 through the input/output terminal io1, the interface 71, and the input/output port 64. If "YES", then control goes to a step S2.

Sectors in a requested range are successively read in the step S2. Actually, however, one sector is read each time the step S2 is executed. Specifically, the CPU 60 of the controller 44 supplies a request signal through the output terminal 73 to the reading/writing circuit 38. Data of a sector are successively read from the optical disk 4 until the sector length indicated by the host computer 3 is reached. The data read from the optical disk 4 are supplied

through the reading/writing circuit 38 and the input terminal 65 to the switch 66. The CPU 66 supplies a switching control signal to the switches 66, 69 to connect the movable contacts "c" to the fixed contacts "a" thereof. The reproduced data supplied from the switch 66 are supplied through the switch 66 to the decoder 67. Then, control proceeds to a step S3.

In the step S3, errors are detected and corrected using the LDC. Specifically, the CPU 60 instructs the decoder 67 to detect and correct errors using the parity data (E1, 1) ~ (E16, 16). The decoder 67 now detects and corrects errors in the data D0 ~ D2047. Then, control proceeds to a step S4.

It is determined in the step S4 whether the error correction is OK or not, i.e., whether errors have been corrected or not. If "YES", then control goes to a step S5, and if "NO", control goes to a step S7.

It is determined in the step S5 whether CRC checking is OK or not, i.e., whether an error is detected by CRC checking or not. If "YES", then control goes to a step S6, and if "NO", control goes to a step S9.

It is determined in the step S6 whether the processing indicated by the command has been finished or not, i.e., whether the reading of all the sectors in the range requested by the command inputted in the step S1 has been finished or not. If "YES", then the processing sequence

comes to an end, and if "NO", then control goes back to the step S2.

In the step S7, errors are detected according to the second ECC, and flags are added. Specifically, the CPU 60 instructs the decoder 67 to detect errors using the parity data P1 ~ P40. The decoder 67 now detects errors in the data D0 ~ D2047 block by block, and generates error flags. Specifically, the decoder 67 effects error detection on each block. If there are errors in a block, then the decoder 67 regards the block as being erased, and adds a flag indicating that the block is erased. For example, the decoder 67 detects whether there are errors or not using the parity data P1, P2 with respect to a block indicated by i = 130 ~ 124. If there are errors in that block, then the decoder 67 adds a flag indicating that the block suffers a burst of errors. The decoder 67 effects such processing on all the blocks. Then, control proceeds to a step S8.

It is determined in the step S8 whether the number of error flags is ≥ 4 or 0. If "YES", then control goes to a step S9, and if "NO", then control jumps to a step S11. In this example, since errors cannot be corrected if bursts of errors occur in four or more blocks in one sector, the step S8 determines whether the number of error flags is at least "4". An error is indicated when the number of error flags is "0" because when the number of error flags is "0" after the error detection using the parity data P1 ~ P40 as the second ECC regardless of the detection of an error using

the parity data (E1, 1) ~ (E16, 16), either error detecting process is in error.

An error message is displayed in the step S9, and then control goes to a step S10. Specifically, in the step S9, the CPU 60 supplies message data stored in the ROM 62 to the host computer 3, which displays a message image on the display of the host computer 3. The message image may contain the following message:

"BECAUSE ERROR HAS OCCURRED, THE SECTOR IS BEING READ AGAIN."

In the step S10, the re-reading of the sector is set. Thereafter, control goes back to the step S6. In the step S10, the CPU 60 supplies a request signal indicating the re-reading of the sector to the reading/writing circuit 38 through the output terminal 73. The data of the sector are read again from the optical disk 4.

It is determined in the step S11 whether the number of error flags is "3" or not. If "YES", then control proceeds to a step S12, and if "NO", then control goes to a step S100 which is a subroutine SUB2. The number "3" used as the criterion in the step S11 is the number of blocks which contain bursts of errors in one sector, and is equal to the maximum number of errors that can be corrected.

In the step S12, it is determined whether the error flags are 3 successive error flags or not, i.e., whether the blocks to which the 3 error flags are added are 3 successive blocks or not. If "YES", then control goes to

a step S50 which is a subroutine SUB1, and if "NO", then control goes to a step S150 which is a subroutine SUB3. Whether the error flags are 3 successive error flags or not is determined in order to determine whether the blocks which contain bursts of errors are successive or separate for effecting subsequent processes optimum for both cases.

FIG. 11 illustrates the subroutines SUB1, SUB2 shown in FIG. 10. First, the subroutine SUB1 will be described below.

If "YES" in the step S12 shown in FIG. 10, control jumps to a step S51 of the subroutine SUB1. In the step S51, the central block and one line, closer to the central block, in each of the blocks before and after the central block are regarded as being erased, and errors are erasure-corrected with the LDC, i.e., the first ECC indicated by $i = -13 \sim -16$, and errors are detected and corrected. Then, control proceeds to a step S52. In the step S51, the central block and 1 line above and below the central block are regarded as being erased, and errors are erasure-corrected, and errors are detected and corrected using the remaining distance. If the central block is composed of 7 lines, then a total of 9 lines composed of the 7 lines and 1 line above and below the 7 lines are erasure-corrected for 9 bytes, and errors are detected and corrected using the remaining distance. In this case, up to 3 bytes can be detected and corrected. If the central block is composed of 8 lines, then a total of 10 lines composed of the 8 lines and

1 line above and below the 8 lines are erasure-corrected for 10 bytes, and errors up to 3 bytes are detected and corrected using the remaining distance.

It is determined in the step S52 whether the error correction is OK or not, i.e., whether errors have been corrected or not. If "YES", then control leaves the subroutine SUB1 and goes back to the step S5 in the flowchart shown in FIG. 10, and if "NO", control goes to a step S53.

An error message is displayed in the step S53, and then control goes to a step S54. Specifically, in the step S53, the CPU 60 supplies message data stored in the ROM 62 to the host computer 3, which displays a message image on the display of the host computer 3. The message image may contain the following message:

"BECAUSE UNCORRECTABLE BURST OF ERRORS HAS OCCURRED, THE SECTOR IS BEING READ AGAIN."

In the step S54, the re-reading of the sector is set. Thereafter, control goes back to the step S6 in the flowchart shown in FIG. 10. In the step S54, the CPU 60 supplies a request signal indicating the re-reading of the sector to the reading/writing circuit 38 through the output terminal 73. The data of the sector are read again from the optical disk 4.

The subroutine SUB2 will be described below.

If "NO" in the step S11 shown in FIG. 10, control jumps to a step S101 of the subroutine SUB2. In the step S101, errors are erasure-corrected with the LDC and errors

are detected and corrected. Then, control proceeds to a step S102. The step S101 is executed if the number of error flags is "2" or "1", i.e., either if a burst of errors occurs over two blocks, or if bursts of errors occur respectively in two separate blocks, or if a burst of errors occurs in one block. In the step S101, therefore, the data of one block or two blocks are regarded as being erased, and errors are erasure-corrected. With the remaining distance, errors are checked if two blocks are erased, and errors are detected and corrected if one block is erased.

It is determined in the step S102 whether the error correction is OK or not, i.e., whether errors have been corrected or not. If "YES", then control leaves the subroutine SUB2 and goes back to the step S5 in the flowchart shown in FIG. 10, and if "NO", control goes to a step S103.

An error message is displayed in the step S103, and then control goes to a step S104. Specifically, in the step S103, the CPU 60 supplies message data stored in the ROM 62 to the host computer 3, which displays a message image on the display of the host computer 3. The message image may contain the following message:

"CORRECTABLE BURST OF ERRORS HAS BEEN CORRECTED. HOWEVER, THE SECTOR IS BEING READ AGAIN BECAUSE OF ERROR IN ERROR CHECKING."

In the step S104, the re-reading of the sector is set. Thereafter, control goes back to the step S6 in the

flowchart shown in FIG. 10. In the step S104, the CPU 60 supplies a request signal indicating the re-reading of the sector to the reading/writing circuit 38 through the output terminal 73. The data of the sector are read again from the optical disk 4.

FIGS. 12 and 13 illustrate the subroutine SUB3 shown in FIG. 10.

If the error flags are not 3 successive error flags in the step S12 of the flowchart shown in FIG. 10, then control goes to a step S151 of the subroutine SUB3 shown in FIG. 12. The flowchart illustrated in FIGS. 12 and 13 is based on the assumption that bursts of errors occur in three blocks, with at least one of the blocks being spaced from the other two blocks.

If 8 bytes are regarded as being erased, then errors up to 4 bytes can be detected and corrected with the remaining distance.

In the step S151, the first block, i.e., the uppermost block in FIG. 11, is regarded as being erased, and errors are erasure-corrected, and errors are detected and corrected in the second and third blocks. In the second and third blocks, errors up to 4 bytes can be detected and corrected.

It is determined in a step S152 whether the error correction is OK or not. If "YES", then control goes to the step S5 of the flowchart shown in FIG. 10, and if "NO", then control proceeds to a step S153. In the step S153, the sec-

ond block, i.e., the middle block shown in FIG. 11, is regarded as being erased, and errors are erasure-corrected, and errors are detected and corrected in the first and third blocks. In the first and third blocks, errors up to 4 bytes can be detected and corrected.

It is determined in a step S154 whether the error correction is OK or not. If "YES", then control goes to the step S5 of the flowchart shown in FIG. 10, and if "NO", then control proceeds to a step S155. In the step S155, the third block, i.e., the lowermost block shown in FIG. 11, is regarded as being erased, and errors are erasure-corrected, and errors are detected and corrected in the first and second blocks. In the first and second blocks, errors up to 4 bytes can be detected and corrected.

It is determined in a step S156 whether the error correction is OK or not. If "YES", then control goes to the step S5 of the flowchart shown in FIG. 10, and if "NO", then control proceeds to a step S160.

In the step S160, it is determined whether there are 2 successive blocks, i.e., whether two of the three blocks are successive blocks or not. If "YES", then control goes to a step S161, and if "NO", then control jumps to a step S166.

In the step S161, data which correspond to one block and extend over two blocks are regarded as being erased, and errors in the remaining data are detected and corrected. Errors up to 4 bytes can be detected and cor-

rected in the data in the two blocks which are not regarded as being erased. Thereafter, control goes to a step S162.

The step S162 determines whether errors have been detected or not. If "YES", then control goes to a step S163. If "NO", then control goes to a step S164.

In the step S163, the errors are corrected. Then, control proceeds to a step S165.

In the step S164, the position of the data which correspond to one block and are regarded as being erased is shifted one line. Then, control goes back to the step S161. In the step S164, the position of the data is shifted one line because there is an instance where errors may be corrected by shifting the position of the block that is regarded as being erased.

It is determined in the step S165 whether the error correction is OK or not. If "YES", then control goes to the step S5 of the flowchart shown in FIG. 10, and if "NO", then control proceeds to a step S166.

An error message is displayed in the step S166, and then control goes to a step S167. Specifically, in the step S166, the CPU 60 supplies message data stored in the ROM 62 to the host computer 3, which displays a message image on the display of the host computer 3. The message image may contain the following message:

"CORRECTABLE BURST OF ERRORS HAS BEEN CORRECTED. HOWEVER, THE SECTOR IS BEING READ AGAIN BECAUSE OF ERROR IN ERROR CORRECTION."

In the step S167, the re-reading of the sector is set. Thereafter, control goes back to the step S6 in the flowchart shown in FIG. 10. In the step S167, the CPU 60 supplies a request signal indicating the re-reading of the sector to the reading/writing circuit 38 through the output terminal 73. The data of the sector are read again from the optical disk 4.

The re-reading of the sector may be carried out only in the step S10, and if an error occurs in other steps, re-reading of the sector may not be carried out, but the processing may be ended. For example, if no recovery from an error can be made when the sector is re-read in the steps S54, S104, S167, then since the optical disk drive may possibly have failed or a considerable burst of errors may possibly have occurred, the processing may suffer looping, resulting in a possibility of failure to remove the optical disk 4. Alternatively, if an error occurs even after the re-reading of the sector has been carried out three times, then the optical disk drive may supply the host computer 3 with message data representing a message "OPTICAL DISK WILL BE DISCHARGED BECAUSE OF POSSIBILITY OF UNCORRECTABLE BURST OF ERRORS OR FAILURE OF OPTICAL DISK DRIVE.", and then discharge the optical disk 4.

FIG. 14 shows a level detector according to another embodiment of the present invention, which is necessary to detect the length and position of a burst of errors

by detecting an RF level instead of parity data as the second ECC used in the previous embodiment.

The drive controller shown in FIG. 2 may include a level detecting circuit 200 connected to the selector/clamp circuit 33, the data system clock generator 35, and the controller 44. The level detecting circuit 200 may have an internal structure as shown in FIG. 14.

In FIG. 14, the level detecting circuit 200 has an input terminal 201 for being supplied with an RF signal, before being clamped, from the selector/clamp circuit 33, an input terminal 202 for being supplied with the data system clock signal from the data system clock generator 35, and an output terminal 207 connected to the controller 44. The level detecting circuit 200 also has an averaging circuit 203 for averaging the RF signal supplied through the input terminal 201 in timed relation to the data system clock signal supplied through the input terminal 202, producing a DC voltage signal. The DC voltage signal generated by the averaging circuit 203 is supplied to a comparator 204, which compares the DC voltage signal with a reference voltage from a reference power supply 205 connected to the comparator 204. In a sample servo system, it is easy to obtain, in advance, a representative level upon a reduction of the RF level which is caused by a tracking error due to the dropout of wobble pits that are formed one byte per about 20 bytes of data. Therefore, the reference voltage from the refer-

ence power supply 205 should be of a level lower than the RF level in a condition free of tracking errors.

The comparator 204 outputs an error signal of "1" when the DC voltage signal from the averaging circuit 203 is smaller than the reference voltage from the reference power supply 205. The error signal is supplied to a delay circuit 206, which delays the error signal by a period of time corresponding to the processing time for main signals, and supplies the delayed signal to the controller 44 when errors are detected in reproduced data.

FIG. 15 shows a controller according to the other embodiment of the present invention, for detecting the length and position of a burst of errors by detecting an RF level instead of parity data as the second ECC. The controller shown in FIG. 15 may be incorporated in a drive controller which differs from the drive controller shown in FIG. 2 except that the level detecting circuit 200 is included. The controller shown in FIG. 15 is similar to the controller shown in FIG. 3, and those parts shown in FIG. 15 which are identical to those shown in FIG. 3 will not be described in detail below.

As shown in FIG. 15, the controller has an input/output terminal 65 connected to the reading/writing circuit 38 shown in FIG. 2 and a movable contact "c" of a switch 66. The switch 66 has a fixed contact "a" connected to an input terminal of a decoder 300, and another fixed

contact "b" connected to an output terminal of an encoder 301.

The decoder 300 has a data output terminal connected to a fixed terminal "a" of a switch 69, and the encoder 301 has an input terminal connected to another fixed terminal "b" of the switch 69. The switch 69 has a movable contact "c" connected to an input/output terminal of the buffer 70 whose another input/output terminal is connected to an input/output terminal of the interface 71. The interface 71 has another input/output terminal connected through the input/output terminal io1 to the input/output terminal of the host computer 3 shown in FIG. 1.

The decoder 300 effects error detection and error correction on reproduced data supplied through the switch 66, and effects error correction based on the result of detection by a burst detecting circuit 302 if there is a request from the CPU 60 through the input/output port. The decoder 300 comprises a RAM 300a having a storage capacity of 2 sectors and a RAM controller 300b for controlling reproduced data stored in the RAM 300a to effect error correction using the LDC, error checking using the CRC, and error correction using the parity data of the LDC upon occurrence of a burst of errors for which the error correction and the error checking are ineffective, based on the result of detection by the burst detecting circuit 302.

The encoder 301 comprises a RAM 301a having a storage capacity of 2 sectors and a RAM controller 301b for

controlling input data stored in the RAM 301a to generate parity data as the first ECC, parity data as the CRC, and add these parity data.

The encoder 301 adds the parity data for error detection, the parity data as the CRC for error correction, and parity data as the first ECC to data which have been transferred from the host computer 3, stored into the buffer 70 through the interface 71, read from the buffer 700, and supplied through the switch 69 for being recorded.

In the optical disk drive shown in FIG. 1, the parity data for error checking and the parity data for error correction can written in writable areas on a magnetooptical disk, a write-once disk, and a partial disk, and hence both the encoder and the decoder are involved for recording of the data on these disks. For reading data from a read-only area on a read-only optical disk or a partial disk, the encoder is not involved, but only the decoder is involved because the parity data and other data are recorded when the disk is manufactured.

The burst detecting circuit 302 detects the magnitude and position of a burst of errors when it occurs, based on the result of detection by the level detecting circuit 200 shown in FIG. 14, and supplies a signal indicative of the detected magnitude and position through the input/output port 64 to the decoder 300.

Major aspects of operation of the controller shown in FIG. 15 will be described below.

To reproduce recorded data from the optical disk 4, the CPU 60 supplies a switching control signal through the input/output port 64 to the switches 66, 69 to connect the movable contacts "c" of the switches 66, 69 to the fixed contacts "a" thereof. Reproduced data read from the optical disk 4 and supplied through the reading/writing circuit 38, the input/output terminal 65, and the switch 66 are supplied to the decoder 300. After errors have been detected and corrected in the reproduced data by the decoder 300, the reproduced data are supplied through the switch 69, the buffer 70, the interface 71, and the input/output port io1 to the host computer 3.

At this time, the decoder 300 effects error correction on the data of one of the two sectors stored in the RAM 67a, using the parity data as the first ECC, and effects error checking on the same data using the parity data as the CRC. If a burst of errors occurs, making it impossible to effect such error correction and error checking, then the decoder 300 recognizes the magnitude and position of the burst of errors based on the result of detection by the burst detecting circuit 302, and thereafter effects error correction on the data of the sector using the parity data as the first ECC, and effects error checking on the data of the sector using the parity data as the CRC. After the processing of the reproduced data is finished, the decoder 300 outputs the data of the sector, and supplies a signal indicating the outputting of the data through the in-

put/output port 64 and the bus 61 to the CPU 60. The CPU 60 then instructs the reading/writing circuit 38 shown in FIG. 2 to reproduce a next sector. All the data of the above sector are supplied to the buffer 70, after which reproduced data from the next sector read from the optical disk 4 are supplied to the RAM 300a.

FIG. 16 shows a sequence of operation of the controller shown in FIG. 15, for detecting a burst of errors, upon reproduction of data, by detecting an RF level instead of the second ECC. The flowchart shown in FIG. 16 corresponds to the flowchart shown in FIG. 10, and contains subroutines that are identical to those shown in FIGS. 11 through 13. Therefore, these subroutines will be omitted from illustration. Those steps shown in FIG. 16 which are identical to those shown in FIG. 10 are denoted by identical step numbers, and will not be described in detail below.

If the errors cannot be corrected as determined in the step S4, then control goes to a step S200 which determines the lengths and positions of bursts of errors from the detected RF level. Thereafter, control proceeds to a step S201. In the step S200, the burst detecting circuit 302 shown in FIG. 15 determines the number, lengths, and positions of bursts of errors in one sector based on the result of detection by the level detecting circuit 200 shown in FIG. 14.

It is determined in the step S201 whether the error correction is OK or not. If "YES", then control goes

to the step S8, and if "NO", control goes to a step S202. In the step S202, errors are determined as being uncorrectable if the number of bursts of errors in one sector is at least "4".

The step S202 determines whether the number of bursts of errors is "3" or not. If "YES", then control proceeds to a step S203, and if "NO", then control goes to the step S100 which is the subroutine SUB2. The number "3" used as the criterion in the step S202 is essentially the same as the number of error flags in the previous embodiment.

In the step S203, it is determined whether the bursts of errors are 3 successive bursts of errors or not. If "YES", then control goes to the step S150 which is the subroutine SUB3, and if "NO", then control goes to the step S50 which is the subroutine SUB1.

The processing in the subroutines SUB1, SUB2, SUB3 is the same as that in the previous embodiment. The rate of error correction can be increased by not using the second ECC. In this embodiment, the parity data P1 ~ P40 as the second ECC are recorded in the same manner as with the previous embodiment. When they are used upon reproduction of data, the number of bytes that can be detected and corrected using the LDC can be increased up to 16 at maximum.

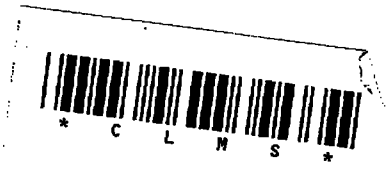
According to the present invention, data containing successive errors that cannot be corrected with an intersymbol minimum distance of first error-processing data can be recovered. Therefore, data which contain an uncor-

rectable burst of errors can be recovered through a simple process, resulting in an increased error-correcting capability for reliable data reproduction.

Furthermore, the present invention makes it possible to increase the error-correcting capability in the event of errors occurring over a plurality of blocks.

If errors occur over a plurality of blocks, then the data of at least one, which is substantially central, of the blocks and the data of blocks adjacent to the block are regarded as being erased, and errors are corrected using the first error-processing data. Consequently, the error-correcting capability in the event that errors occur over a plurality of blocks is increased. Therefore, errors can be corrected efficiently for reproducing recorded data well, and the recording capacity of a recording medium is prevented from being lowered.

Although certain preferred embodiments of the present invention have been shown and described in detail, it should be understood that various changes and modifications may be made therein without departing from the scope of the appended claims.



What is claimed is:

1. A method of recording and reproducing data, comprising the steps of:

(a) generating first error-processing data with respect to a predetermined amount of data, and generating second error-processing data with respect to each of a plurality of blocks produced by dividing said predetermined amount of data;

(b) generating data of record units from said predetermined amount of data, said first error-processing data, and said second error-processing data;

(c) recording said data of record units on a recording medium;

(d) reproducing said data of record units on said recording medium;

(e) correcting errors in said predetermined amount of data in the reproduced data of record units with said first error-processing data with respect to each of said record units;

(f) if errors cannot be corrected in the step (e), at least detecting errors in said predetermined amount of data in each of said blocks with said second error-processing data; and

(g) if errors are detected in N (N is a positive integer) successive blocks, regarding all data in at least one block which is not positioned at an end of the N succes-

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sive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data, thus producing reproduced data.

2. A method according to claim 1, wherein said second error-processing data generated in said step (a) comprise a plurality of parity data in a direction corresponding to the order of data reproduced from said recording medium, with respect to said predetermined amount of data.

3. A method according to claim 1, wherein said step (g) comprises the step of regarding all data in at least one block which is not positioned at an end of the N successive blocks and portions of data of blocks adjacent to said at least one block, as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data.

4. A method according to claim 1, wherein said step (g) comprises the step of, if errors are detected in two successive blocks, regarding data corresponding to one block and extending over said two successive blocks as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data, and the steps of, when the errors cannot be corrected, positionally shifting the data of one block which

is regarded as being erased, and correcting errors again with said first error-processing data.

5. A method of transmitting data, comprising the steps of:

(a) generating first error-processing data with respect to a predetermined amount of data, and generating second error-processing data with respect to each of a plurality of blocks produced by dividing said predetermined amount of data;

(b) generating transmission data of units from said predetermined amount of data, said first error-processing data, and said second error-processing data;

(c) transmitting said transmission said data of units;

(d) correcting errors in said transmission data of units which have been transmitted with said first error-processing data with respect to each of the transmitted units;

(e) if errors cannot be corrected in the step (d), at least detecting errors in the transmitted data in each of said blocks with said second error-processing data; and

(f) if errors are detected in N (N is an integer of at least 3) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting er-

rors in the predetermined amount of data in the transmitted units with said first error-processing data.

6. A method according to claim 5, wherein said second error-processing data generated in said step (a) comprise a plurality of parity data in a direction corresponding to the order of data which are transmitted, with respect to said predetermined amount of data.

7. A method according to claim 5, wherein said step (f) comprises the step of regarding all data in at least one block which is not positioned at an end of the N successive blocks and portions of data of blocks adjacent to said at least one block, as being erased, thereby correcting errors in the predetermined amount of data in the transmitted units with said first error-processing data.

8. A method according to claim 5, wherein said step (f) comprises the step of, if errors are detected in two successive blocks, regarding data corresponding to one block and extending over said two successive blocks as being erased, thereby correcting errors in the predetermined amount of data in the transmitted units with said first error-processing data, and the steps of, when the errors cannot be corrected, positionally shifting the data of one block which is regarded as being erased, and correcting errors again with said first error-processing data.



9. An apparatus for recording and reproducing data, comprising:

error-processing data generating means for generating first error-processing data with respect to a predetermined amount of data, and second error-processing data with respect to each of a plurality of blocks produced by dividing said predetermined amount of data;

record unit data generating means for generating data of record units from said predetermined amount of data, said first error-processing data, and said second error-processing data;

recording and reproducing means for recording said data of record units on a recording medium and reproducing said data of record units on said recording medium; and

error correcting means for correcting errors in said predetermined amount of data in the data of record units reproduced by said recording and reproducing means with said first error-processing data with respect to each of said record units, and if errors cannot be corrected, at least detecting errors in said predetermined amount of data in each of said blocks with said second error-processing data, and if errors are detected in N (N is a positive integer) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the

predetermined amount of data in the record units with said first error-processing data.

10. An apparatus according to claim 9, wherein said error-processing data generating means comprises means for generating as said second error-processing data a plurality of parity data in a direction corresponding to the order of data reproduced from said recording medium, with respect to said predetermined amount of data.

11. An apparatus according to claim 9, wherein said error correcting means comprises means for regarding all data in at least one block which is not positioned at an end of the N successive blocks and portions of data of blocks adjacent to said at least one block, as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data.

12. An apparatus according to claim 9, wherein said error correcting means comprises means for, if errors are detected in two successive blocks, regarding data corresponding to one block and extending over said two successive blocks as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data, and means for, when the errors cannot be corrected, positionally shifting the data of one

block which is regarded as being erased, and correcting errors again with said first error-processing data.

13. An apparatus for transmitting data, comprising:

error-processing data generating means for generating first error-processing data with respect to a predetermined amount of data, and second error-processing data with respect to each of a plurality of blocks produced by dividing said predetermined amount of data;

transmission data generating means for generating transmission data of units from said predetermined amount of data, said first error-processing data, and said second error-processing data;

transmitting means for transmitting said transmission said data of units; and

error correcting means for correcting errors in said transmission data of units which have been transmitted with said first error-processing data with respect to each of the transmitted units, and if errors cannot be corrected, at least detecting errors in the transmitted data in each of said blocks with said second error-processing data, and if errors are detected in N (N is an integer of at least 3) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the

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predetermined amount of data in the transmitted units with said first error-processing data.

14. An apparatus according to claim 13, wherein said error-processing data generating means comprises means for generating as said second error-processing data a plurality of parity data in a direction corresponding to the order of data which are transmitted, with respect to said predetermined amount of data.

15. An apparatus according to claim 13, wherein said error correcting means comprises means for regarding all data in at least one block which is not positioned at an end of the N successive blocks and portions of data of blocks adjacent to said at least one block, as being erased, thereby correcting errors in the predetermined amount of data in the transmitted units with said first error-processing data.

16. An apparatus according to claim 13, wherein said error correcting means comprises means for, if errors are detected in two successive blocks, regarding data corresponding to one block and extending over said two successive blocks as being erased, thereby correcting errors in the predetermined amount of data in the transmitted units with said first error-processing data, and means for, when the errors cannot be corrected, positionally shifting the data

of one block which is regarded as being erased, and correcting errors again with said first error-processing data.

17. A method of reproducing data, comprising the steps of:

(a) reproducing data of record units from a recording medium on which there are recorded a predetermined amount of data, first error-processing data generated with respect to said predetermined amount of data, and second error-processing data generated with respect to each of a plurality of blocks produced by dividing said predetermined amount of data, making up said data of record units;

(b) correcting errors in said predetermined amount of data in the reproduced data of record units with said first error-processing data with respect to each of said record units;

(c) if errors cannot be corrected in the step (b), at least detecting errors in said predetermined amount of data in each of said blocks with said second error-processing data; and

(d) if errors are detected in N (N is a positive integer) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data, thus producing reproduced data.

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18. A method according to claim 17, wherein said second error-processing data generated in said step (a) comprise a plurality of parity data in a direction corresponding to the order of data reproduced from said recording medium, with respect to said predetermined amount of data.

19. A method according to claim 17, wherein said step (d) comprises the step of regarding all data in at least one block which is not positioned at an end of the N successive blocks and portions of data of blocks adjacent to said at least one block, as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data.

20. A method according to claim 17, wherein said step (d) comprises the step of, if errors are detected in two successive blocks, regarding data corresponding to one block and extending over said two successive blocks as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data, and the steps of, when the errors cannot be corrected, positionally shifting the data of one block which is regarded as being erased, and correcting errors again with said first error-processing data.

21. A method of transmitting data, comprising the steps of:

(a) transmitting transmission data of units which are composed of a predetermined amount of data, first error-processing data generated with respect to said predetermined amount of data, and second error-processing data generated with respect to each of a plurality of blocks produced by dividing said predetermined amount of data;

(b) correcting errors in said transmission data in the units which are transmitted with respect to each of the transmitted units;

(c) if errors cannot be corrected in the step (b), at least detecting errors in said transmission data in each of said blocks with said second error-processing data; and

(d) if errors are detected in N (N is an integer of at least 3) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the transmitted units with said first error-processing data.

22. An apparatus for reproducing data, comprising:

reproducing means for reproducing data of record units from a recording medium on which there are recorded a predetermined amount of data, first error-processing data

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generated with respect to said predetermined amount of data, and second error-processing data generated with respect to each of a plurality of blocks produced by dividing said predetermined amount of data, making up said data of record units;

error correcting means for correcting errors in said predetermined amount of data in the data of record units reproduced by said reproducing means, with said first error-processing data with respect to each of said record units, and if errors cannot be corrected, at least detecting errors in said predetermined amount of data in each of said blocks with said second error-processing data, and if errors are detected in N (N is a positive integer) successive blocks, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data.

23. An apparatus for recording and reproducing data, comprising:

error-processing data generating means for generating first error-processing data with respect to a predetermined amount of data, and second error-processing data with respect to each of a plurality of blocks produced by dividing said predetermined amount of data;

record unit data generating means for generating data of record units from said predetermined amount of data, said first error-processing data, and said second error-processing data;

recording and reproducing means for recording said data of record units on a recording medium and reproducing said data of record units on said recording medium;

error detecting means for detecting an error status, in each of said blocks, of a reproduced signal indicative the data of record units which are reproduced by said recording and reproducing means, based on a video level of said reproduced signal; and

error correcting means for correcting errors in said predetermined amount of data in the data of record units reproduced by said recording and reproducing means, with said first error-processing data with respect to each of said record units, and if errors cannot be corrected with said first error-processing data with respect to each of said record units, determining blocks as errors based on the error status detected by said error detecting means, and when N (N is a positive integer) successive blocks are determined as errors, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data.

24. An apparatus for reproducing data, comprising:

reproducing means for reproducing data of record units from a recording medium on which there are recorded a predetermined amount of data, first error-processing data generated with respect to said predetermined amount of data, and second error-processing data generated with respect to each of a plurality of blocks produced by dividing said predetermined amount of data, making up said data of record units;

error detecting means for detecting an error status, in each of said blocks, of a reproduced signal indicative the data of record units which are reproduced by said reproducing means, based on a video level of said reproduced signal; and

error correcting means for correcting errors in said predetermined amount of data in the data of record units reproduced by said reproducing means, with said first error-processing data with respect to each of said record units, and if errors cannot be corrected, determining blocks as errors based on the error status detected by said error detecting means, and when N (N is a positive integer) successive blocks are determined as errors, regarding all data in at least one block which is not positioned at an end of the N successive blocks, as being erased, thereby correcting errors in the predetermined amount of data in the record units with said first error-processing data.