

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
19 September 2002 (19.09.2002)

PCT

(10) International Publication Number
WO 02/074024 A2

(51) International Patent Classification⁷: **H05K**

(21) International Application Number: PCT/US02/09203

(22) International Filing Date: 14 March 2002 (14.03.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/275,843 14 March 2001 (14.03.2001) US

(71) Applicant (for all designated States except US): **LEGACY ELECTRONICS, INC.** [US/US]; 1001 Calle Amancer, San Clemente, CA 92673 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **KLEDZIK, Kenneth** [US/US]; 22 Via Sonrisa, San Clemente, CA 92673 (US).

(74) Agents: **REED, Randall** et al.; Levin and Hawes, Suite 13, 384 Forest Ave., Laguna Beach, CA 92651 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

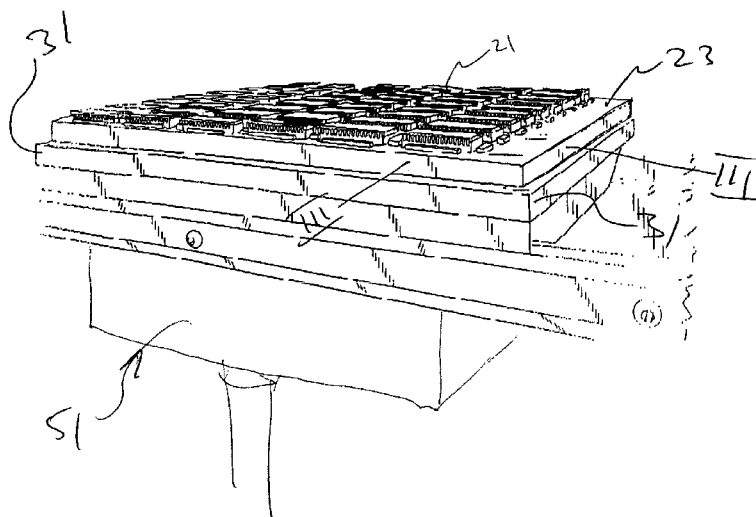
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A METHOD AND APPARATUS FOR FABRICATING A CIRCUIT BOARD WITH A THREE DIMENSIONAL SURFACE MOUNTED ARRAY OF SEMICONDUCTOR CHIPS



(57) Abstract: A method and apparatus for fabricating a three dimensional array of semiconductor chips is disclosed. The method uses a multistep fabrication process that automates the surface mounting of semiconductor chips with unique chip carriers to achieve the three dimensional array of chips. The method includes a step of depositing solder on a multitude of chip carriers at one time, placing the chip carriers with chips on a printed circuit board and then running the board with chips and carriers arranged in a three dimensional array through a single reflow oven to complete a single reflow process to permanently connect all of the components. The apparatus includes a unique chip carrier pallet and print fixture pedestal that works in combination to position the chips and carriers for automatic deposition of solder on a multitude of carriers at once and then position them for addition to the circuit board.



WO 02/074024 A2