

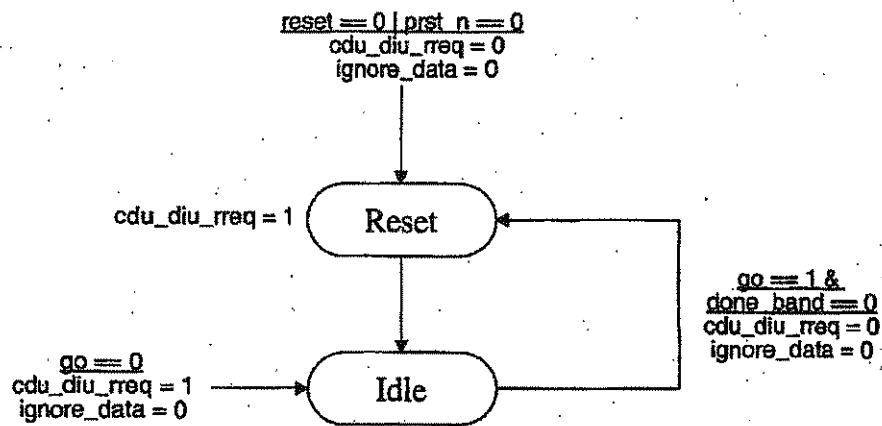


FIG. 1

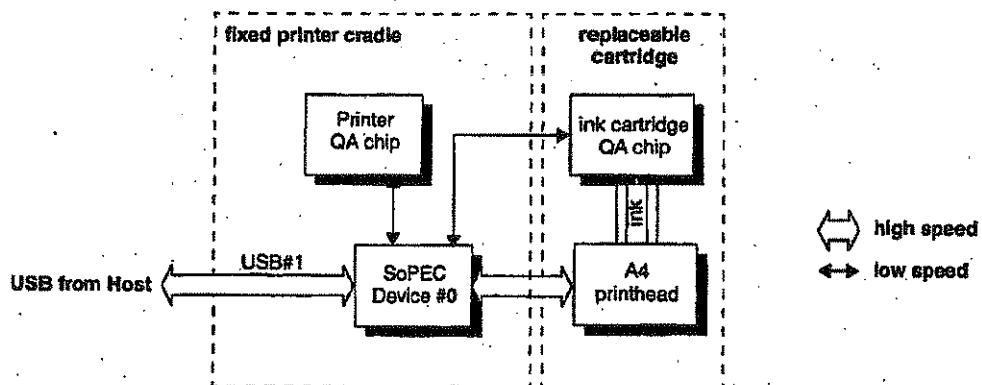


FIG. 2

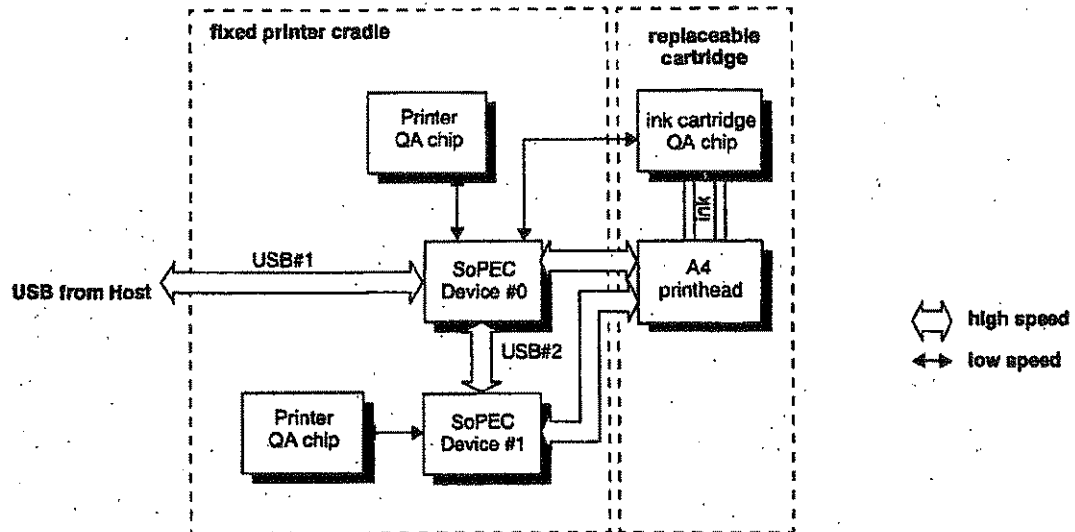


FIG. 3

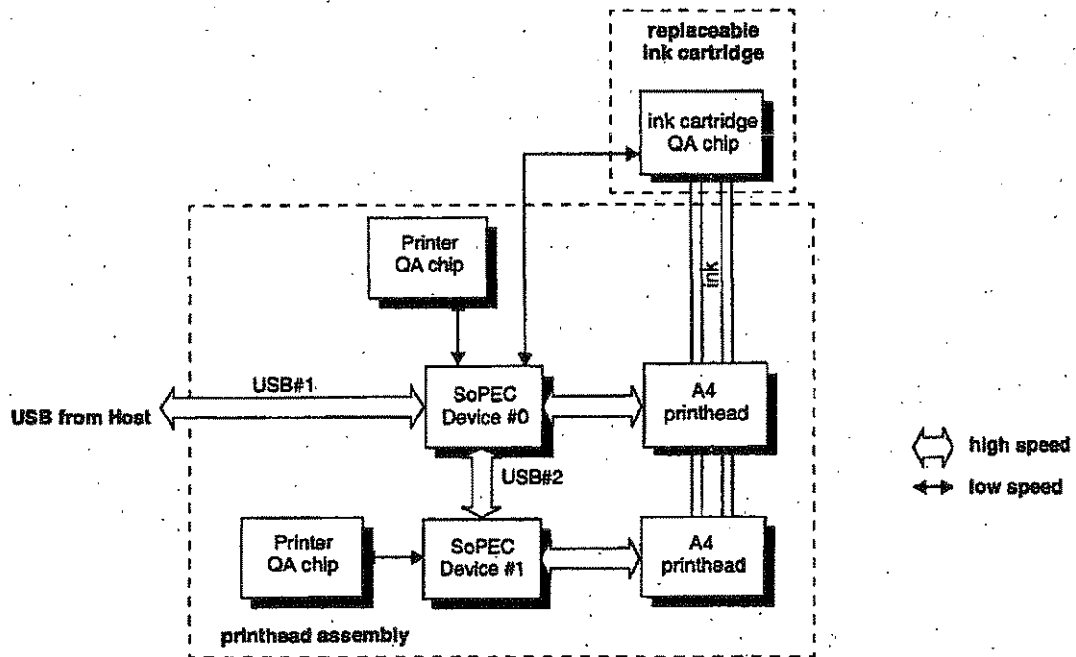


FIG. 4

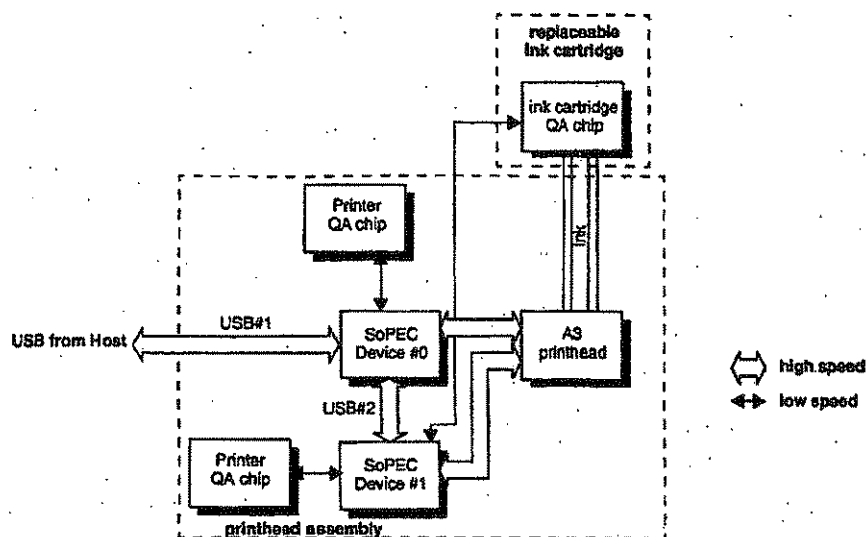


FIG. 5

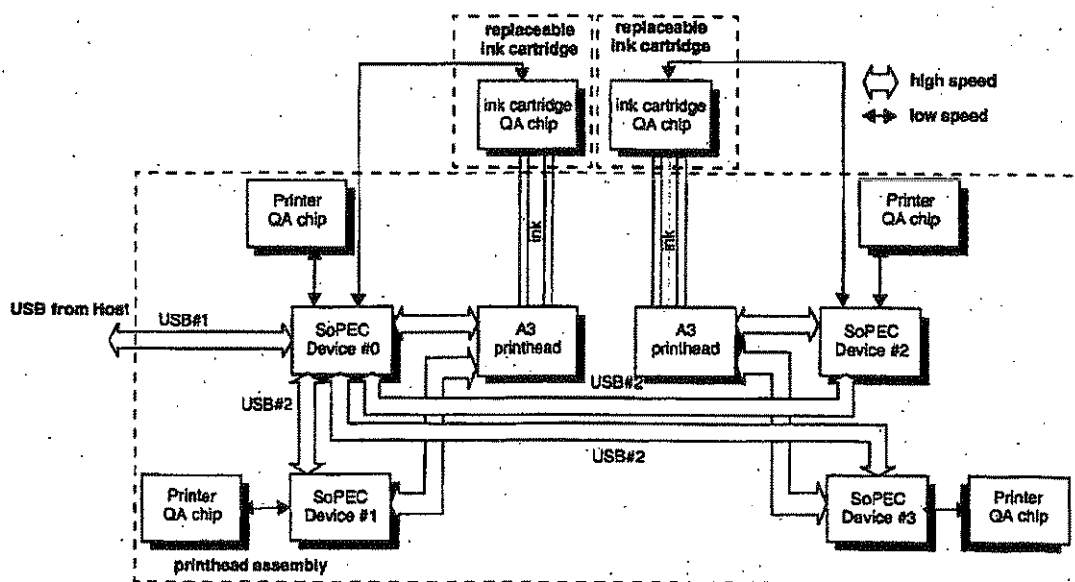


FIG. 6

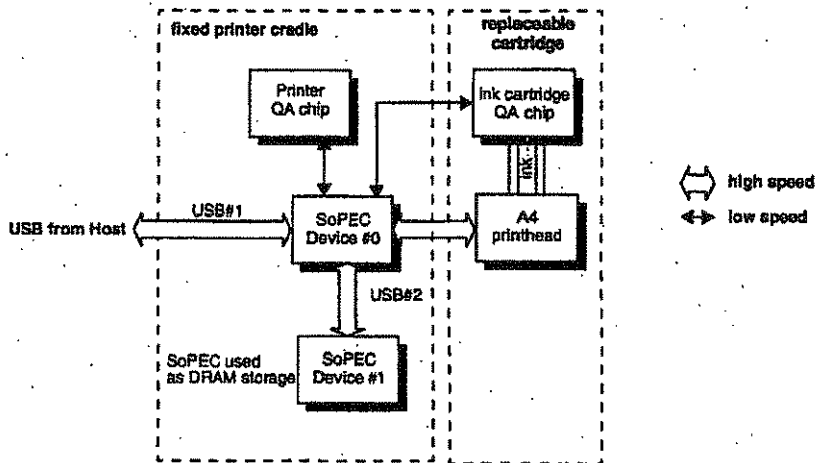


FIG. 7

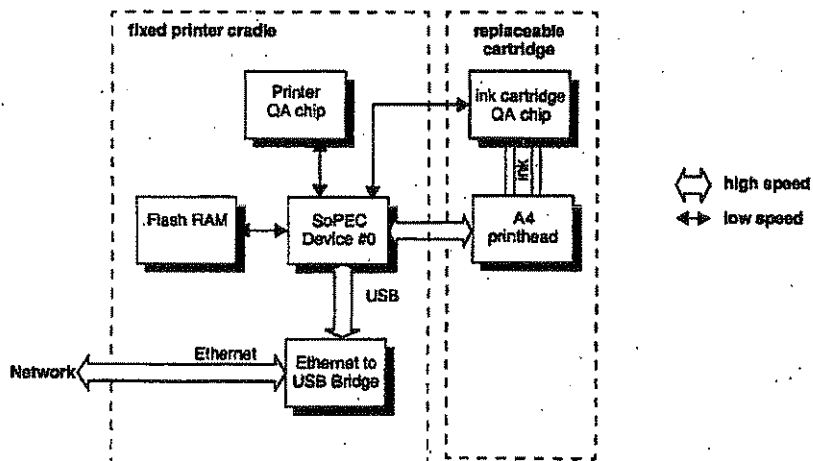


FIG. 8

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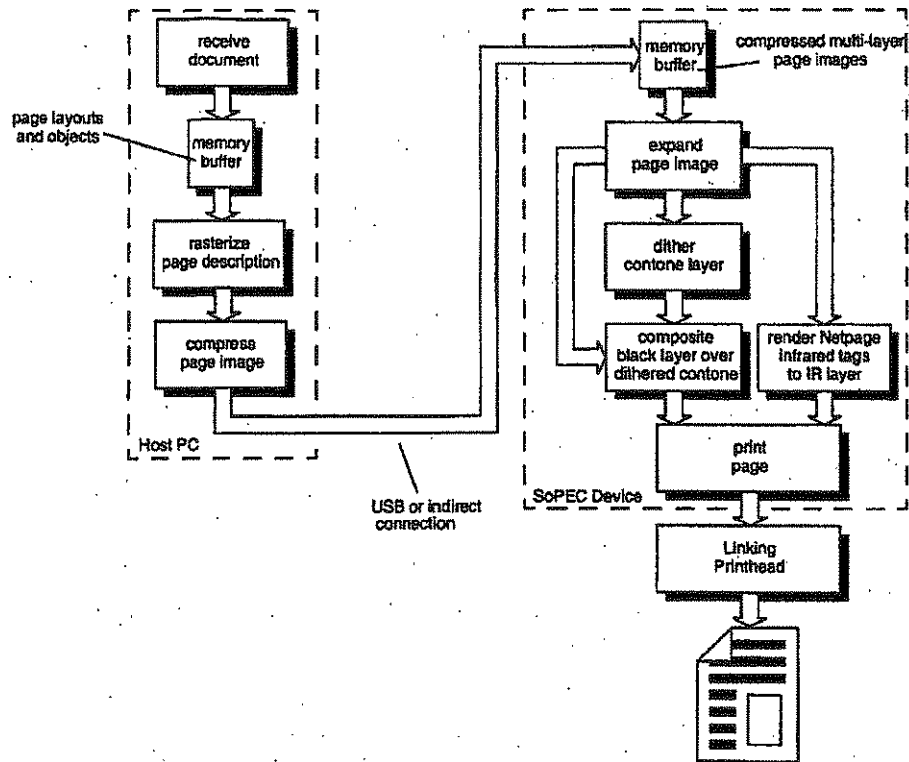


FIG. 9

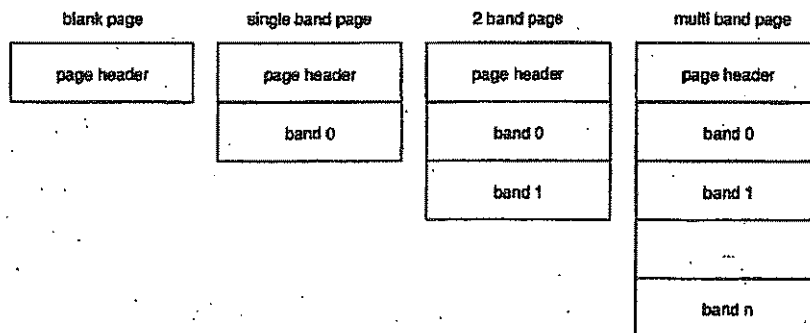


FIG. 10

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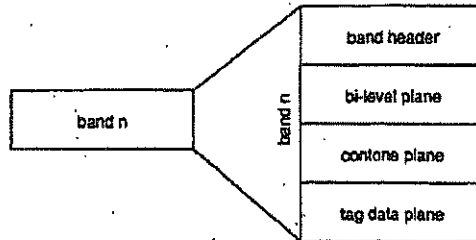


FIG. 11

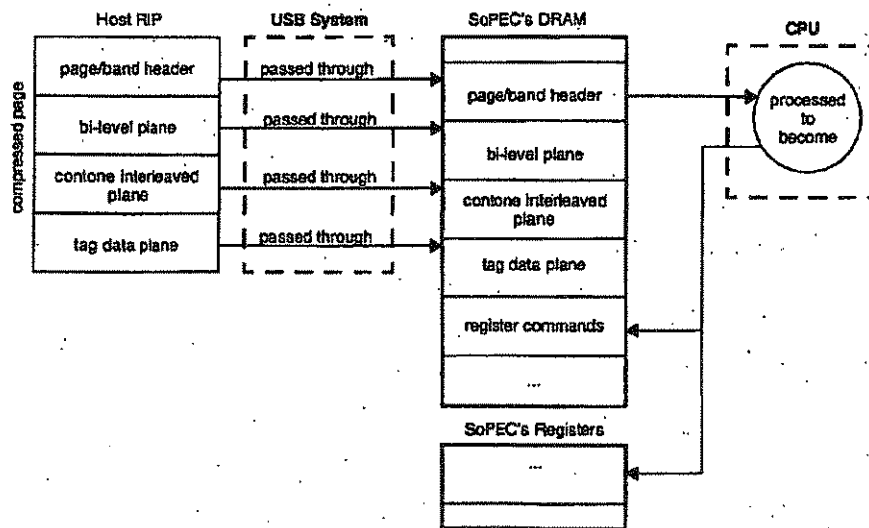


FIG. 12

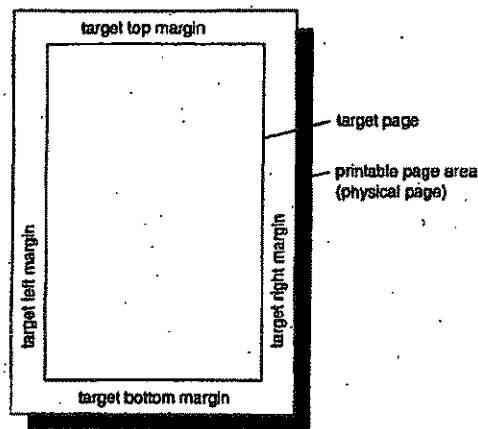


FIG. 13

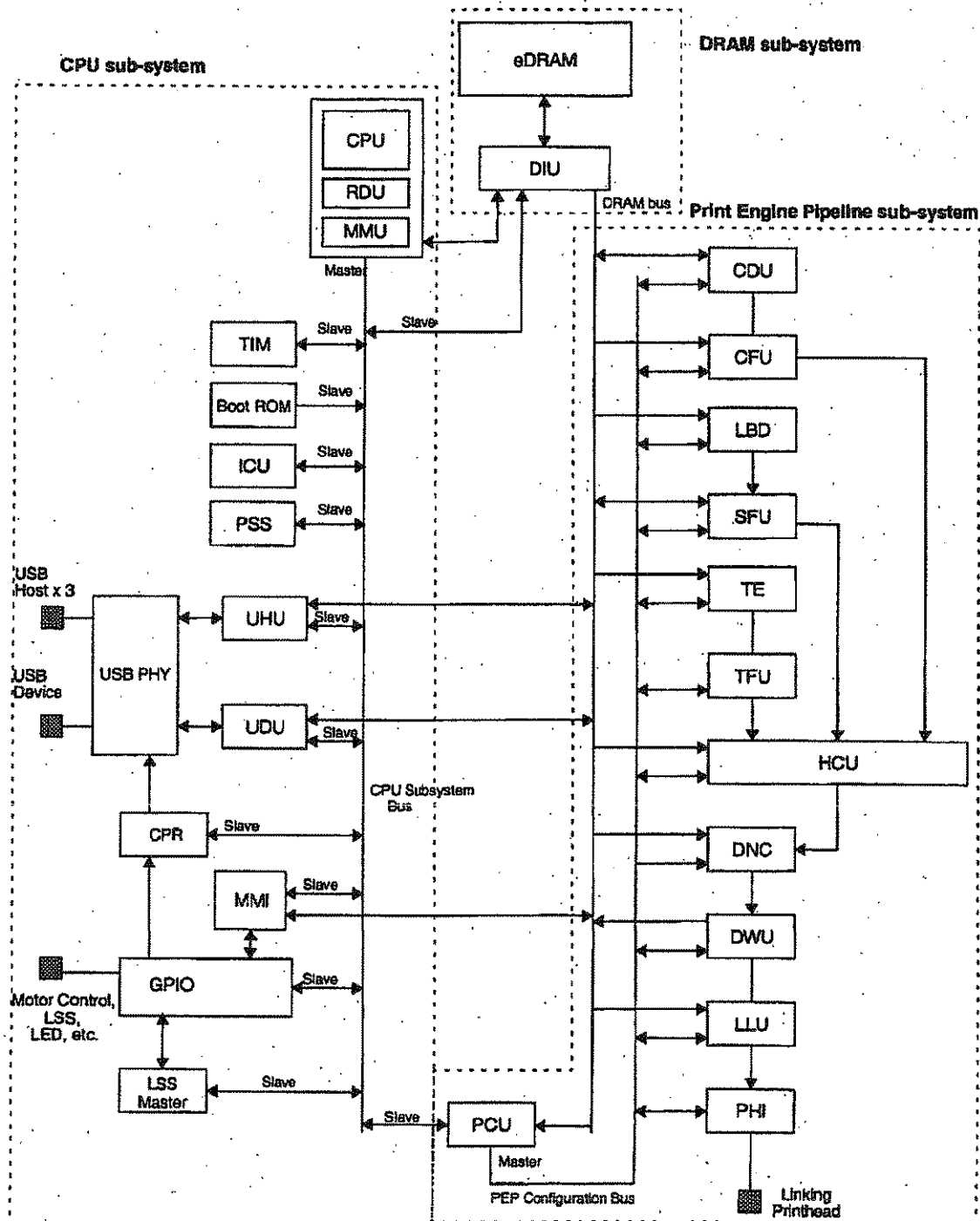


FIG. 14

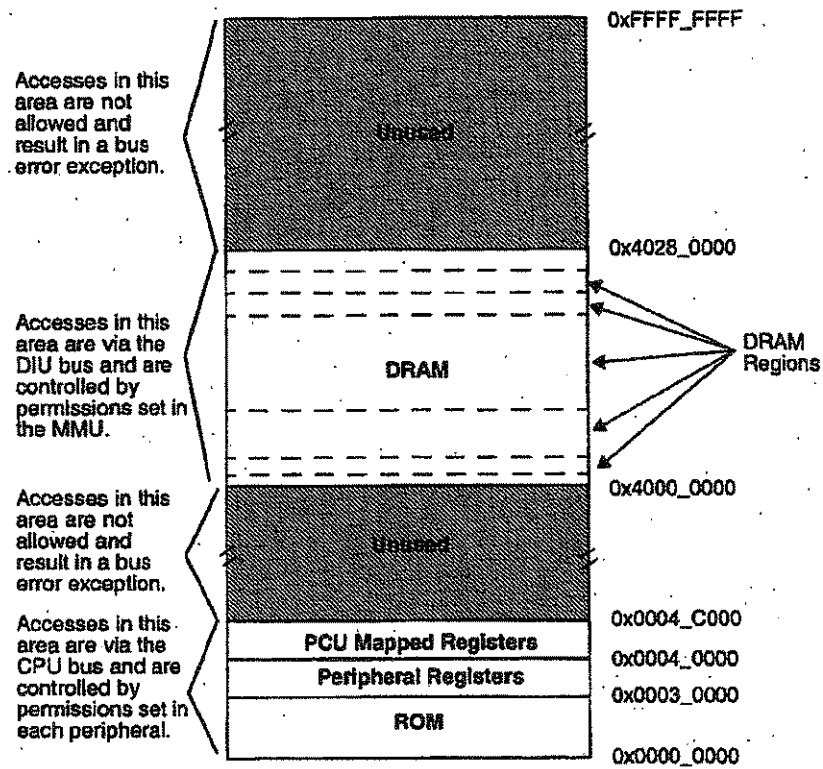
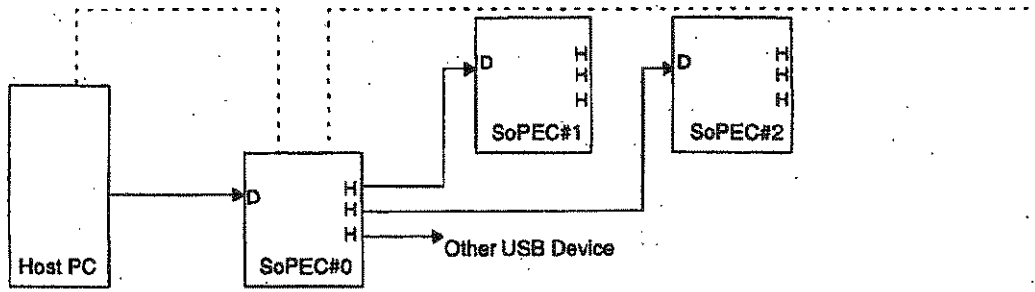
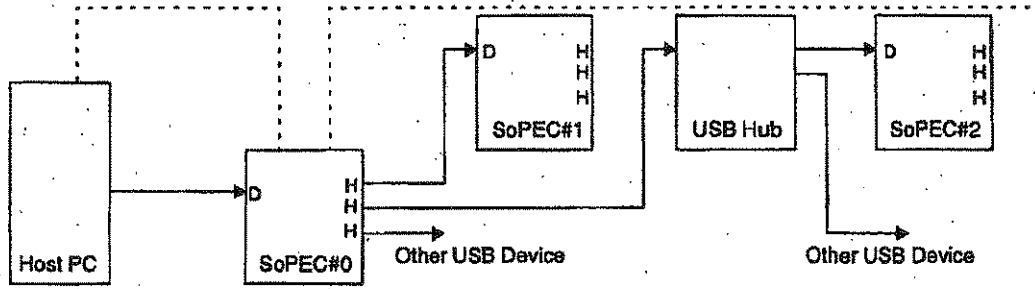


FIG. 15

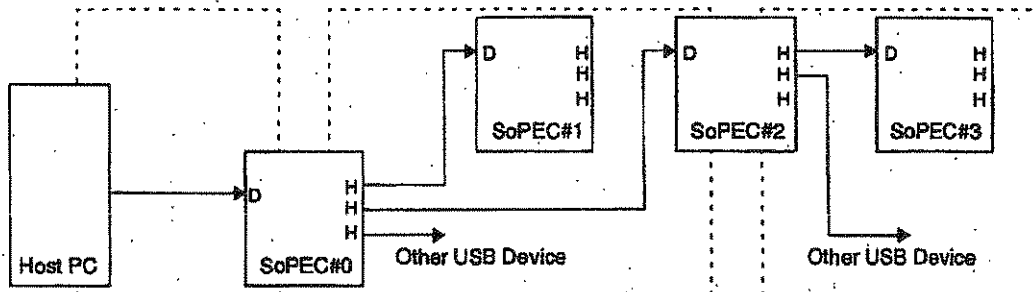
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Case 1: One Printer USB Bus with no Hub chips, up to 3 Devices on the bus



Case 2: One Printer USB Bus including Hub chip, more than 3 Devices on the bus



Case 3: Two Printer USB Busses, up to 3 devices on each bus

FIG. 16

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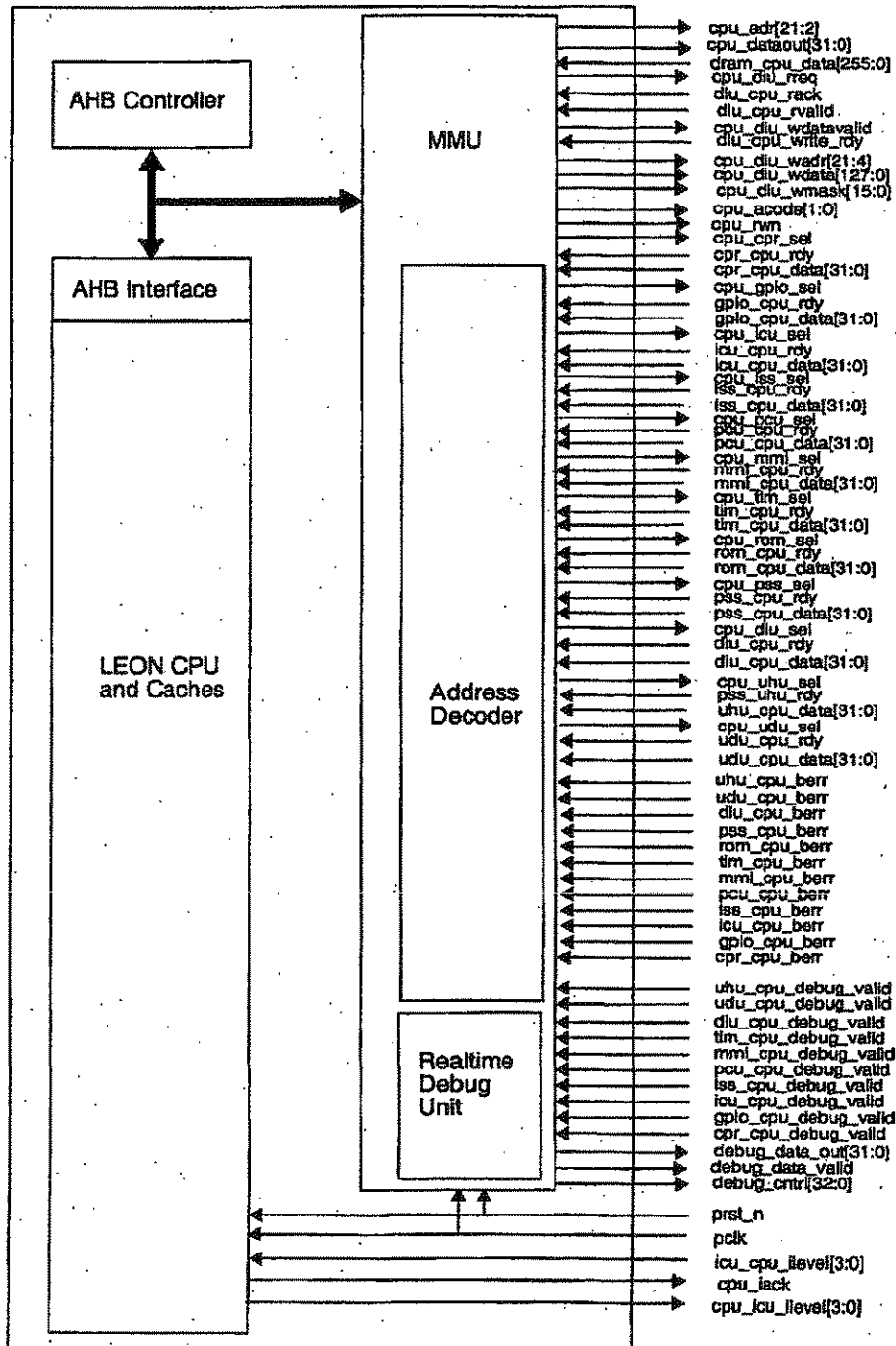


FIG. 17

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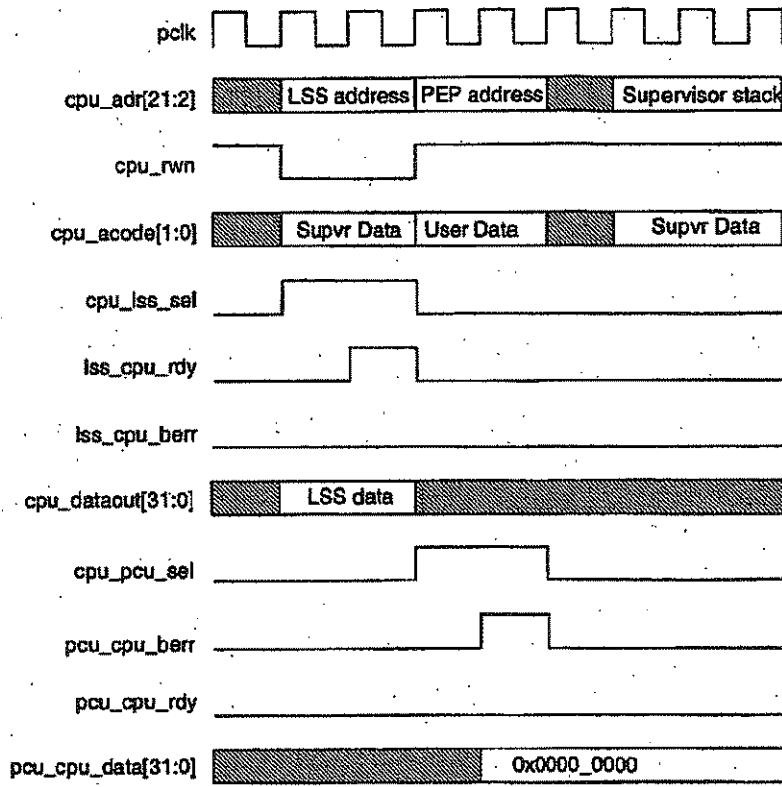


FIG. 18

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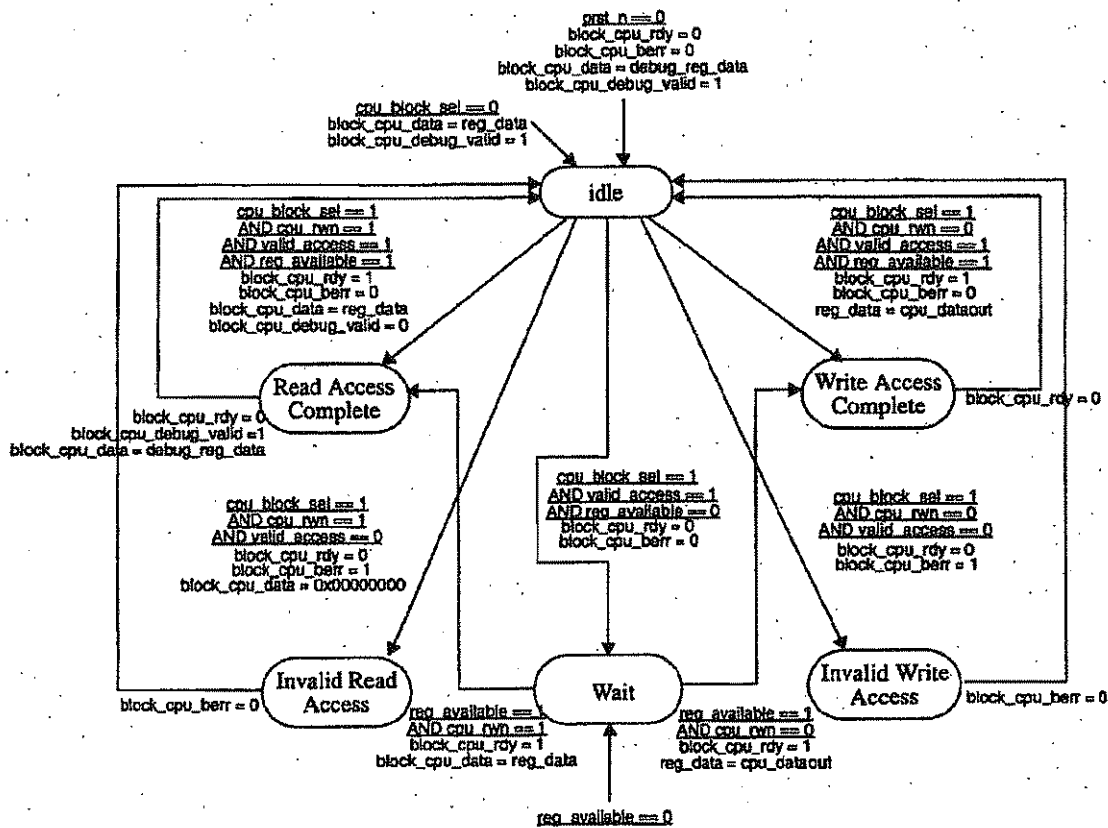


FIG. 19

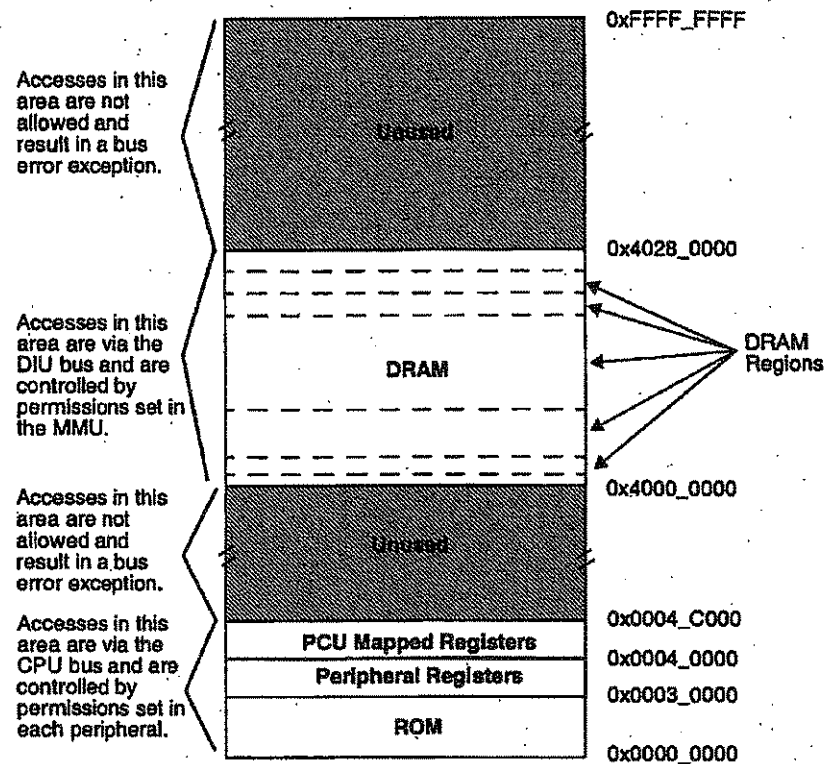


FIG. 20

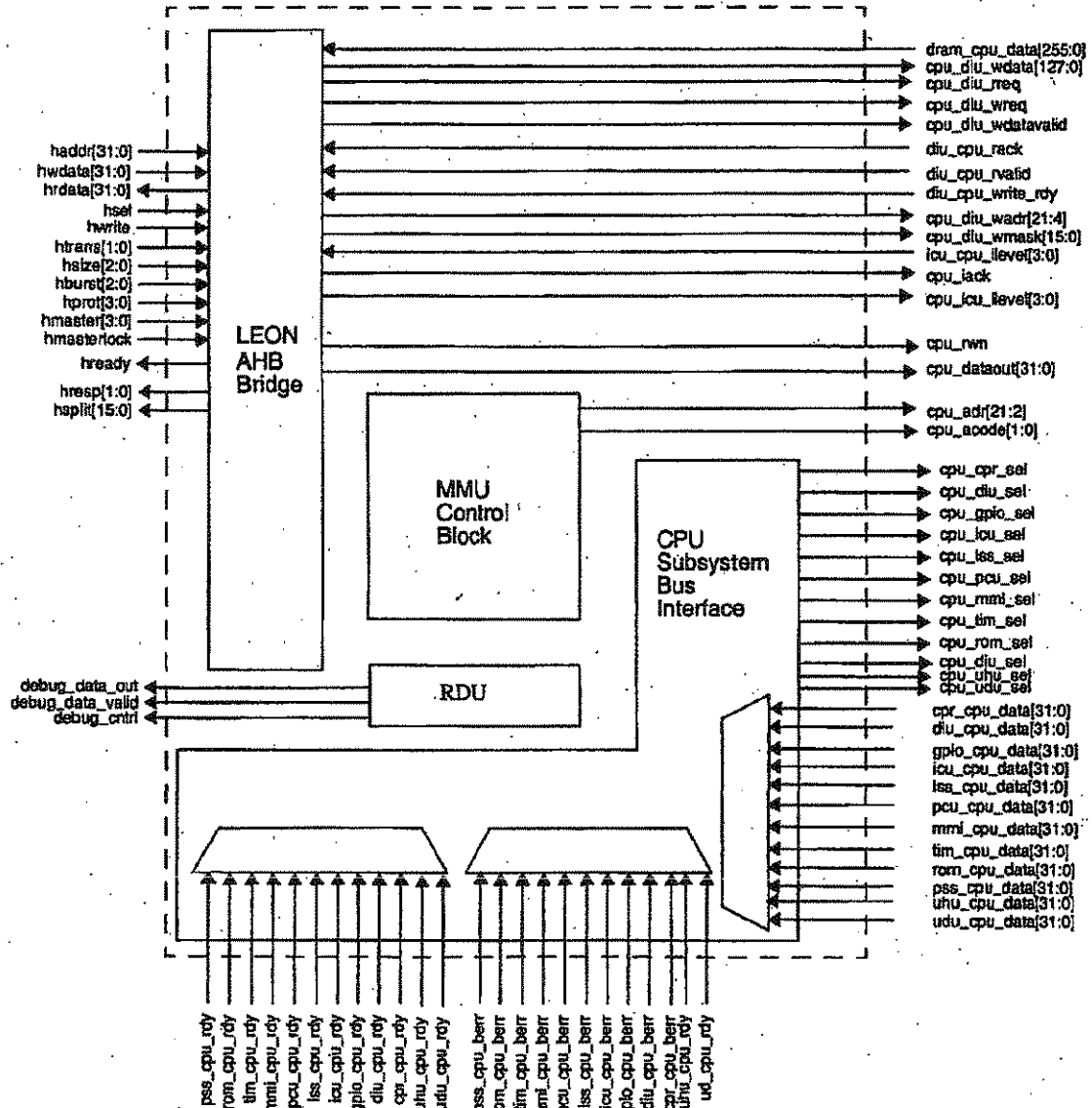


FIG. 21

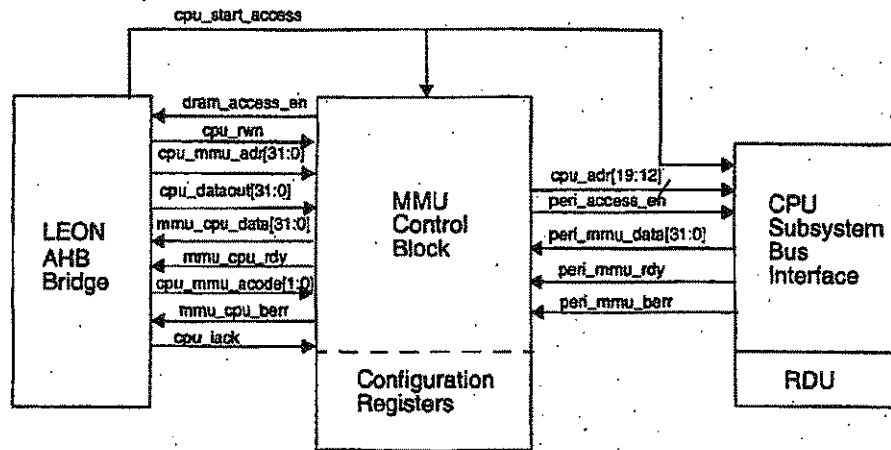


FIG. 22

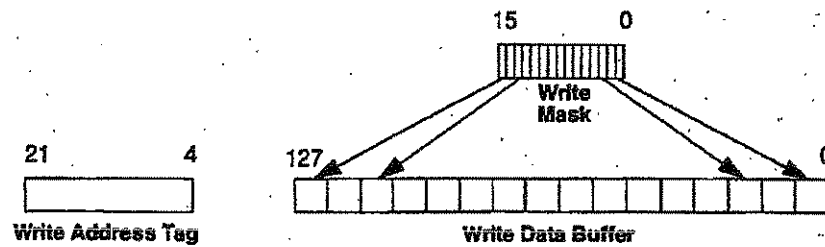


FIG. 23

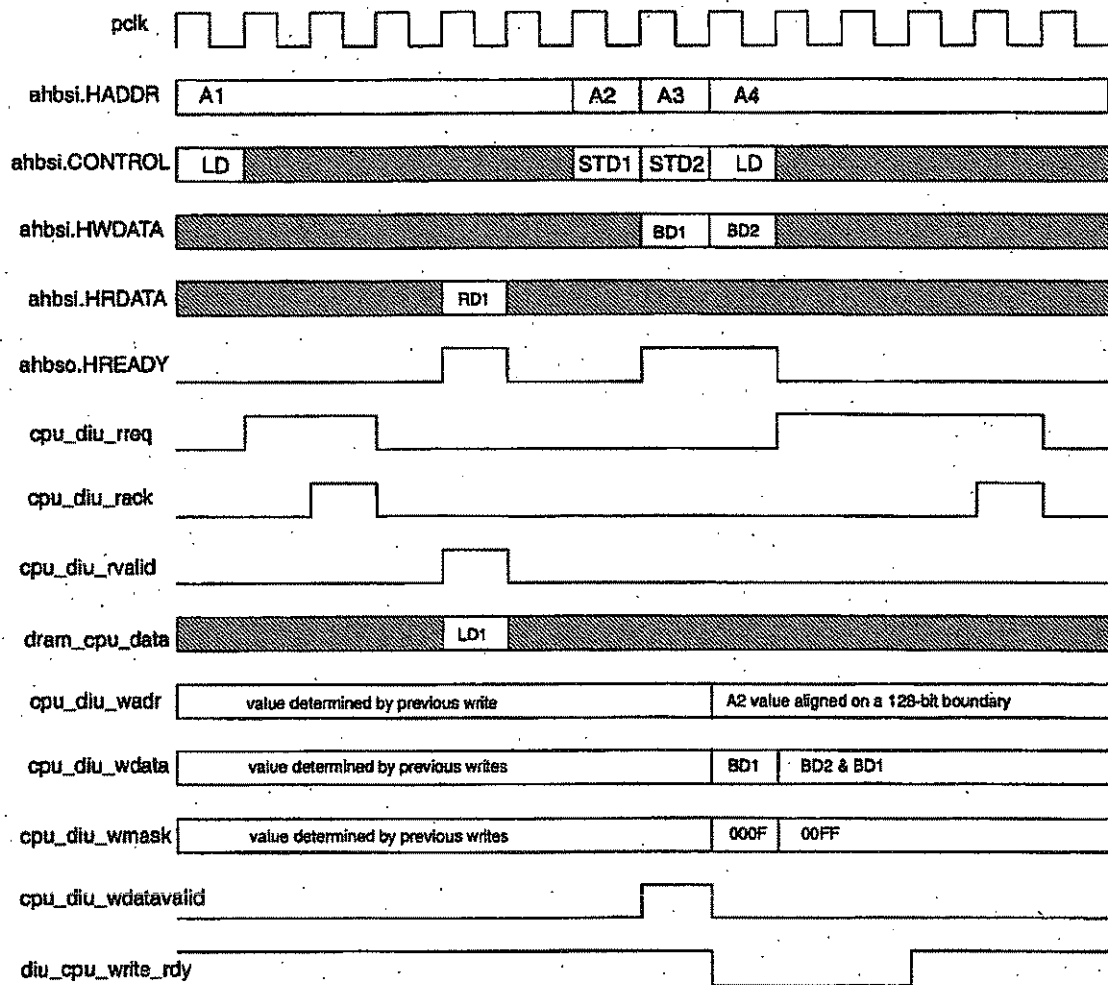


FIG. 24

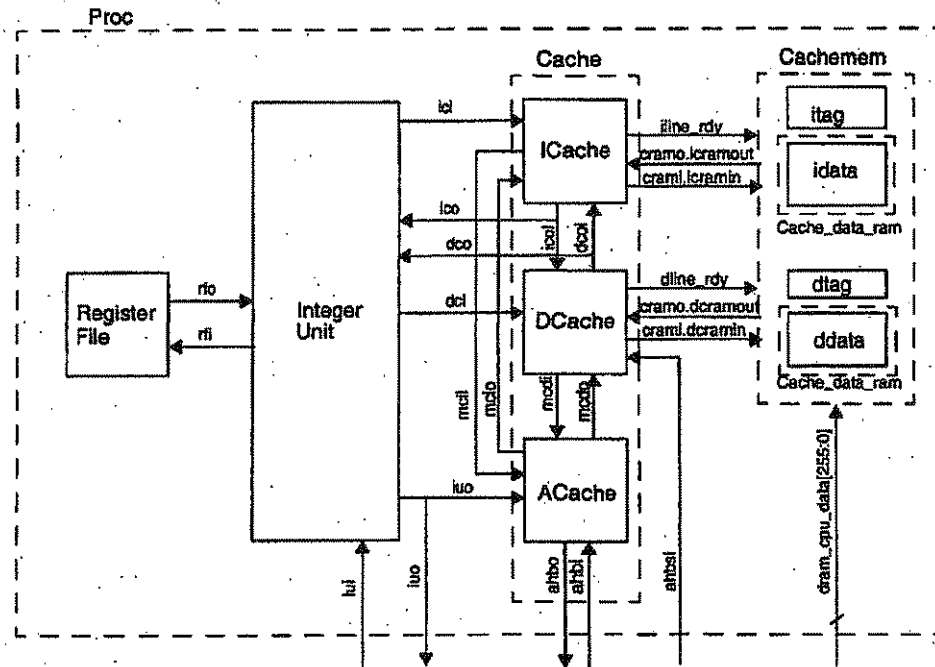


FIG. 25

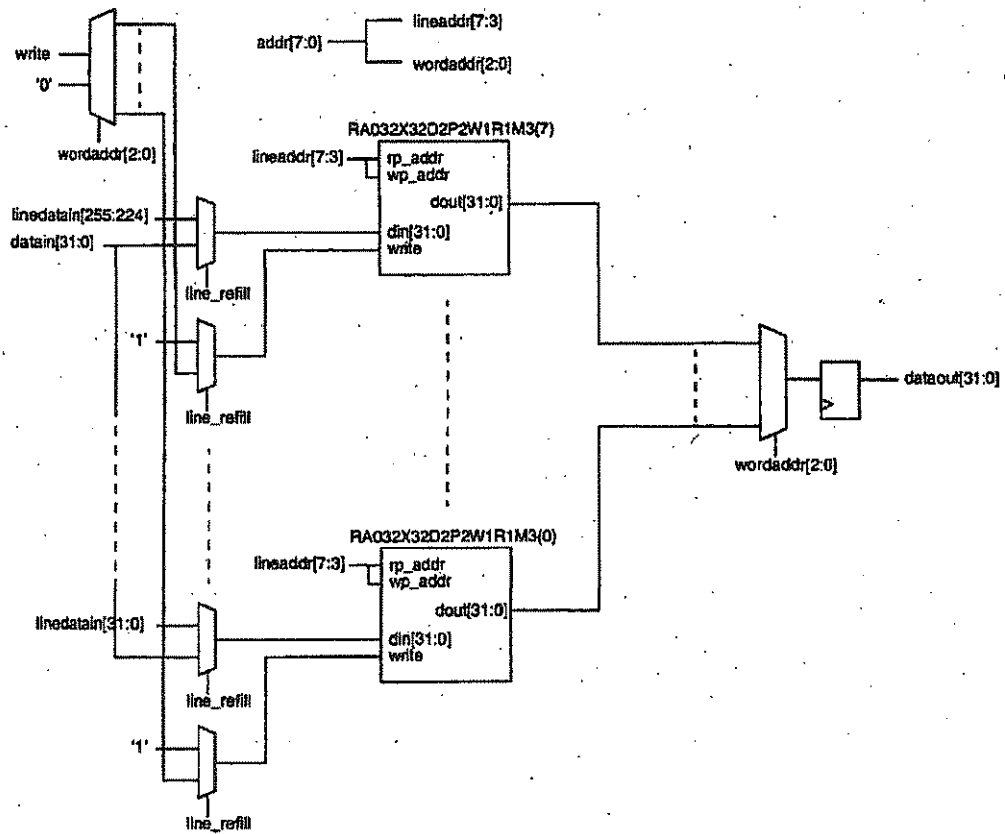


FIG. 26

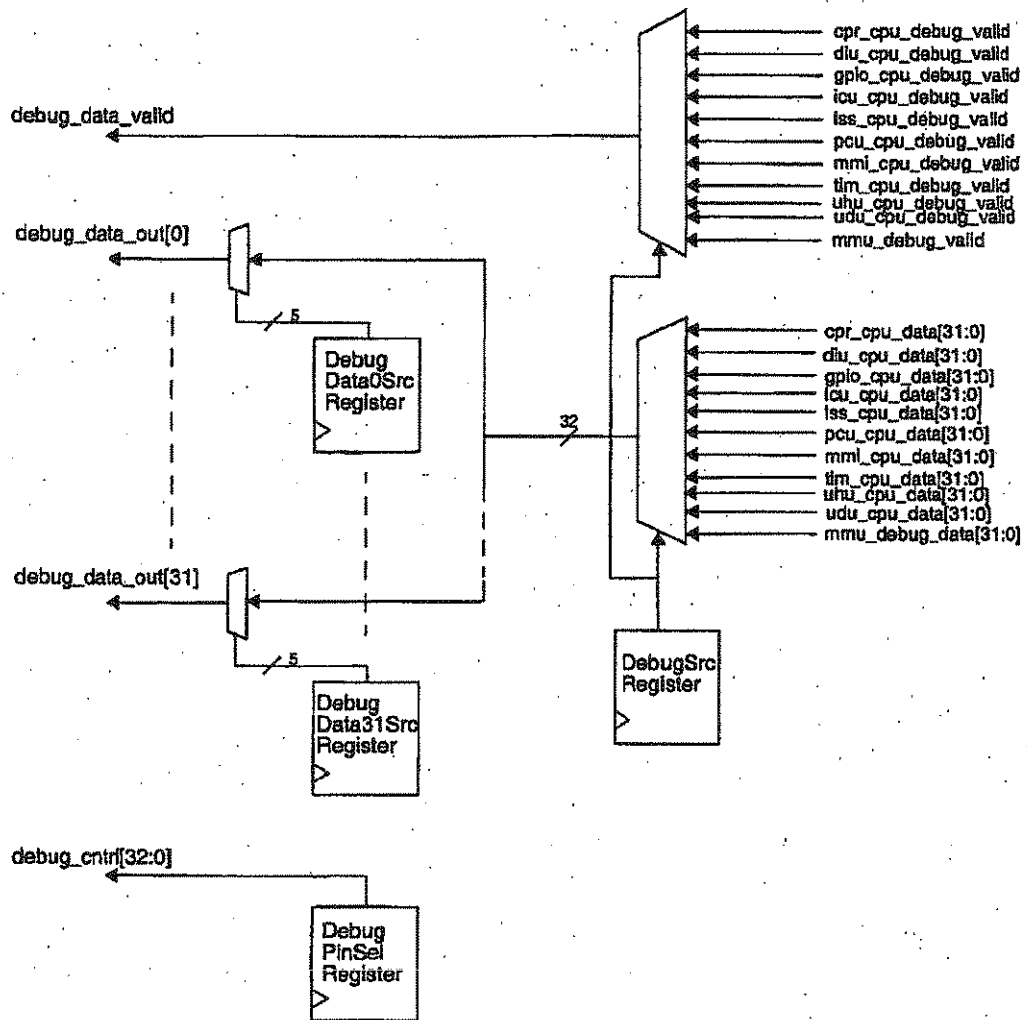


FIG. 27

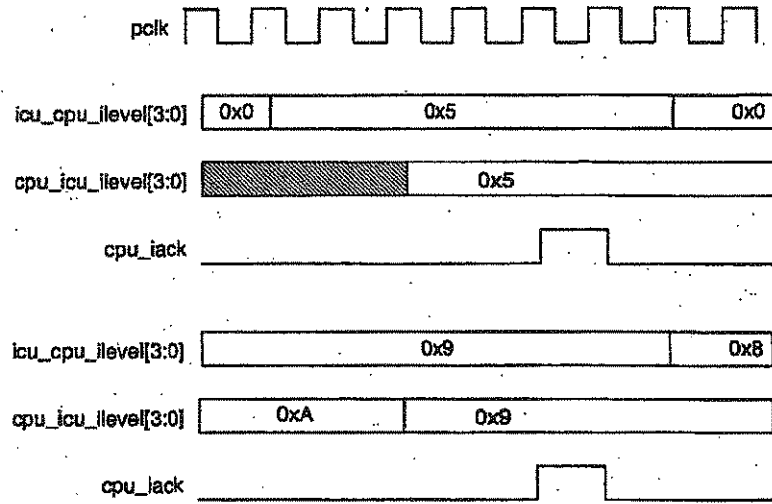


FIG. 28

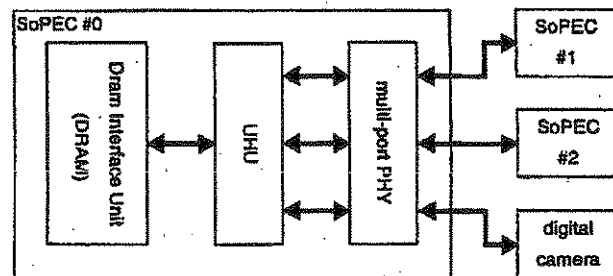


FIG. 29

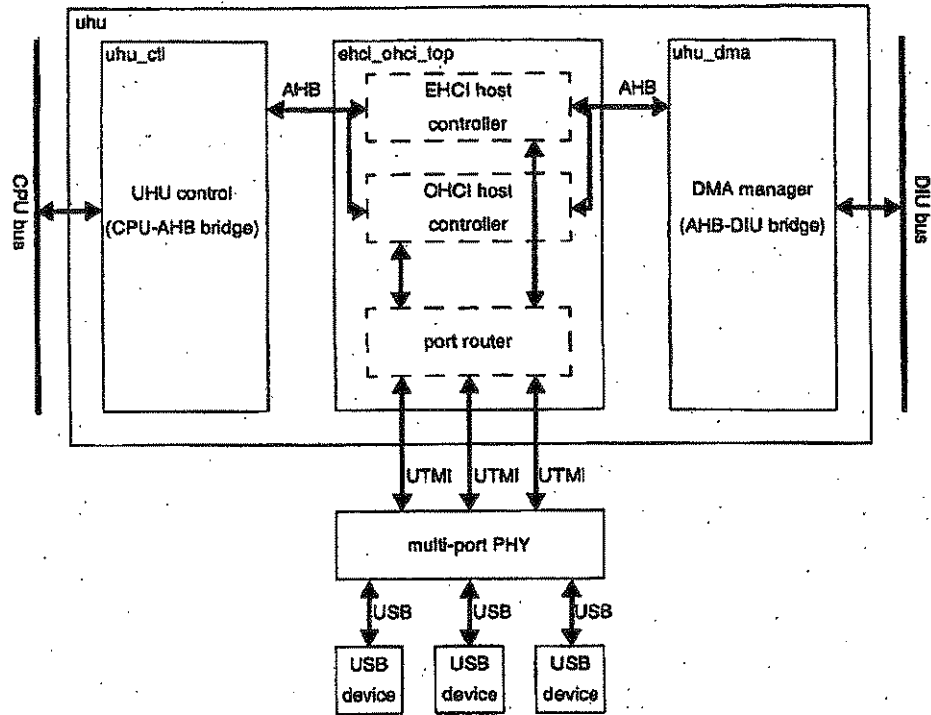


FIG. 30

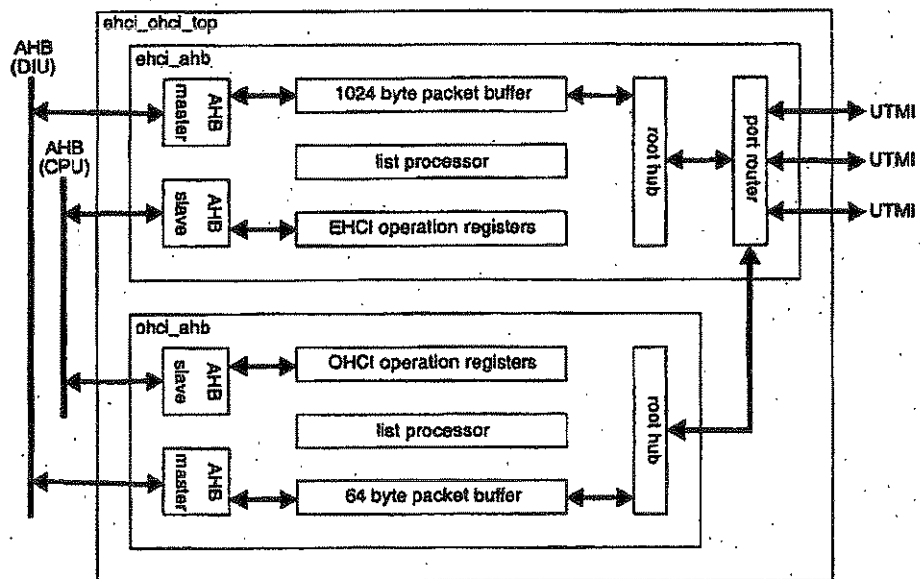


FIG. 31

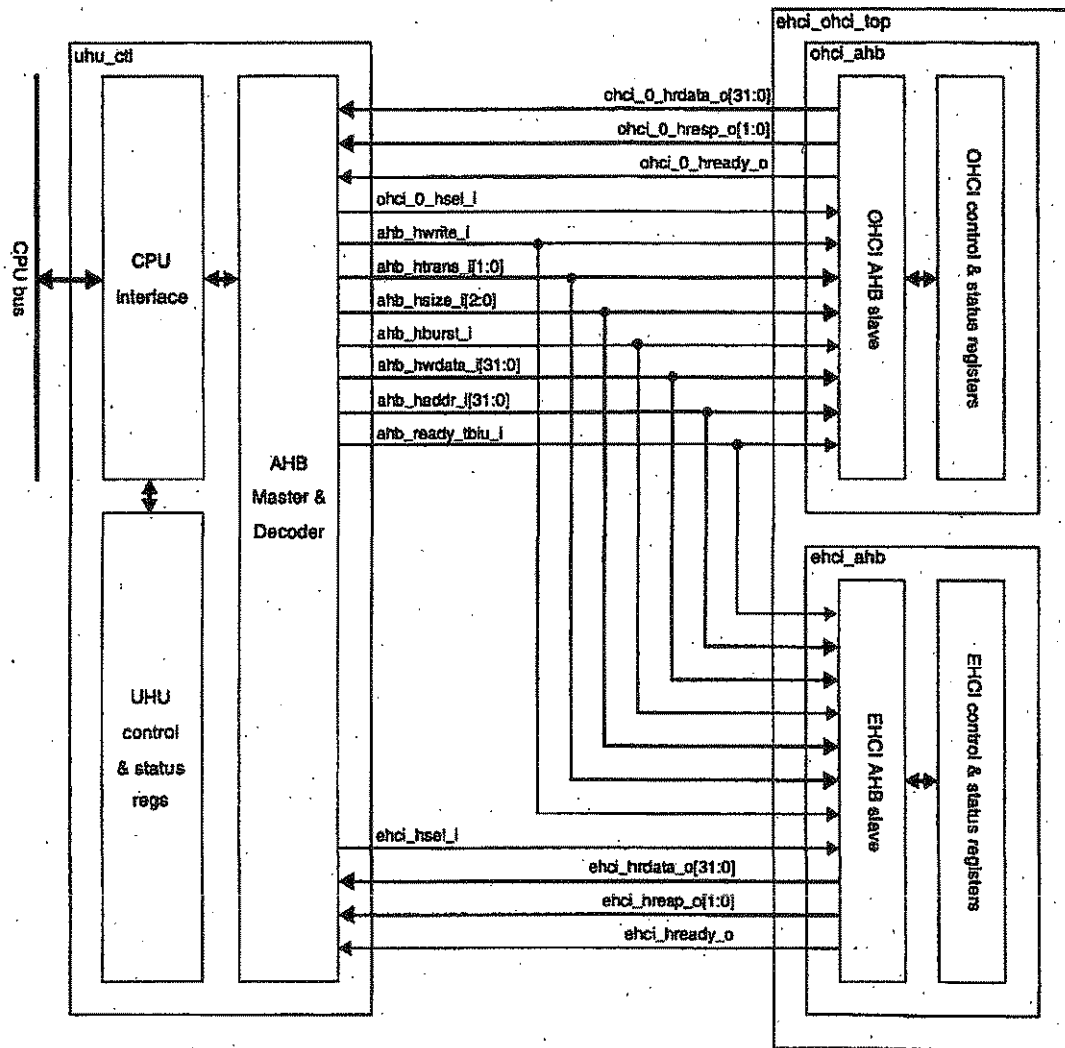


FIG. 32

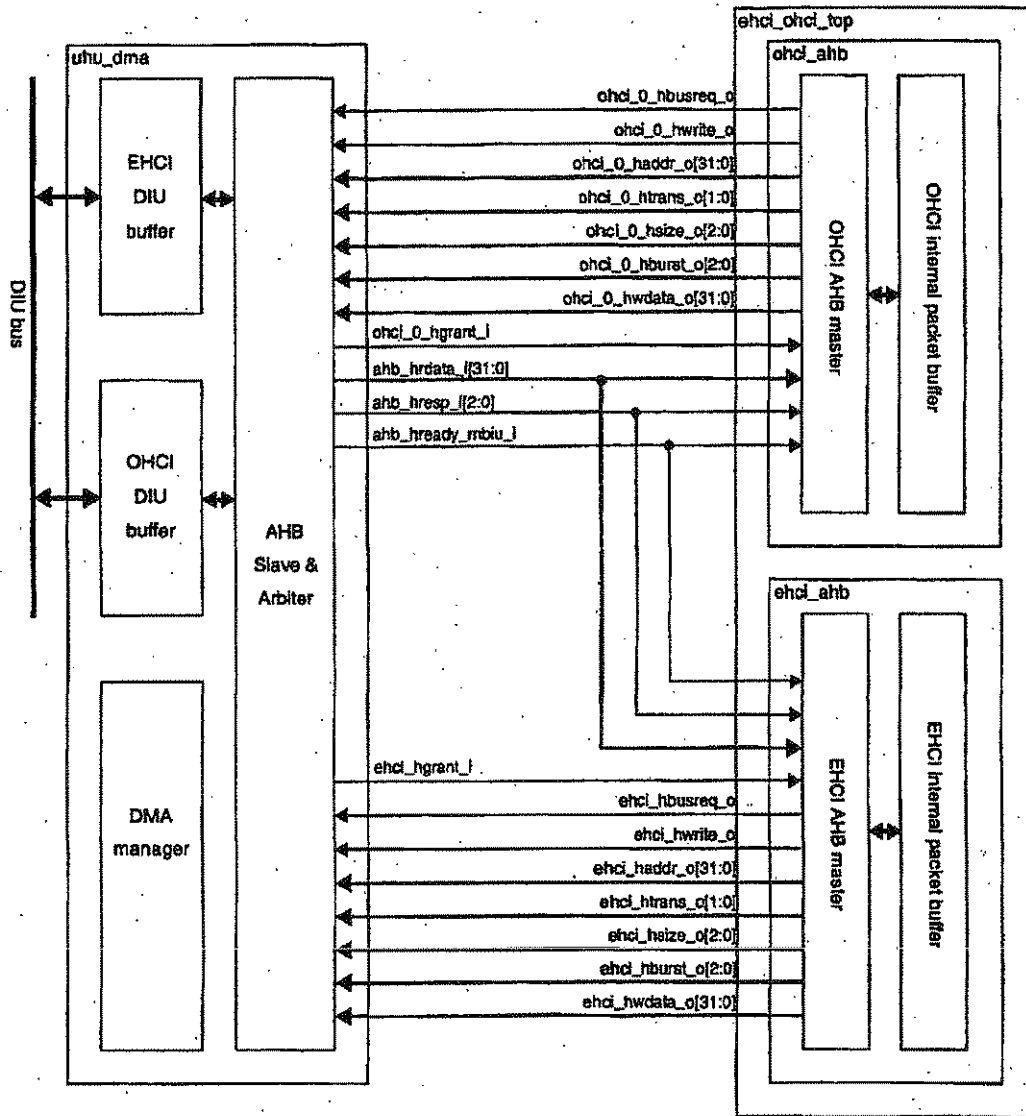


FIG. 33

(4 x 72 bits)
(4 x 72 bits)

The diagram illustrates the internal architecture of the UDC20 USB 2.0 device core. It is divided into several functional blocks and interfaces:

- UDC20 usb 2.0 device core (verilog 3rd party IP)**: The main processing block, containing:
 - Protocol Mgmt**: Manages the USB protocol, connected to the UTMI interface and the VCI master.
 - VCI master**: The central interface controller, connected to the Protocol Mgmt, the VCI read/write port, and the VCI slave.
 - Control/Status Registers**: Registers for device control and status, connected to the VCI slave and the bus adapter.
- Endpoint packet buffer**: A buffer for data packets, containing:
 - Control/Bulk data OUT**: Connected to the DIU write port.
 - Control/Bulk/Interrupt data IN**: Connected to the DIU read port.
 - DMA controller**: Manages direct memory access, connected to the bus adapter via a control signal.
- bus adapter**: Connects the internal core to the external **CPU interface**, containing:
 - Control/Status Registers**: Registers for the bus adapter, connected to the VCI read/write port and the internal Control/Status Registers.
- Interfaces**:
 - UTMI interface**: Connected to the Protocol Mgmt.
 - VCI read/write port**: Connects the VCI master to the Endpoint packet buffer and the bus adapter.
 - DIU write port**: Connects the Control/Bulk data OUT buffer to the Data Input/Output (DIU).
 - DIU read port**: Connects the Control/Bulk/Interrupt data IN buffer to the DIU.
 - CPU interface**: Connects the bus adapter to the system CPU.

FIG. 35

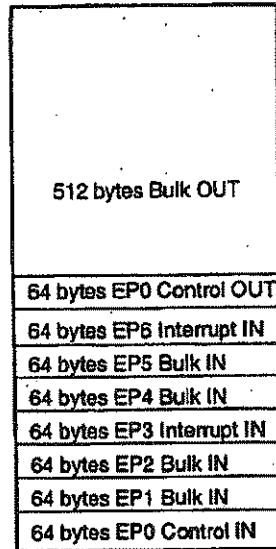
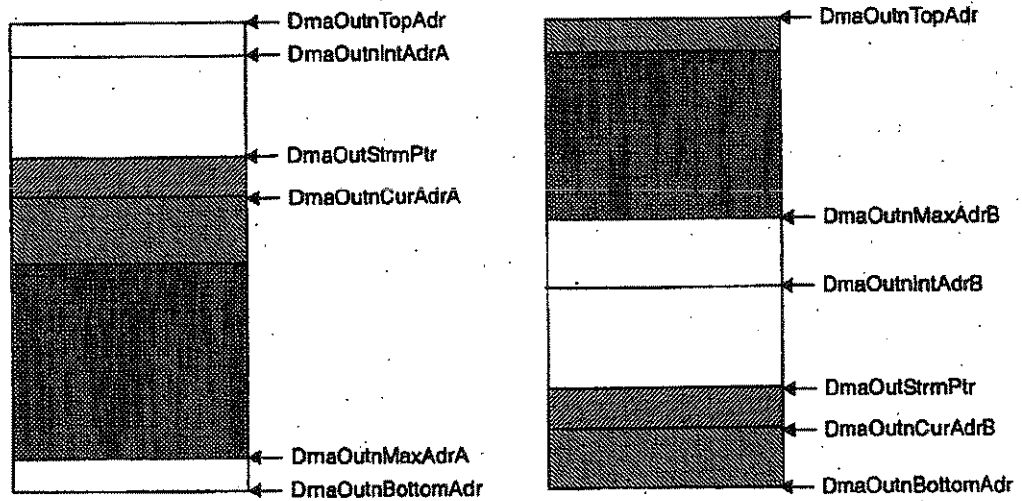


FIG. 36



(a) using Descriptor A

(b) changed to Descriptor B

- Key:
- Free buffer space
 - Filled buffer space (unprocessed data)
 - Buffer space filled since last write to the DMA descriptors
 - Buffer space filled with data before packet transfer is completed

FIG. 37

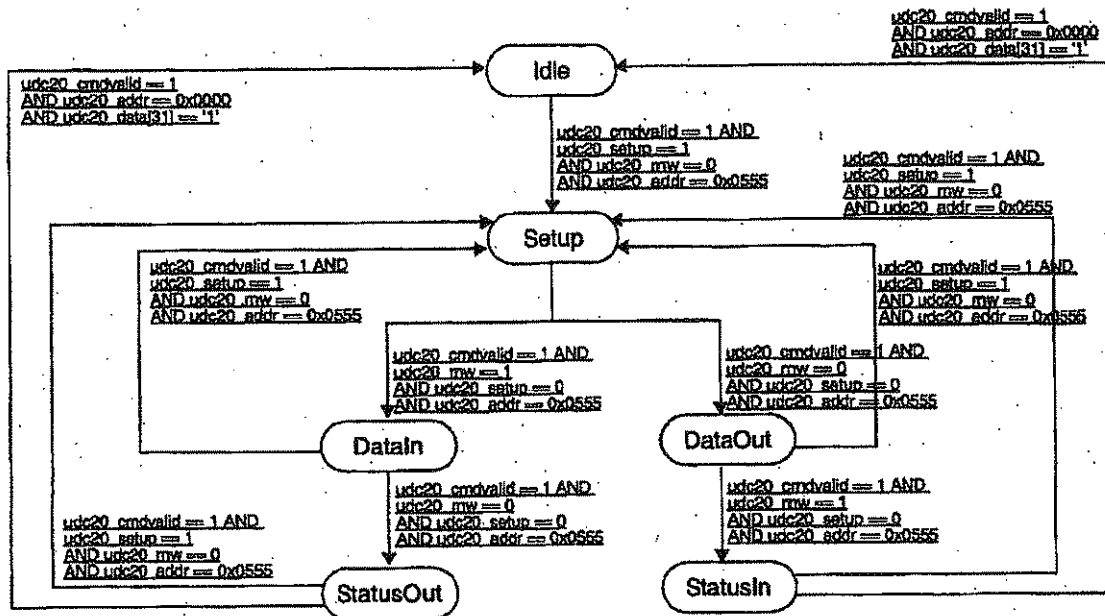


FIG. 38

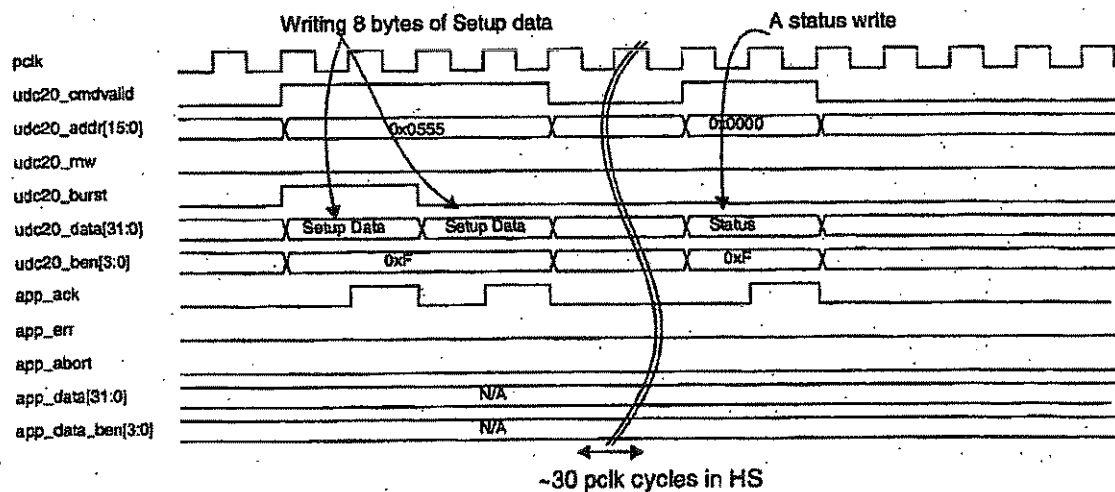


FIG. 39

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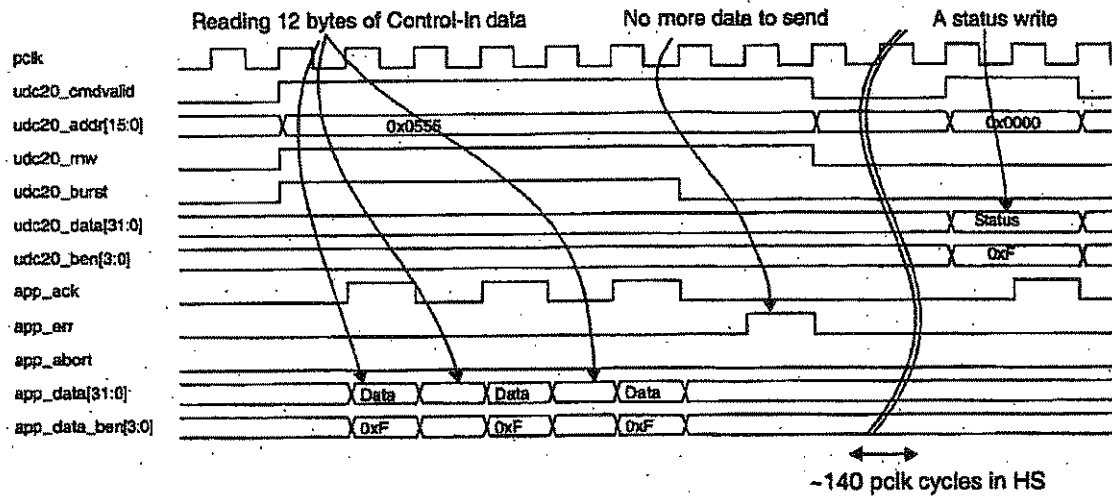


FIG. 40

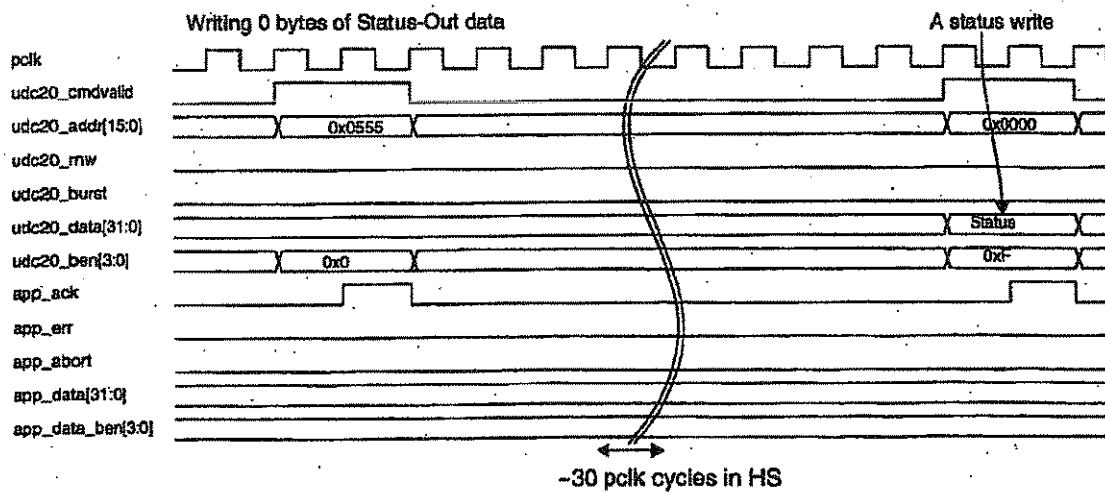


FIG. 41

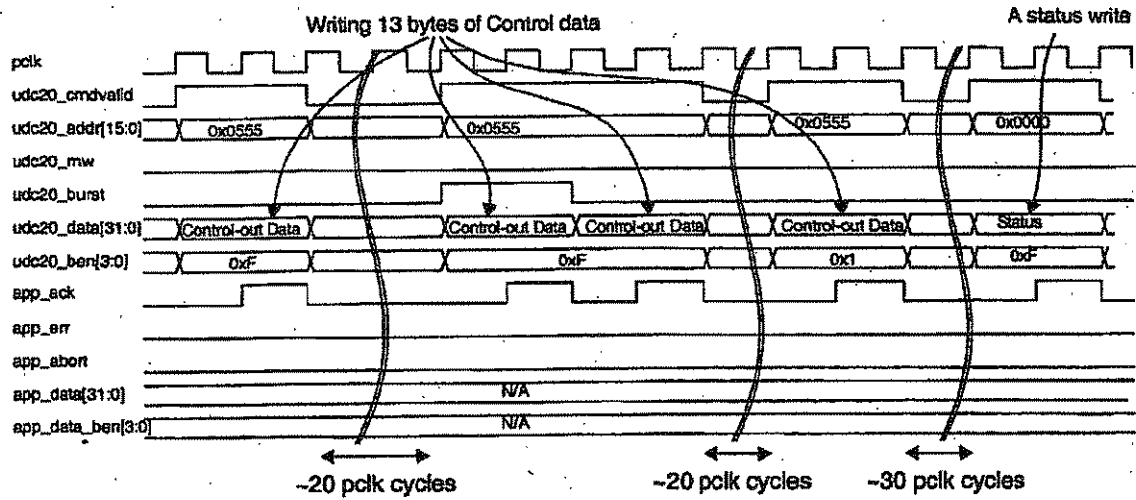


FIG. 42

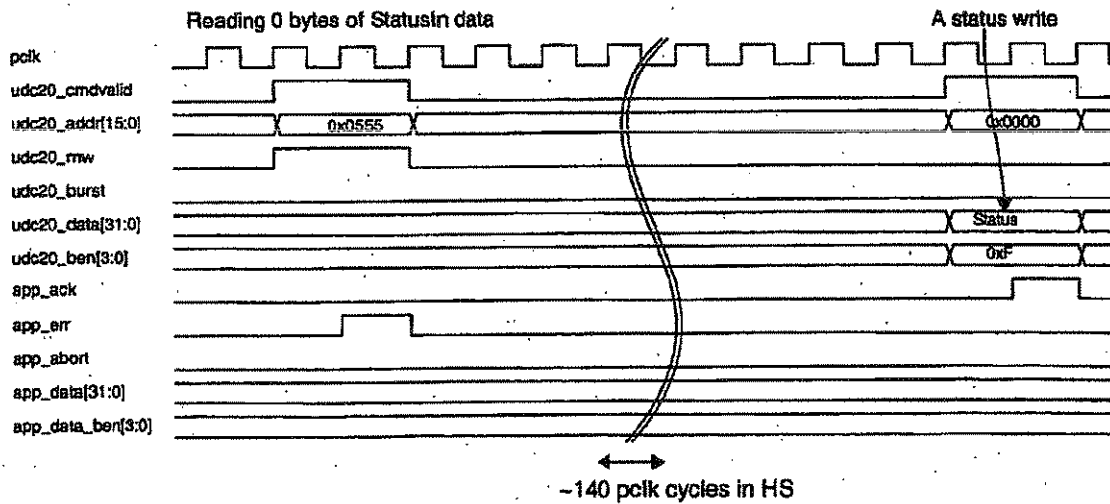


FIG. 43

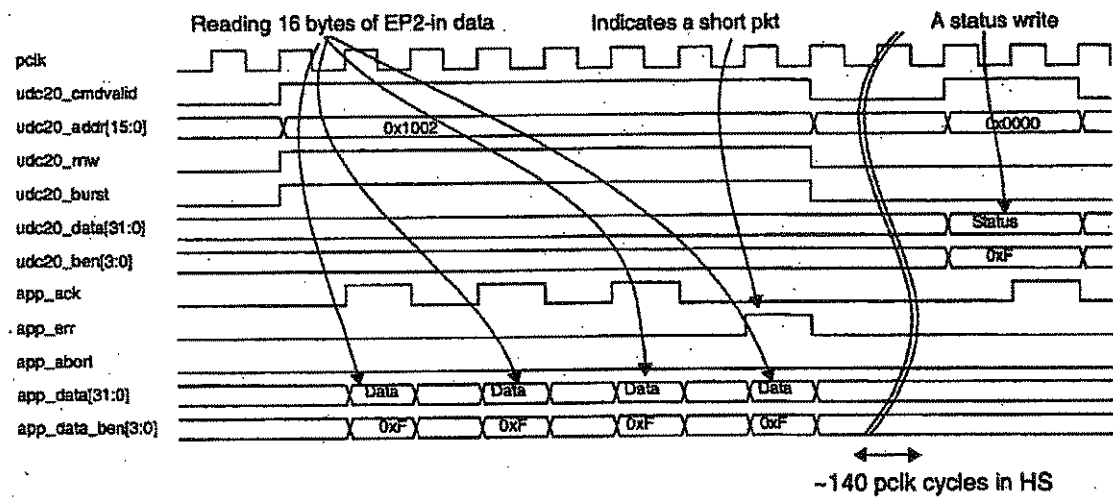


FIG. 44

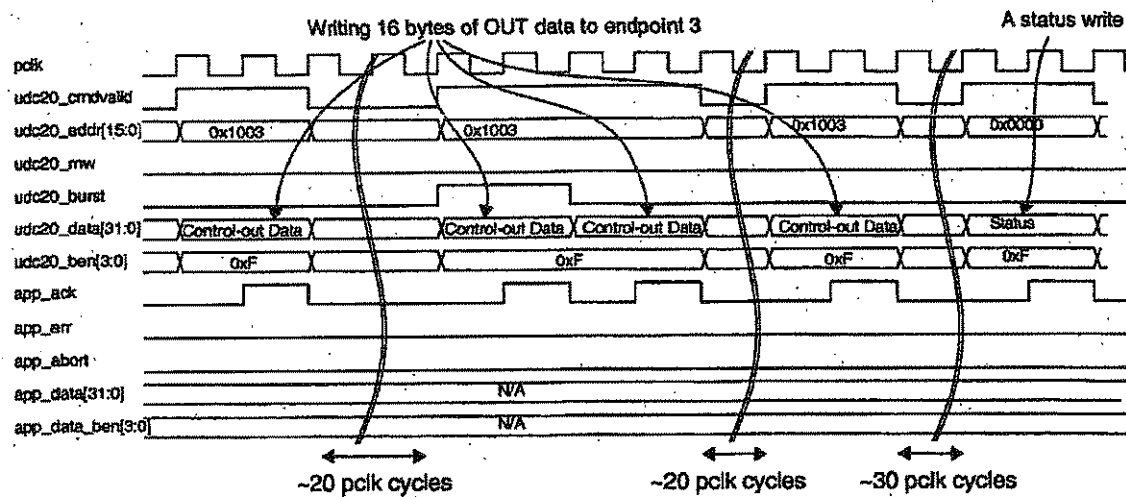


FIG. 45

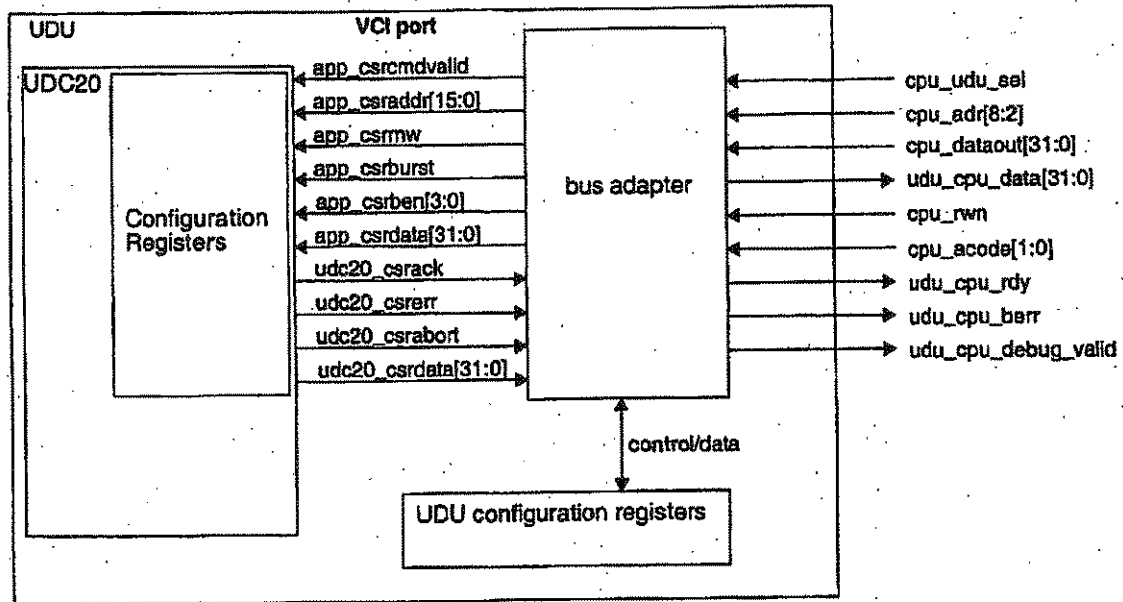


FIG. 46

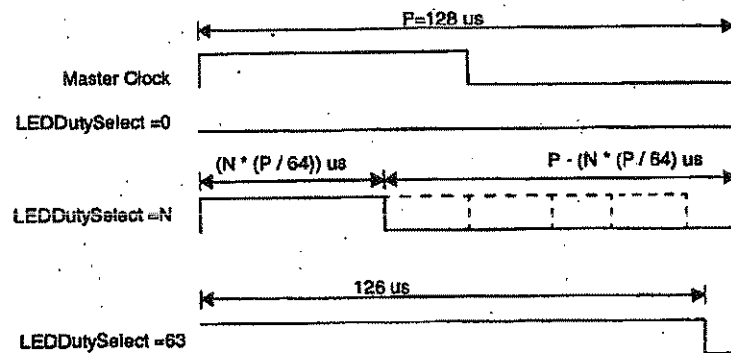


FIG. 47

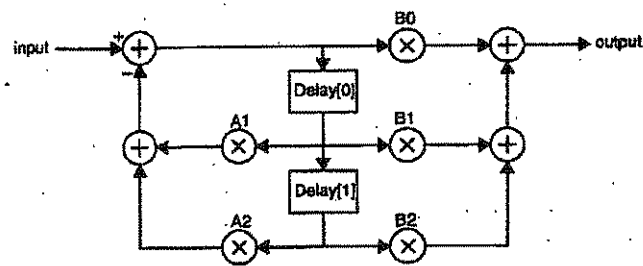


FIG. 48

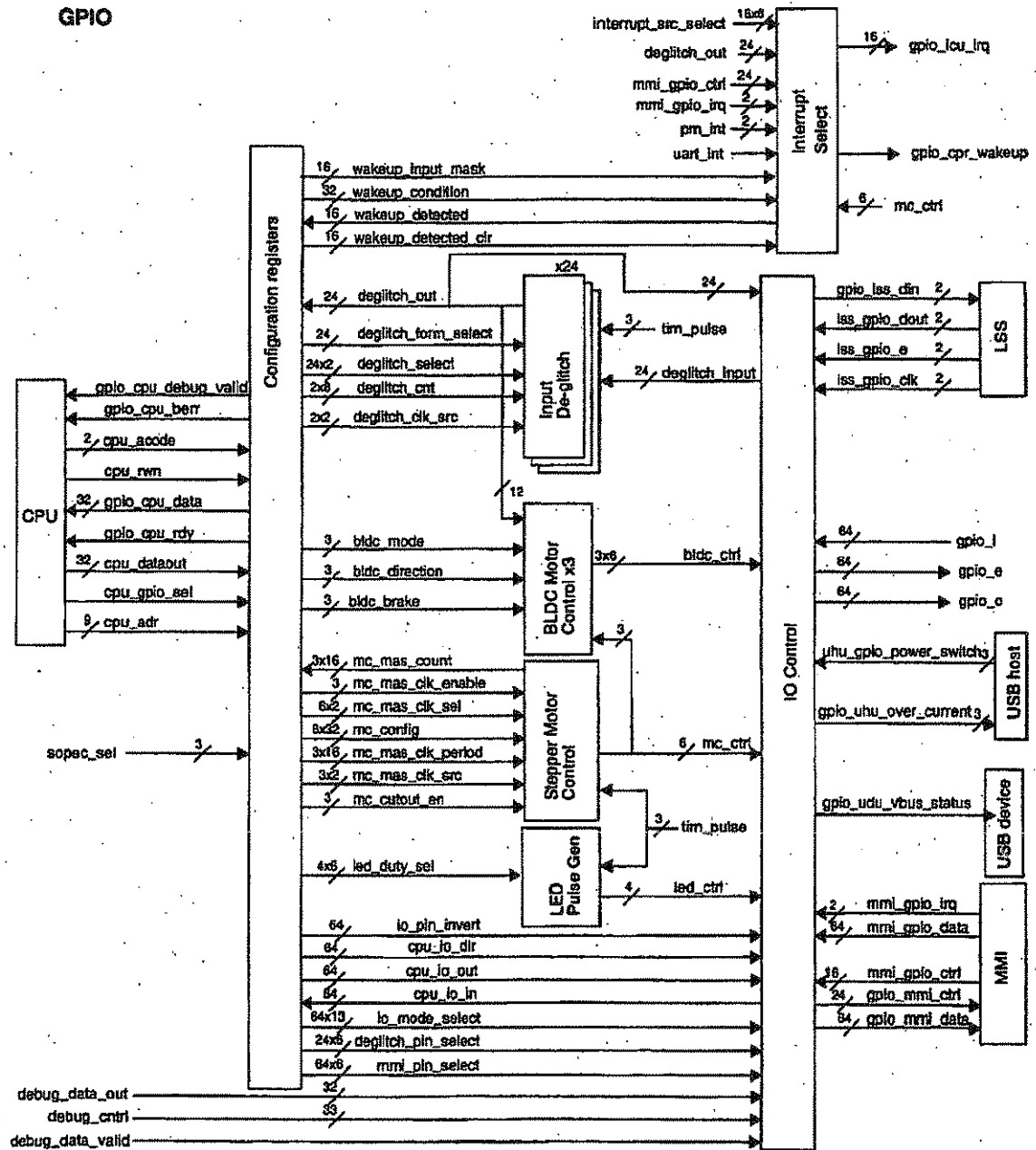


FIG. 49

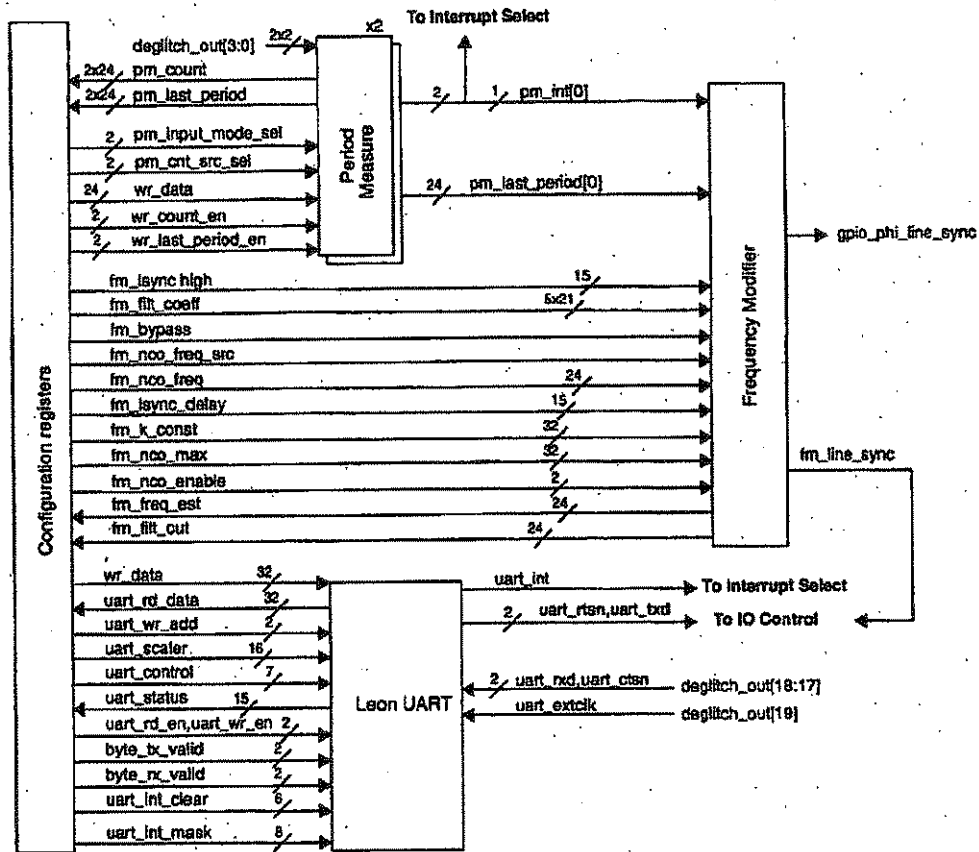


FIG. 50

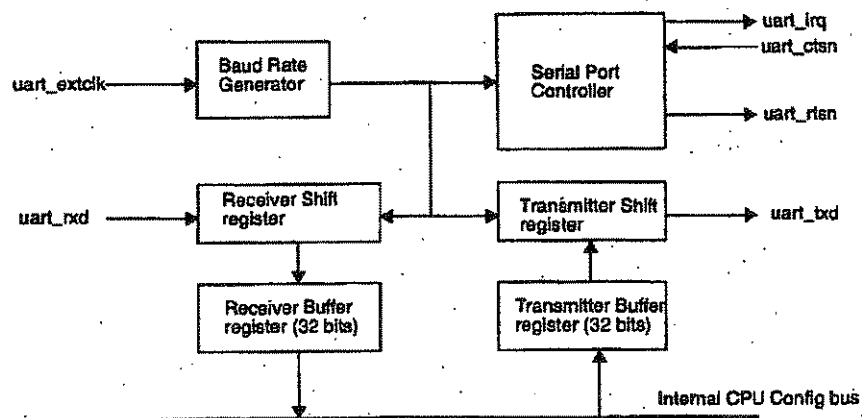


FIG. 51

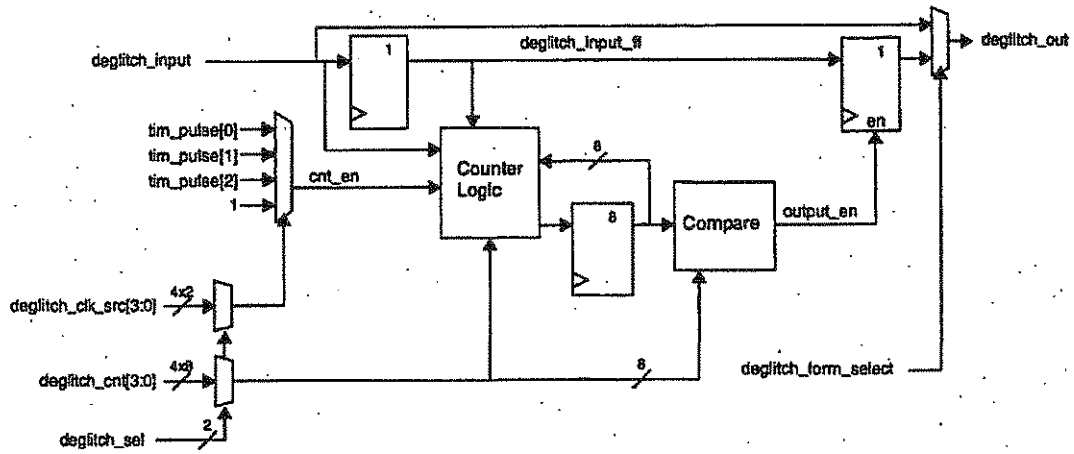


FIG. 52

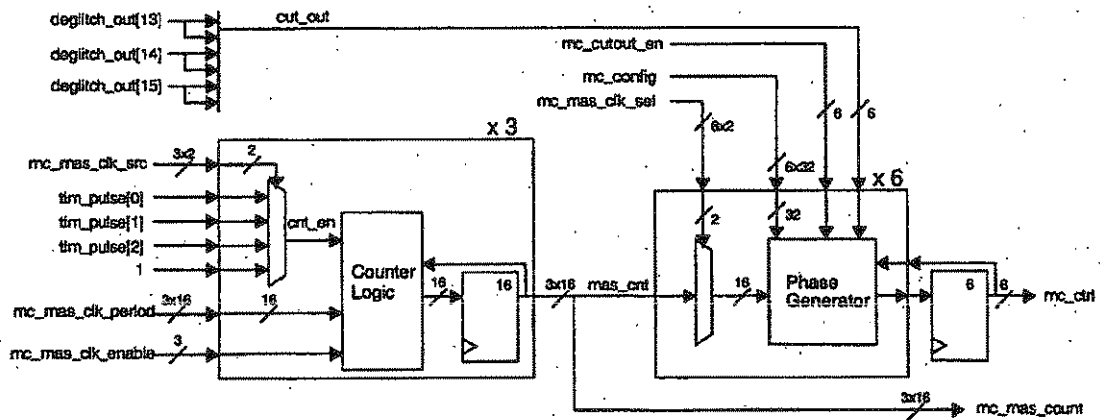


FIG. 53

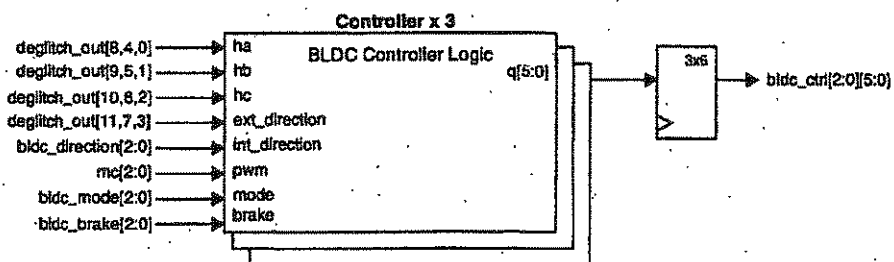


FIG. 54

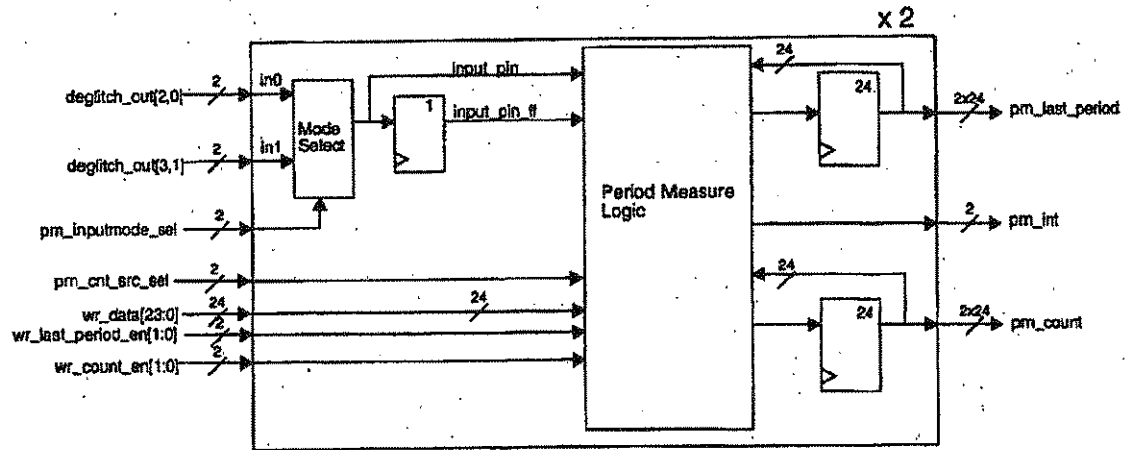


FIG. 55

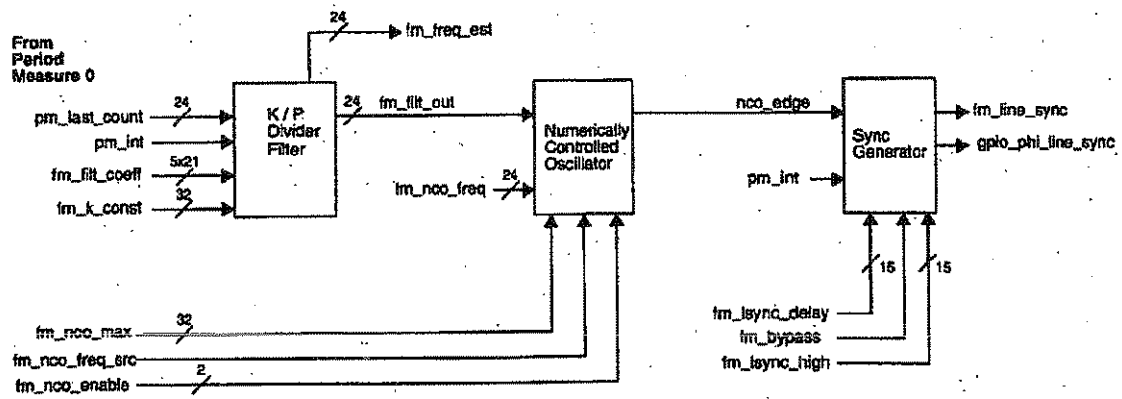


FIG. 56

Value	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Period Count																																
K division Constant																																
Frequency Estimate																																
Coefficient Constant																																
Filter internal states																																
Filter Output Frequency																																



Sign Bit



Fixed Point

FIG. 57

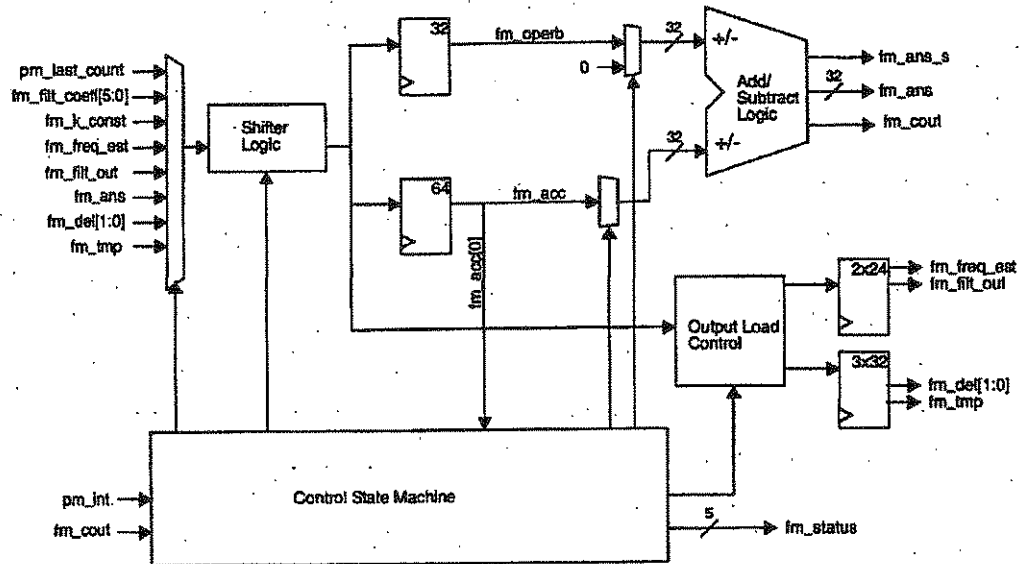


FIG. 58

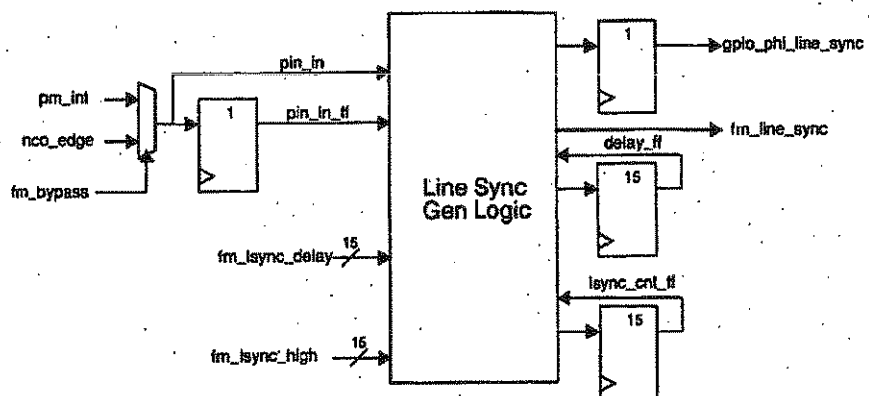


FIG. 59

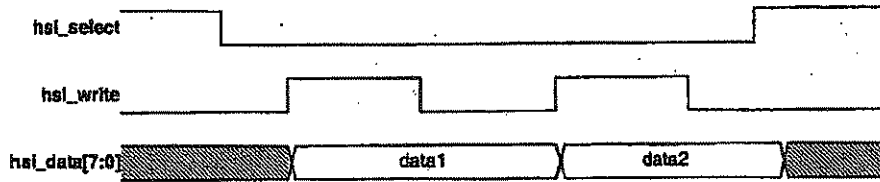


FIG. 60

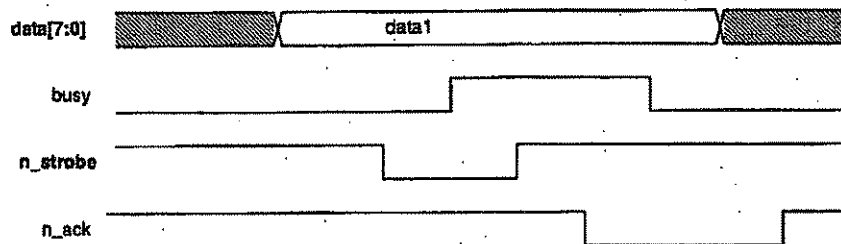


FIG. 61

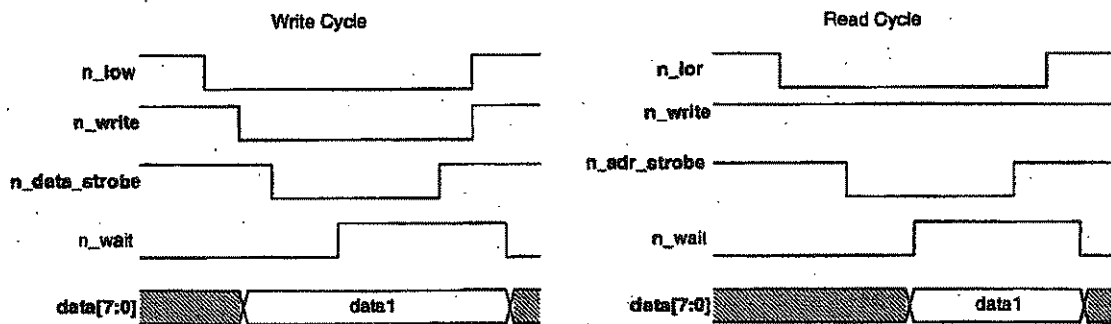


FIG. 62

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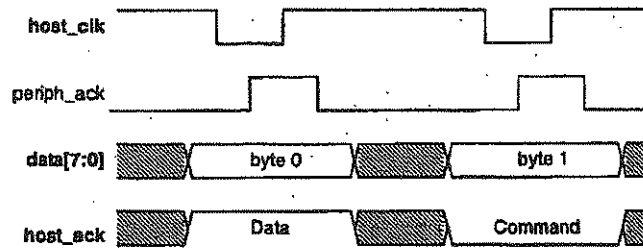


FIG. 63

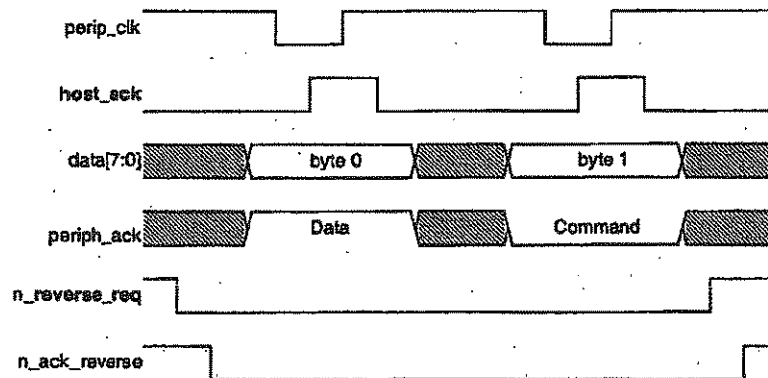


FIG. 64

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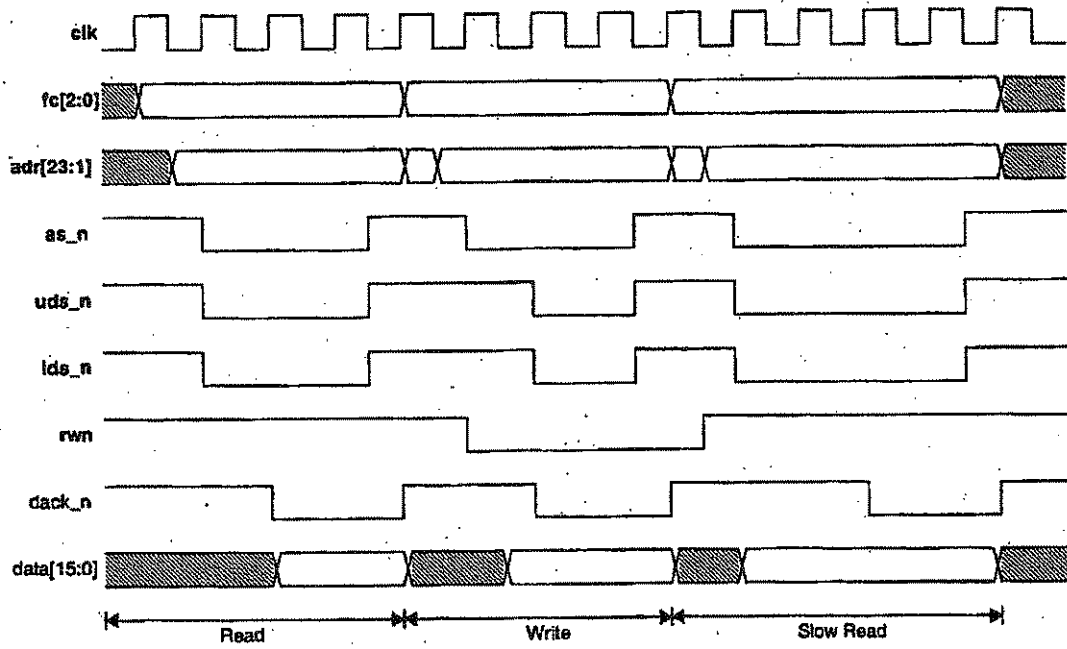


FIG. 65

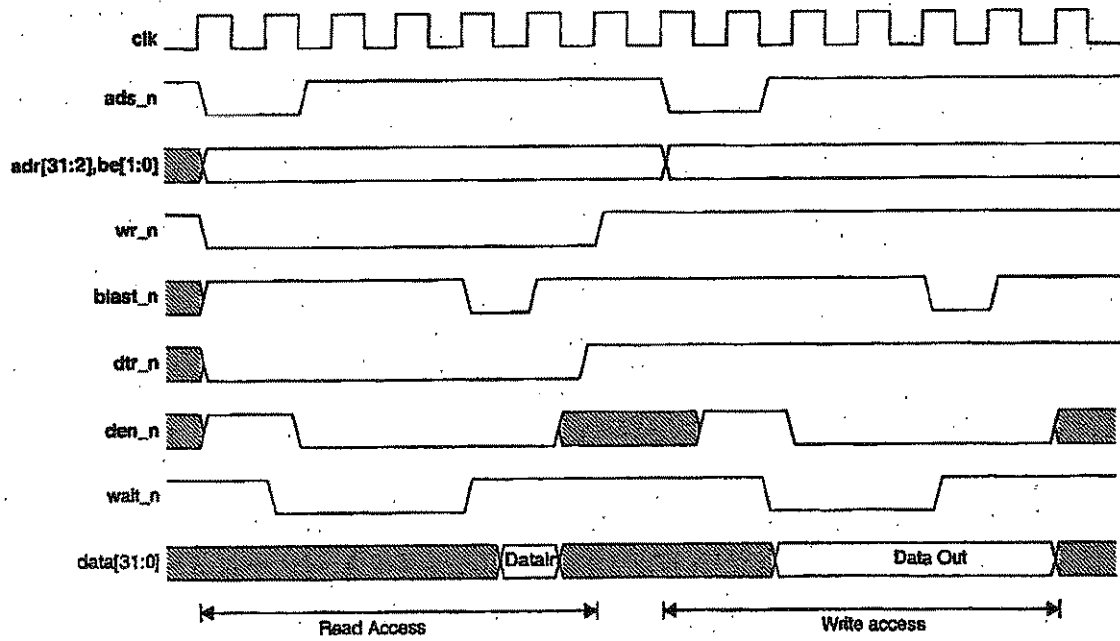


FIG. 66

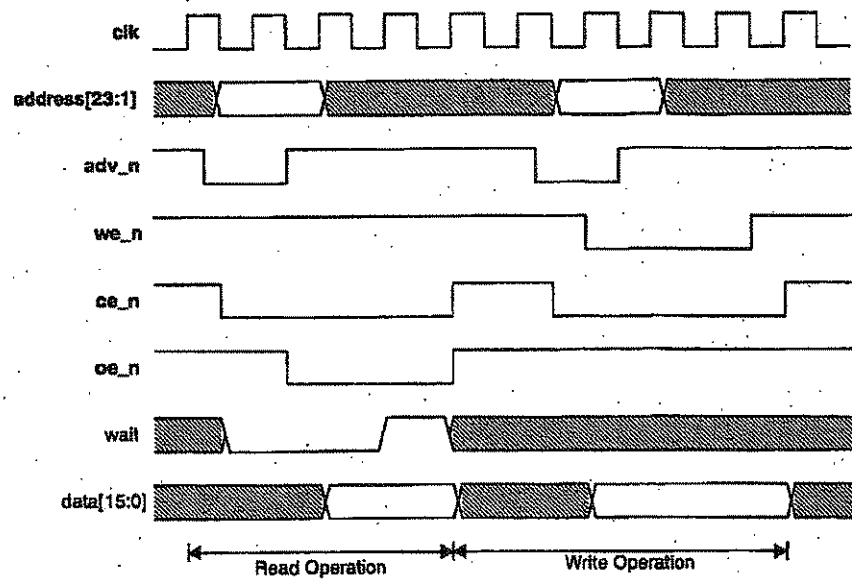


FIG. 67

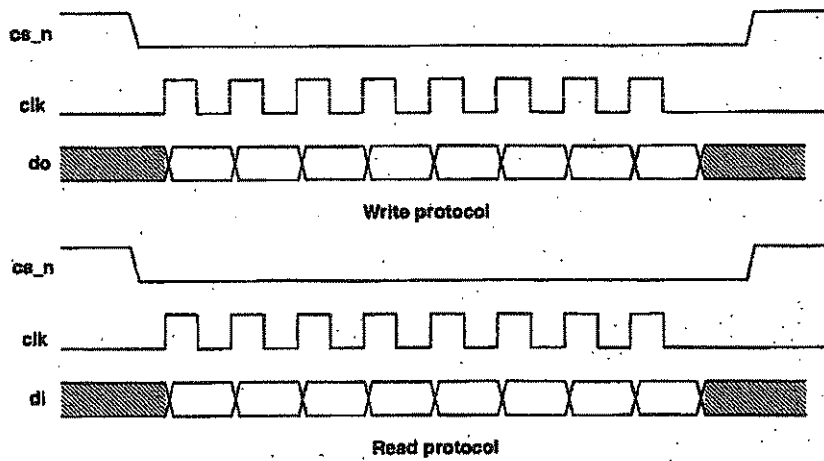


FIG. 68

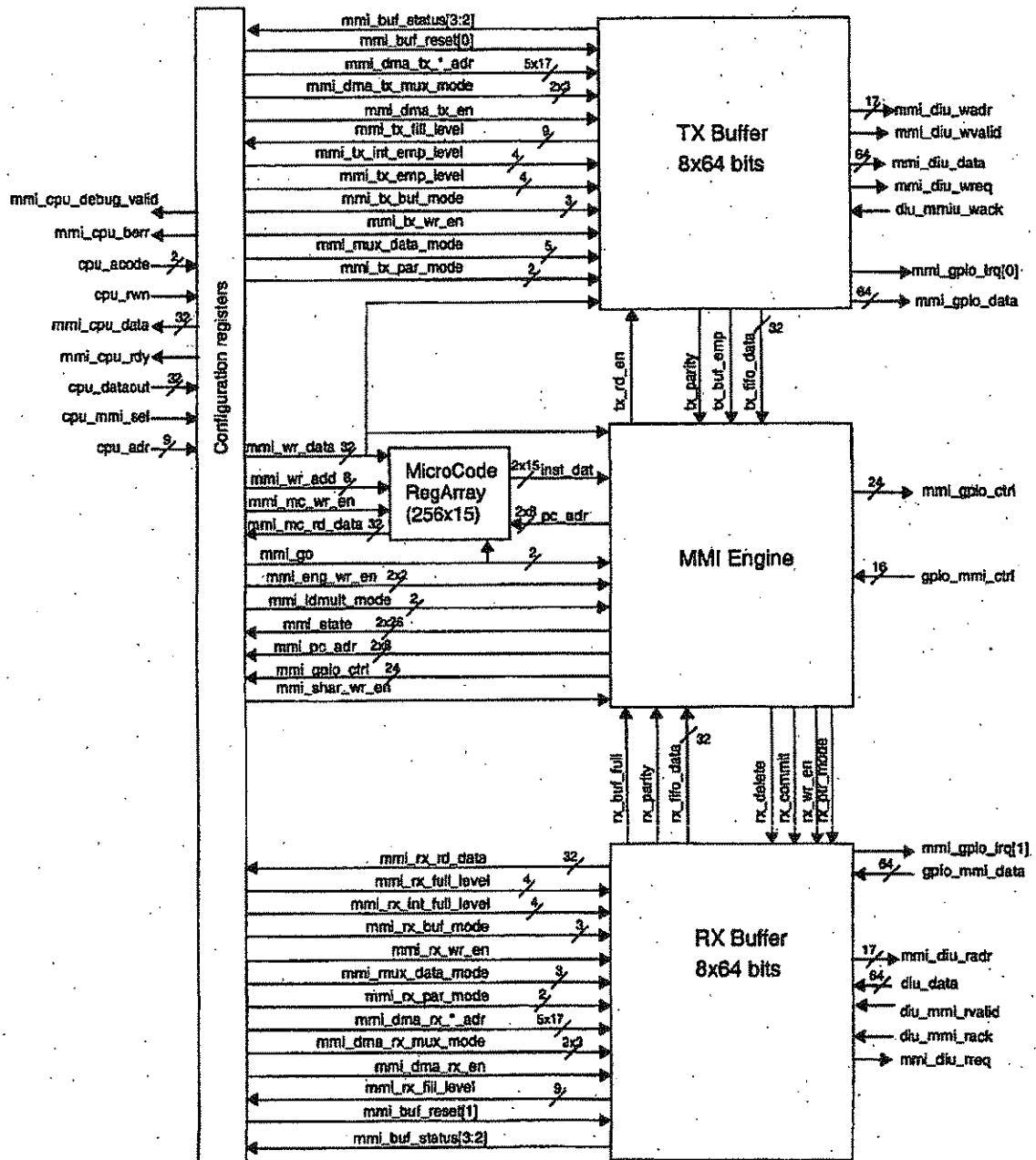


FIG. 69

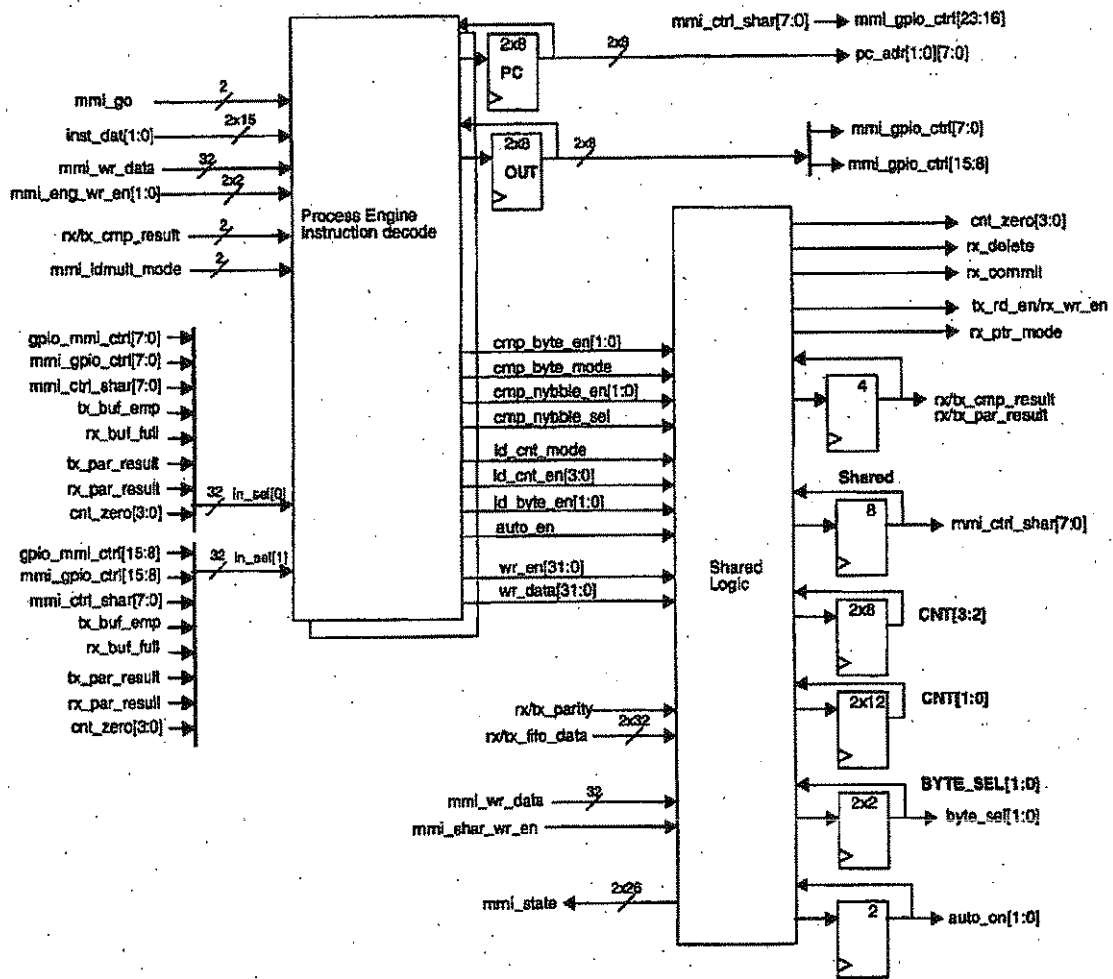


FIG. 70

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Inst	Values
BC	1
ACNT	01
LDMULT	001
CMPNYBBLE	00011
CMYBYTE	00010
LDCNT	00001
BCCMP1	000001
LOBIT	00000001
LDCNT_FIFO	000000001
LDBSEL	00000000001
RX_COMMIT	0000000000001
RX_DELETE	0000000000000

14	12	11		8	7		4	3		0
Instructions										
BC	B	IN_SEL				PC_OFFSET				
ACNT	B	NUM_CYCLES								
LDMULT	MASK				OUT_VALUE					
CMPNYBBLE				B2	B1	MASK			VALUE	
CMPBYTE				B1	ME	MASK/DATA VALUE				
LDCNT				SEL		NUM_COUNT				
BCCMP1					B	PC_OFFSET				
LDBIT						B	OUT_SEL			
LDCNT_FIFO							B	SEL	NYB	
LDBSEL								B	SEL	
RX_COMMIT										
RX_DELETE										

FIG. 71

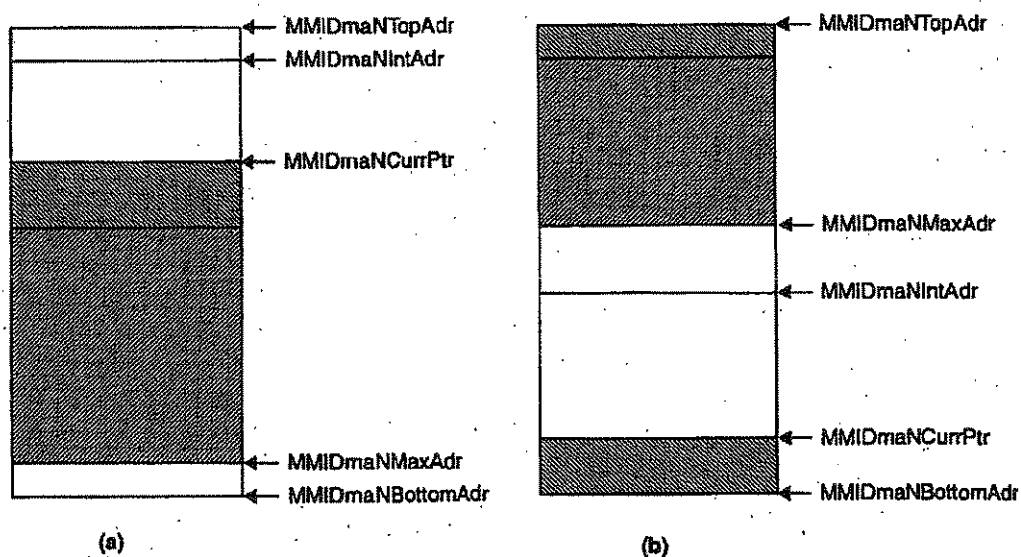


FIG. 72

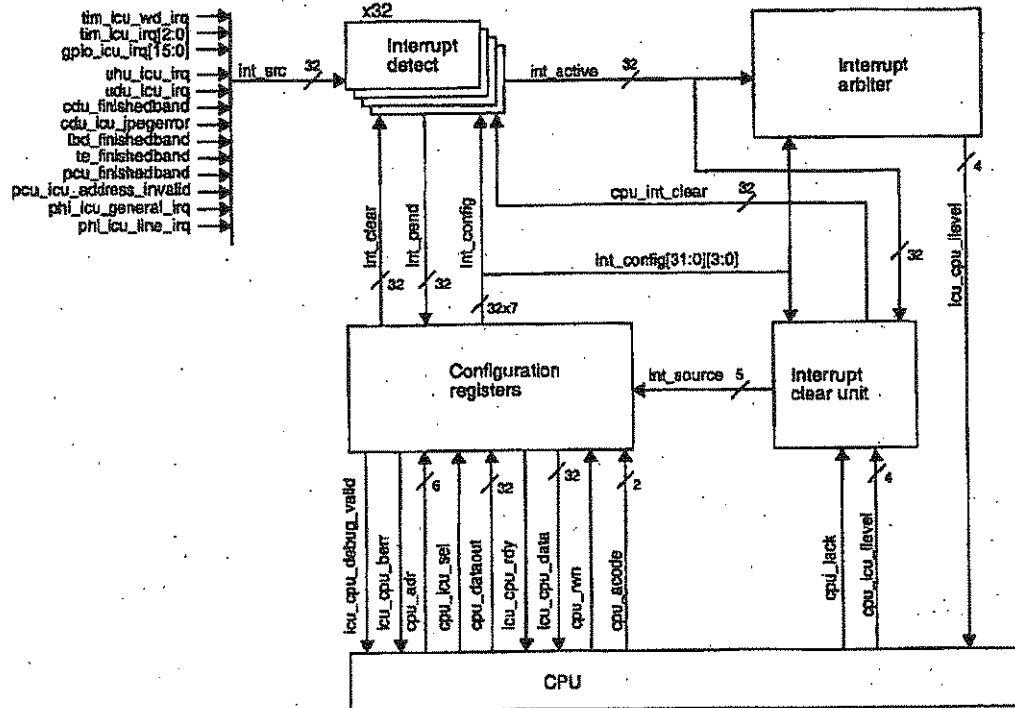
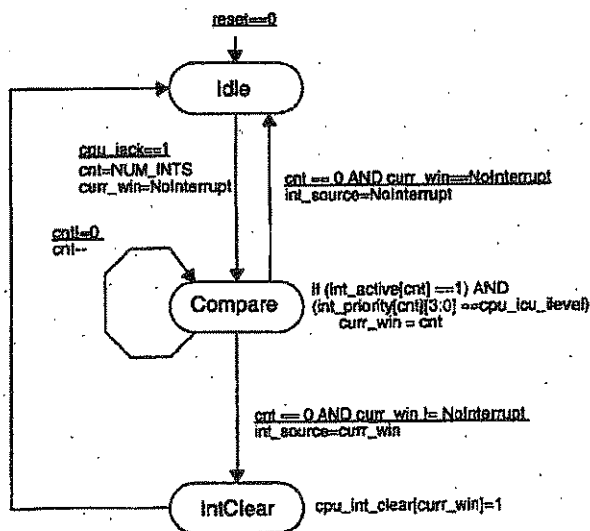


FIG. 73



Machine remains in same state by default
All outputs are zero unless otherwise stated

State Description:

- Idle: Normal Idle state
- Compare: Compare interrupt level. Determines the interrupt source
- IntClear: Interrupt clear, clear the pending bit for the current interrupt vector

FIG. 74

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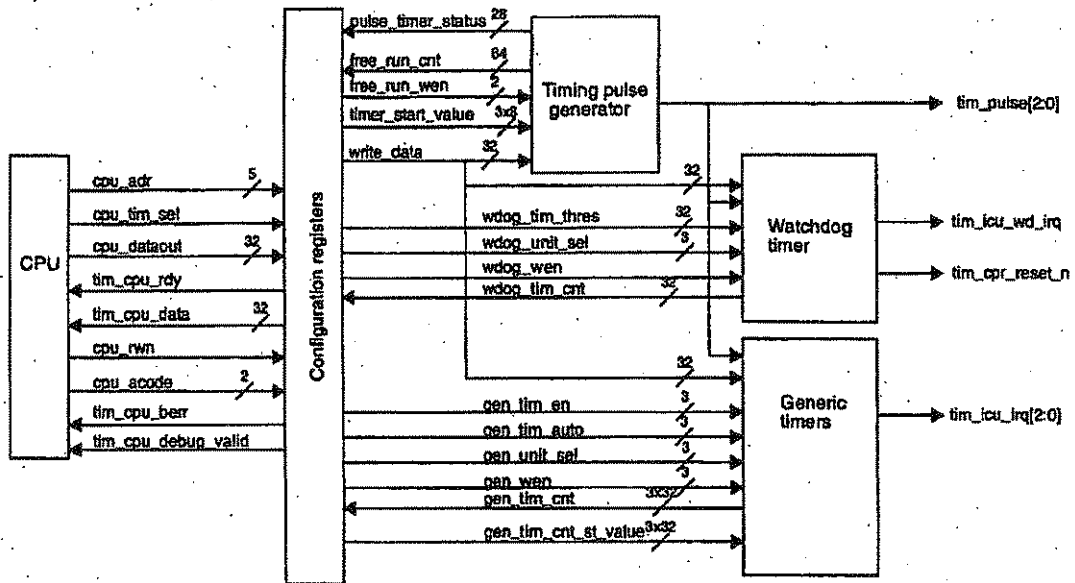


FIG. 75

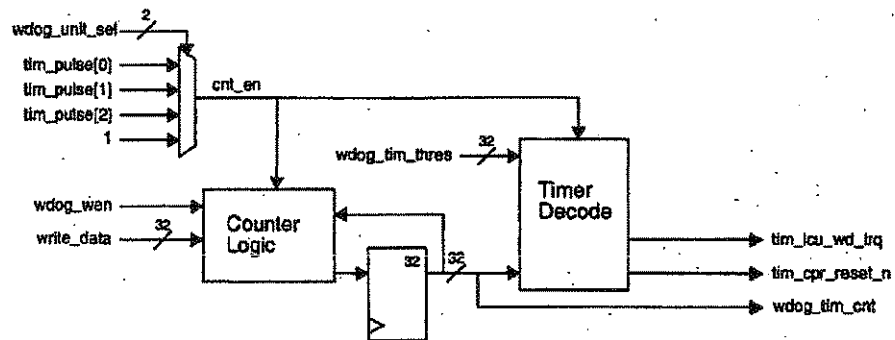


FIG. 76

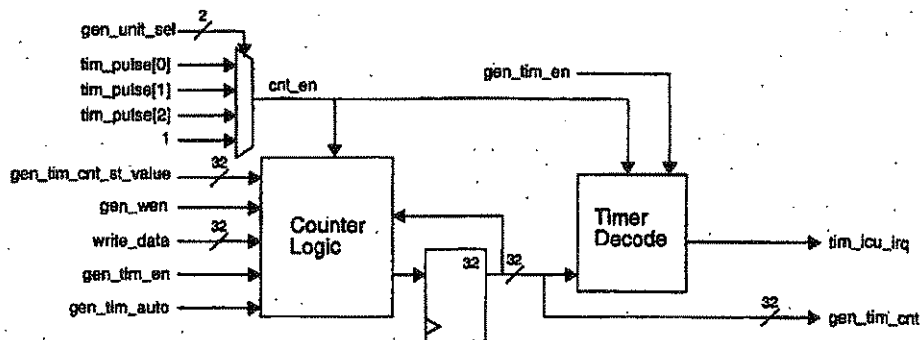


FIG. 77

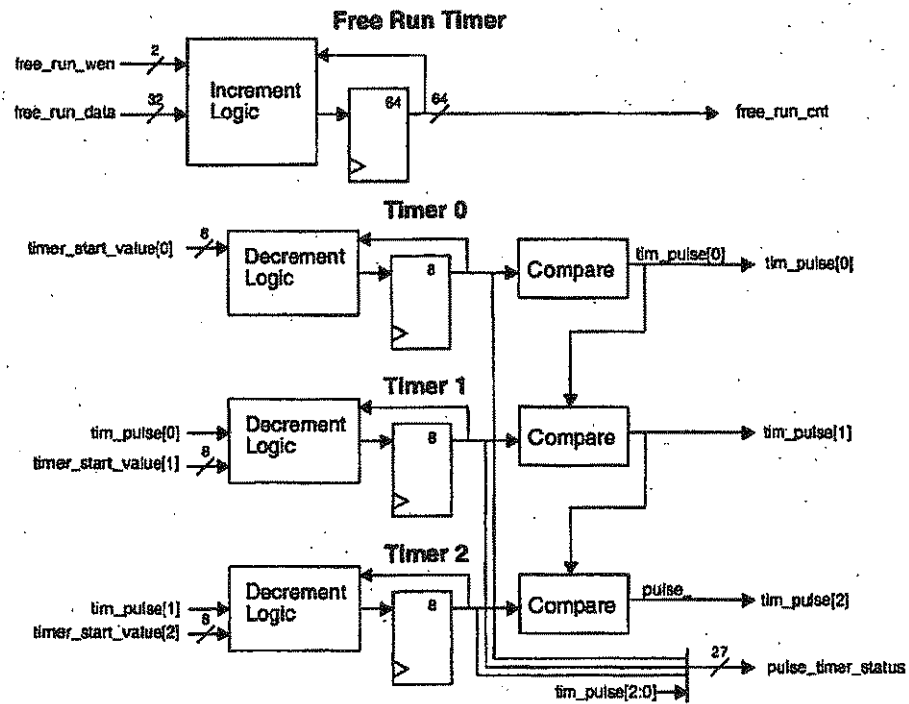


FIG. 78

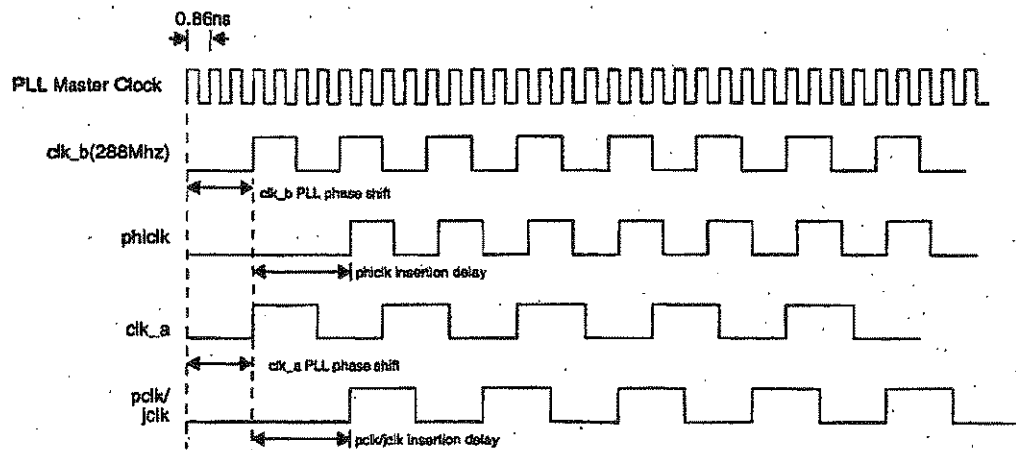


FIG. 79

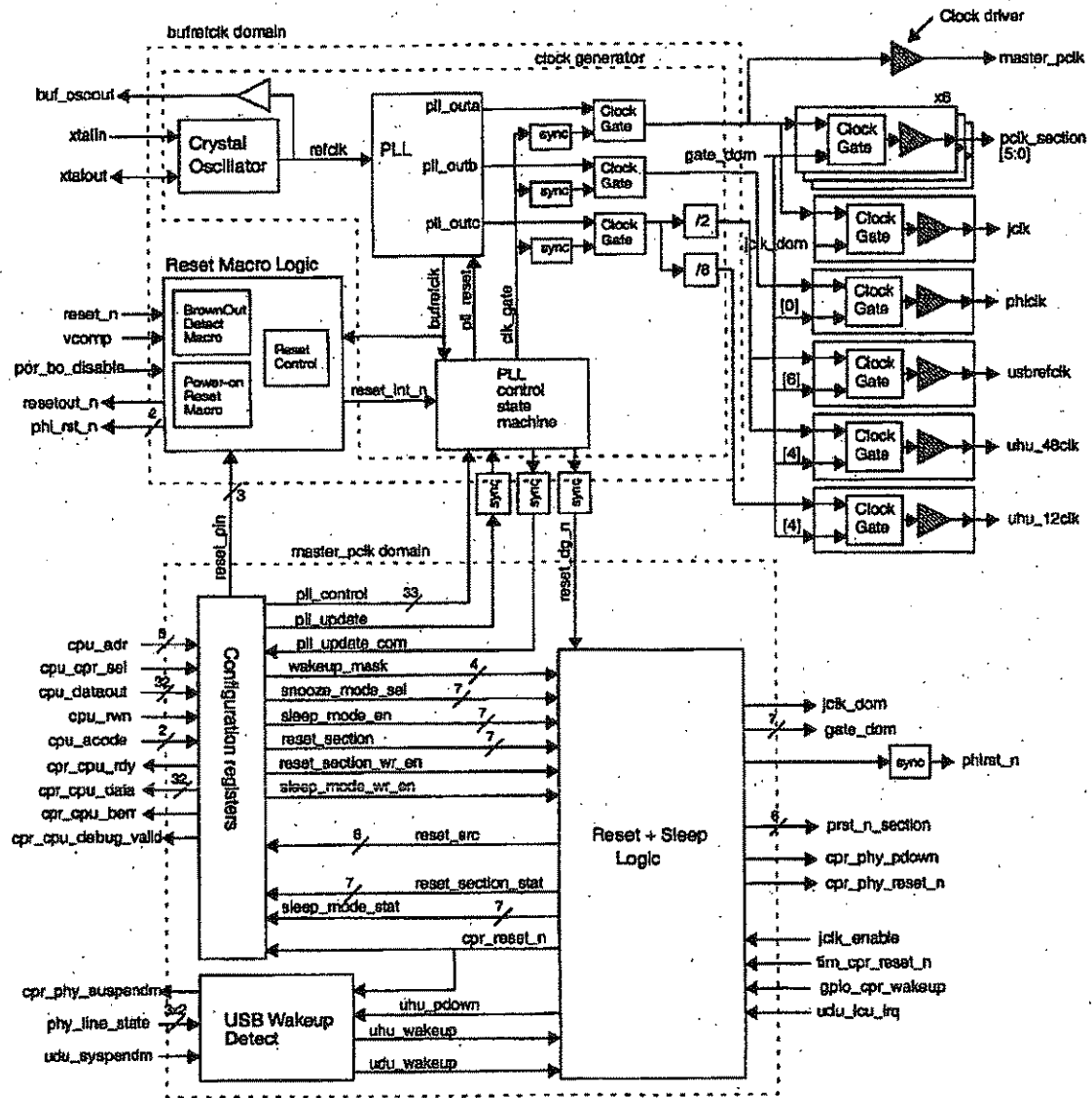
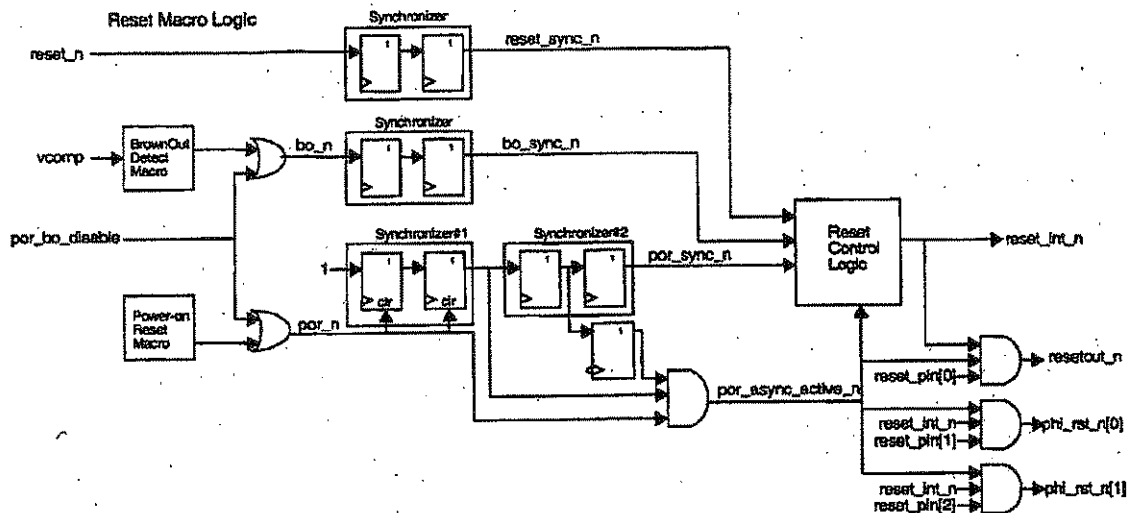


FIG. 80



Note: All logic clocked on bufrefclk unless otherwise indicated

FIG. 81

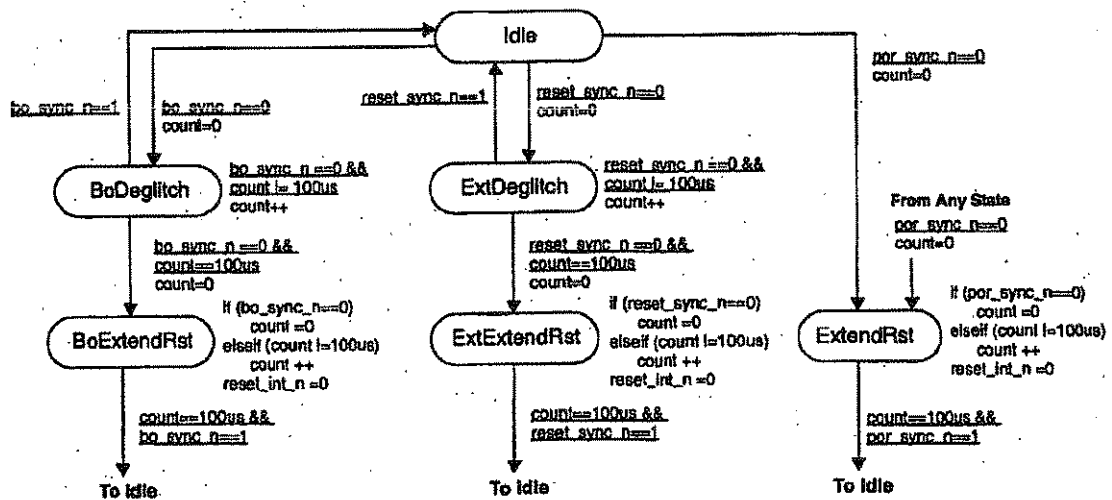


FIG. 82

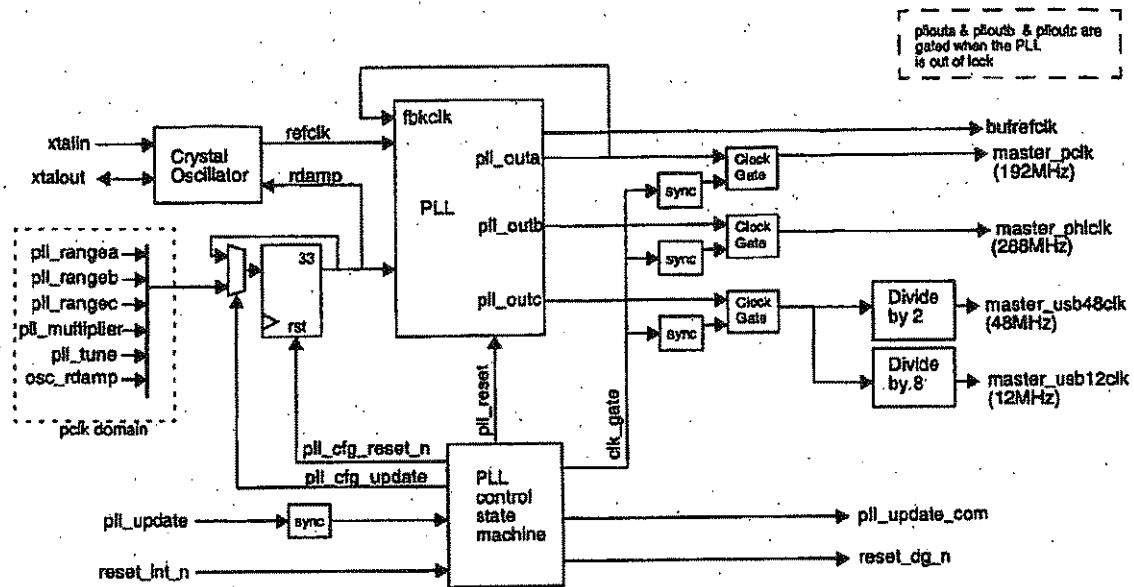


FIG. 83

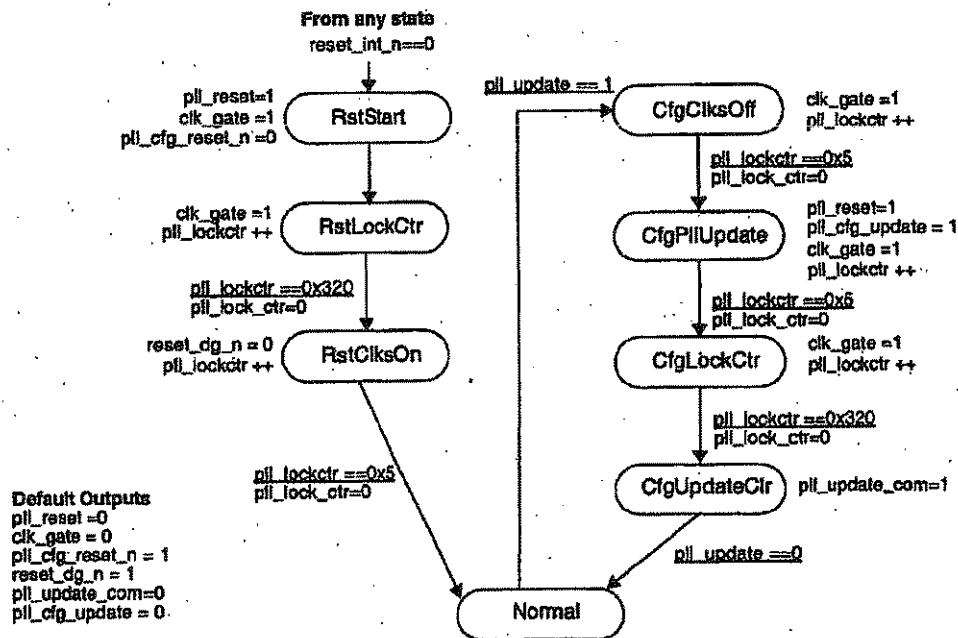


FIG. 84

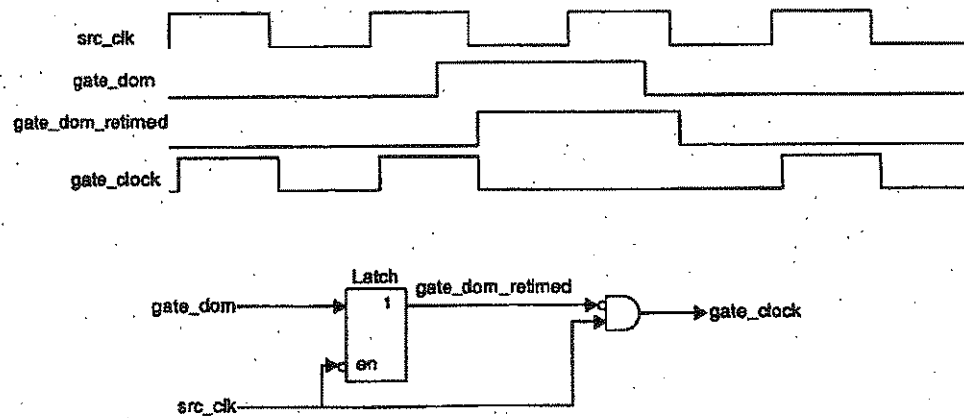


FIG. 85

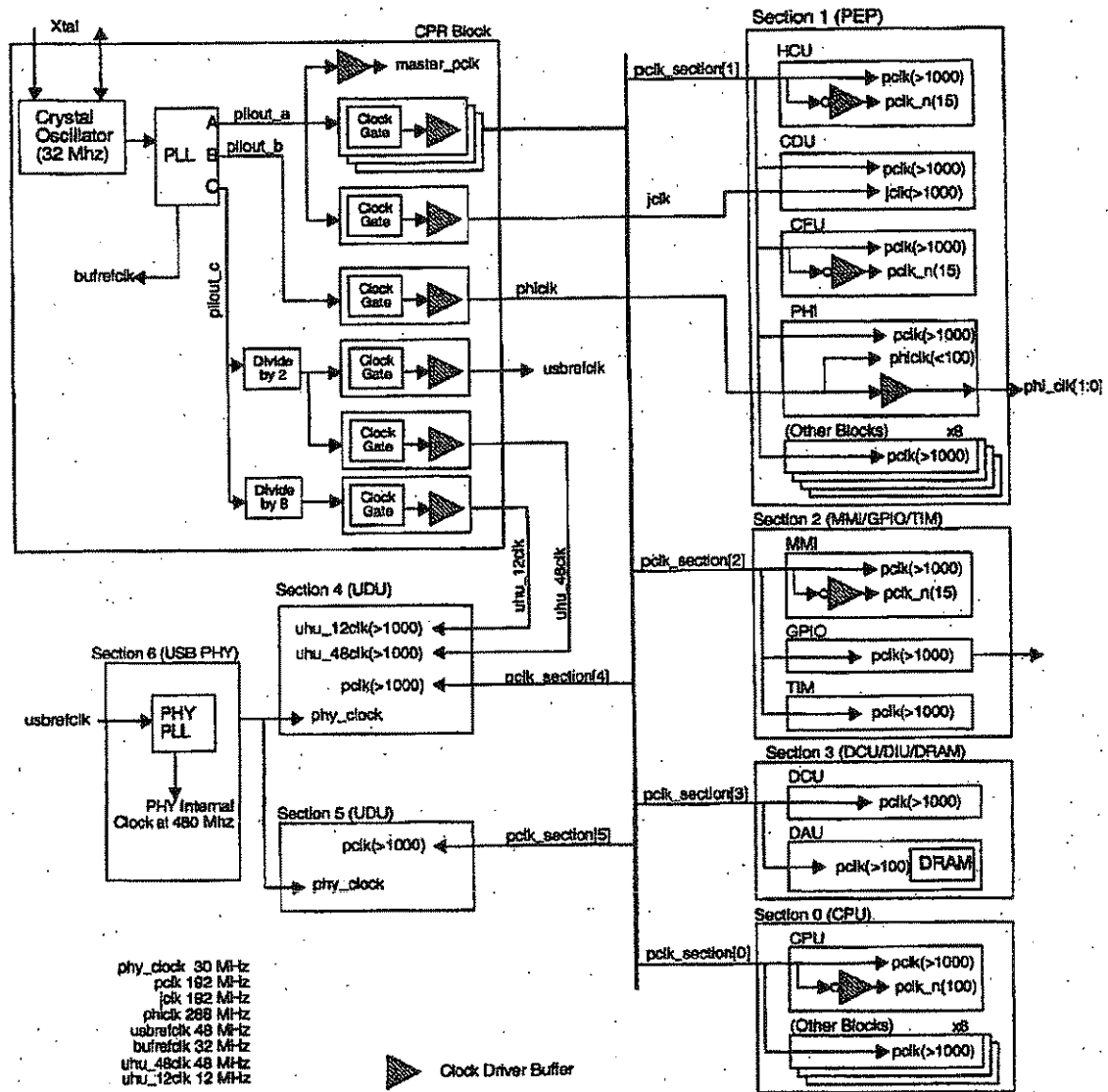


FIG. 86

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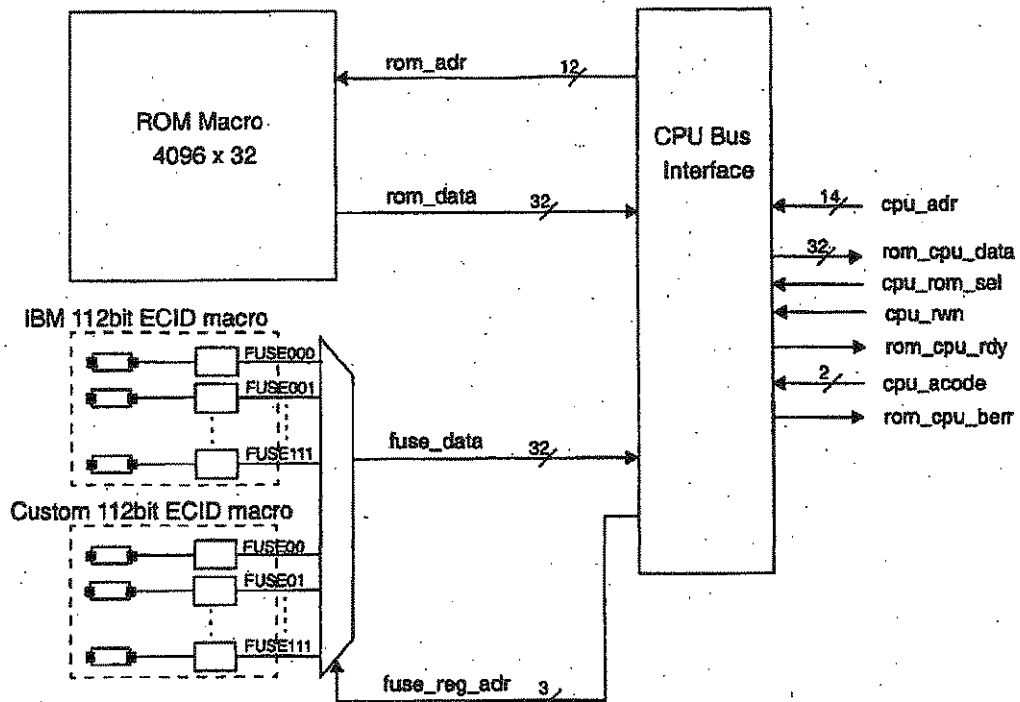


FIG. 87

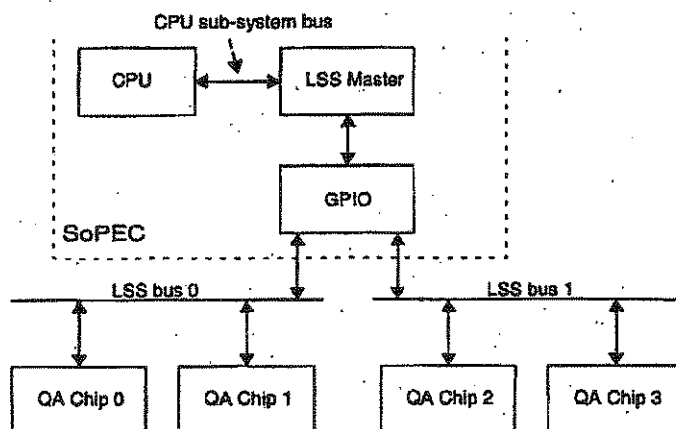


FIG. 88

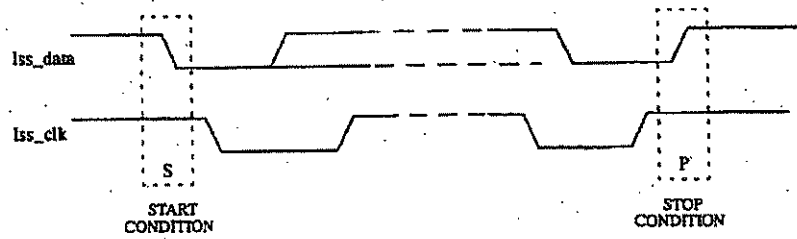


FIG. 89

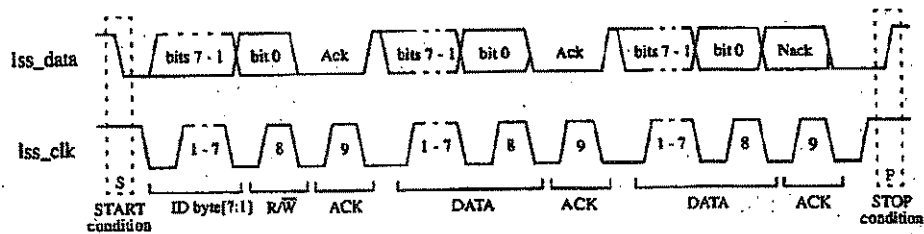


FIG. 90

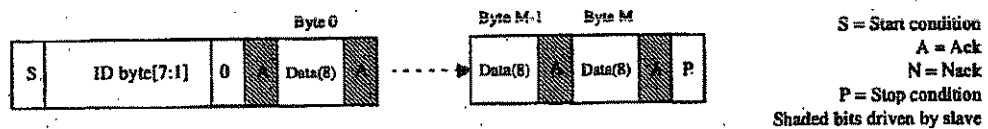


FIG. 91

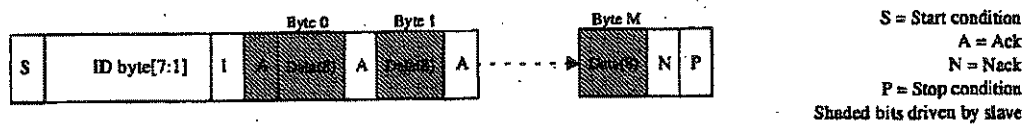


FIG. 92

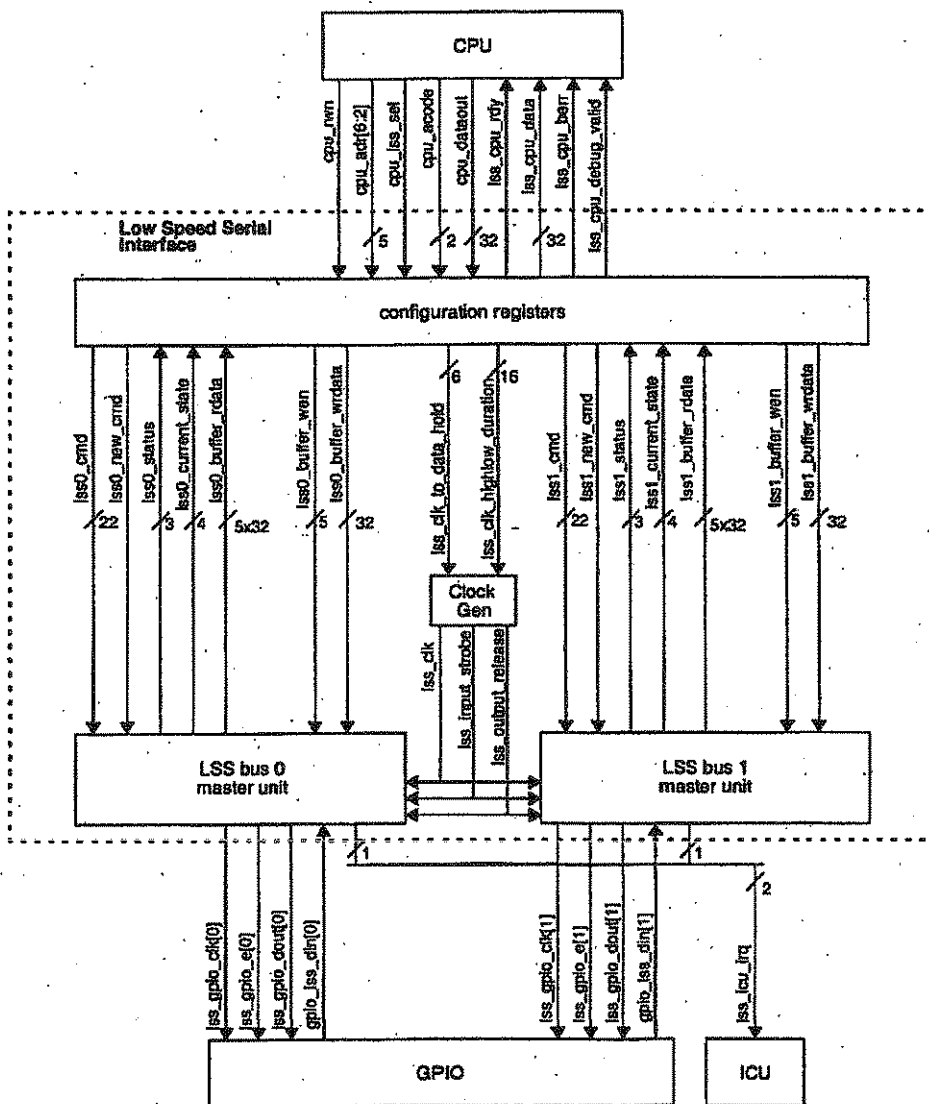


FIG. 93

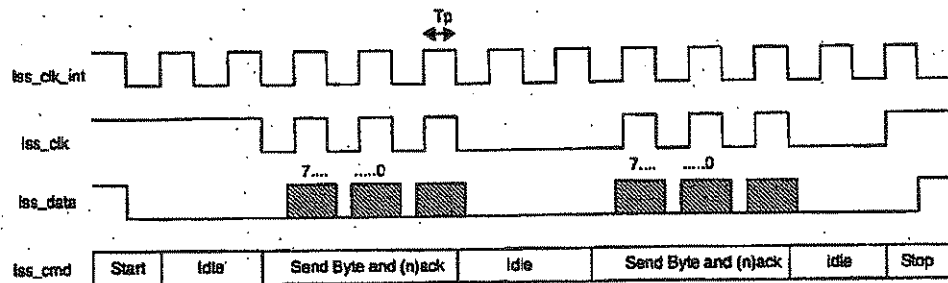


FIG. 94

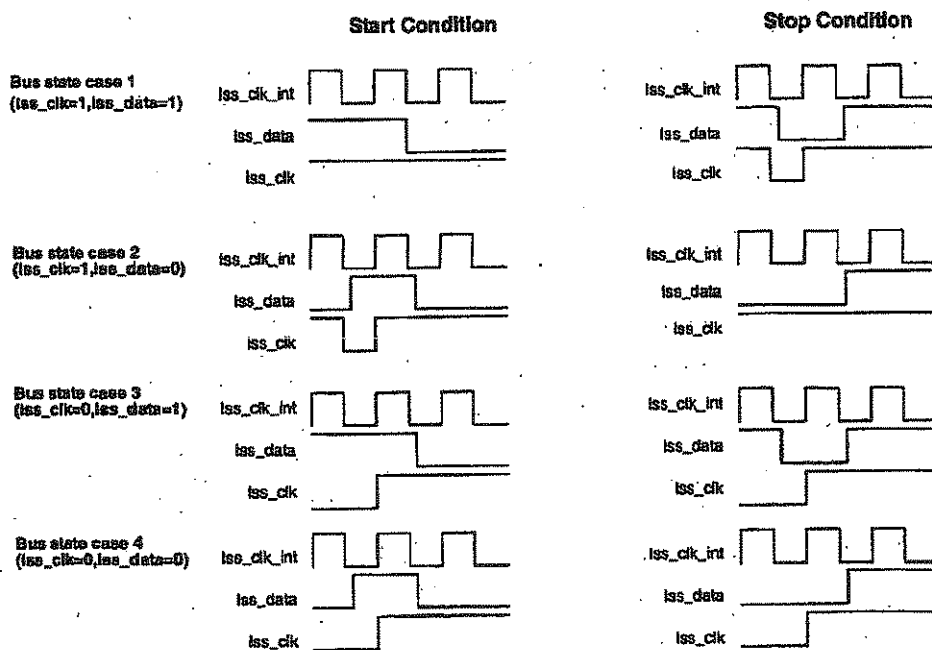


FIG. 95

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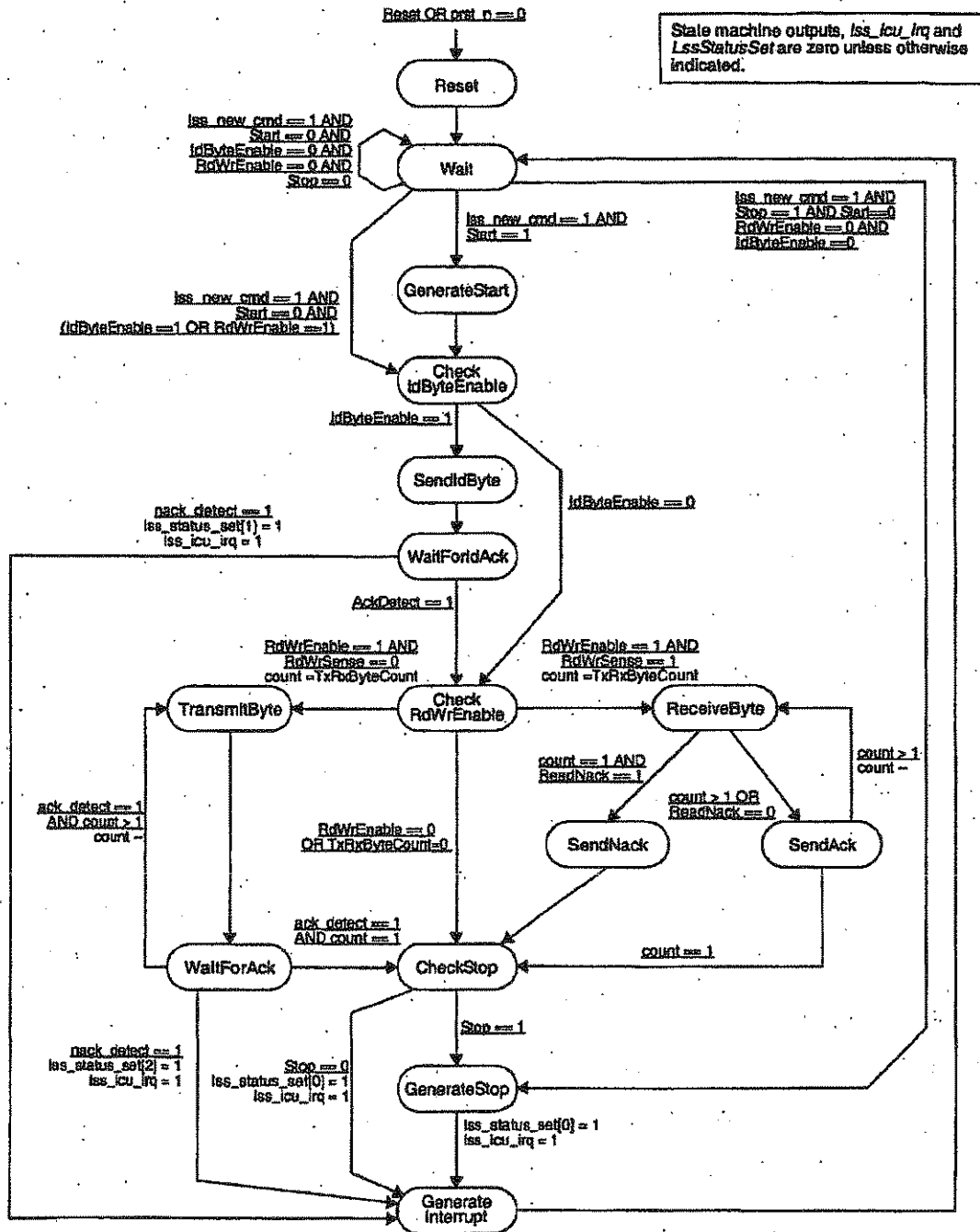


FIG. 96

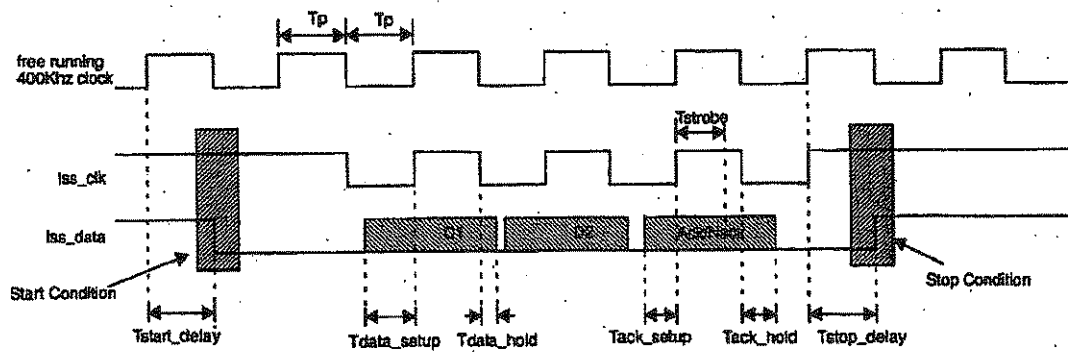


FIG. 97

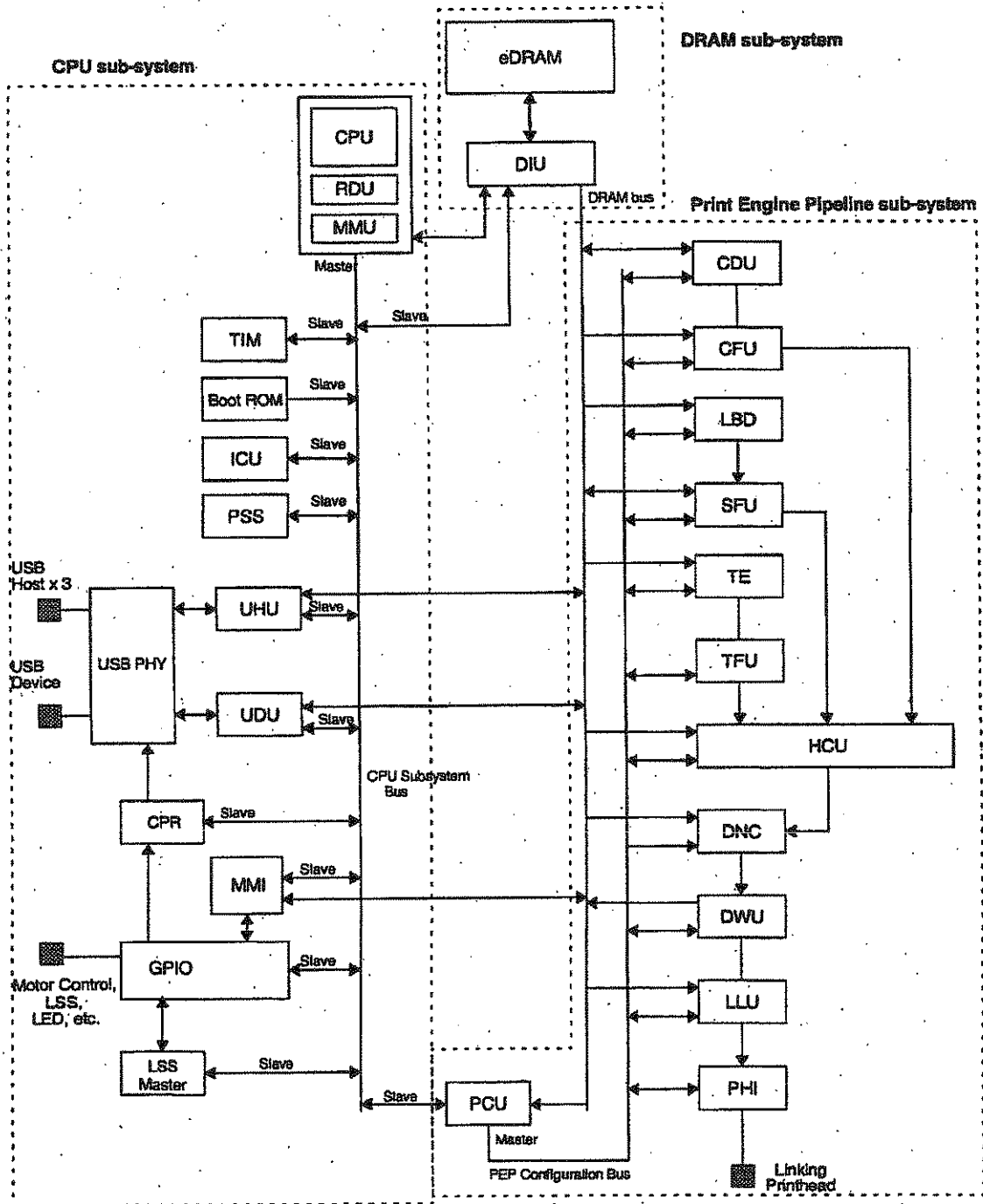


FIG. 98

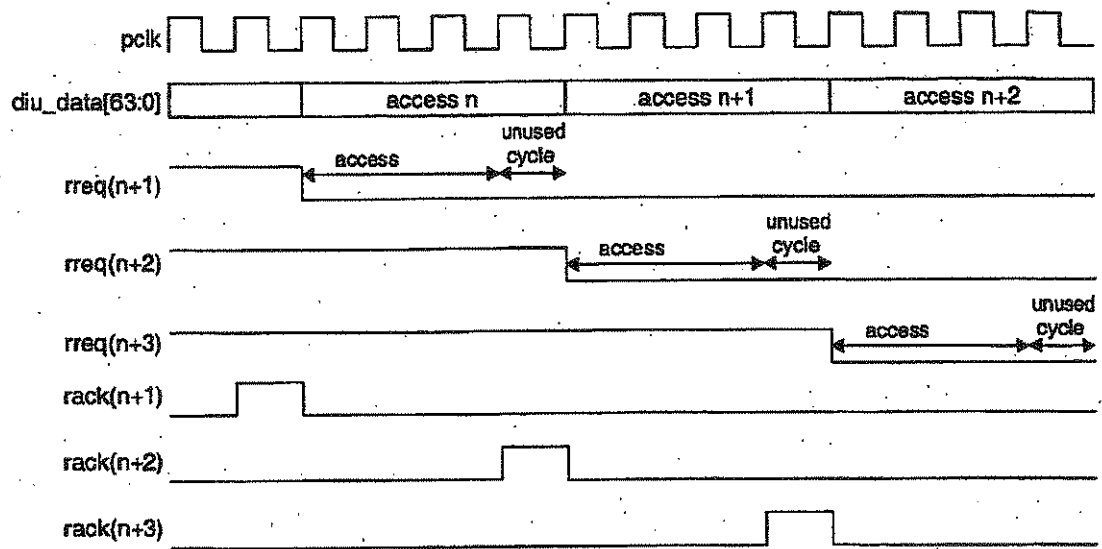


FIG. 99

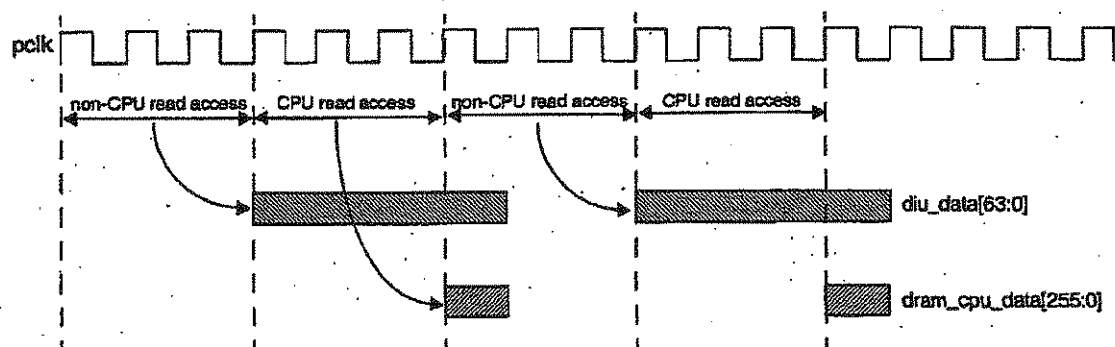


FIG. 100

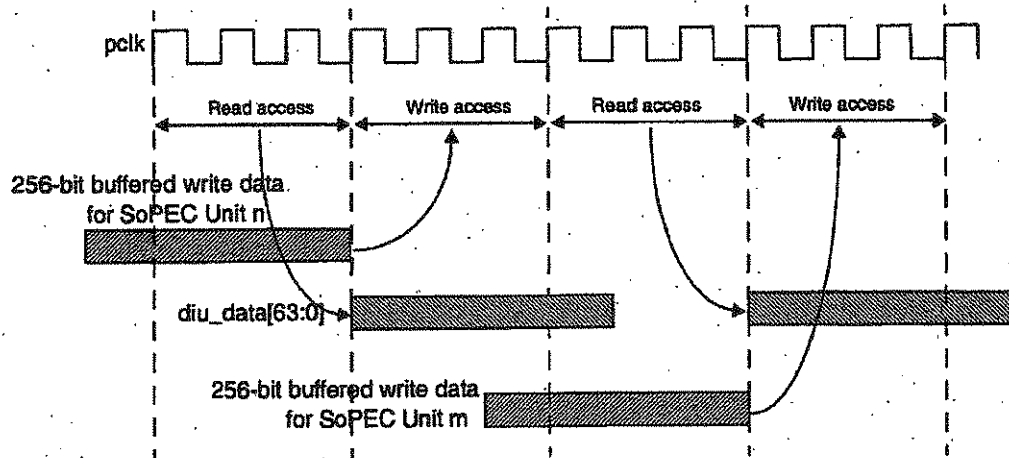


FIG. 101

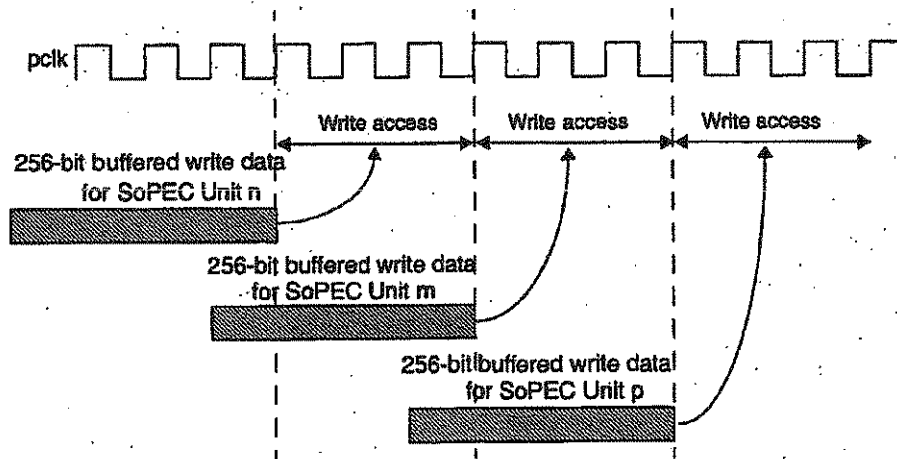


FIG. 102

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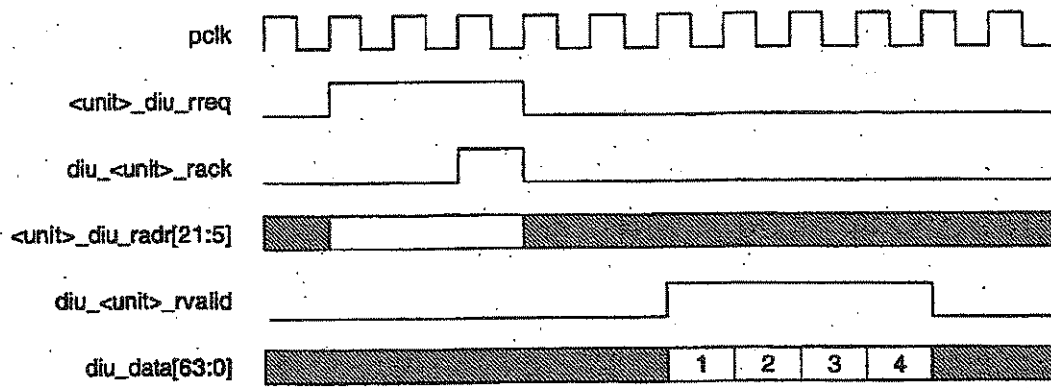


FIG. 103

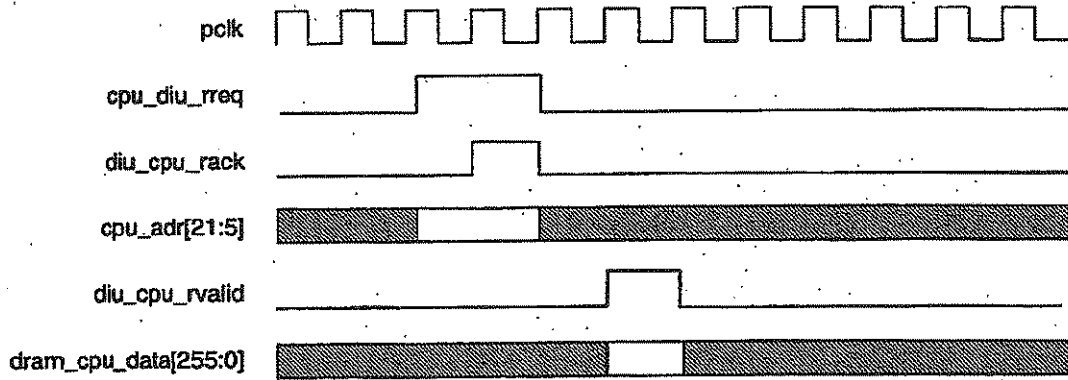


FIG. 104

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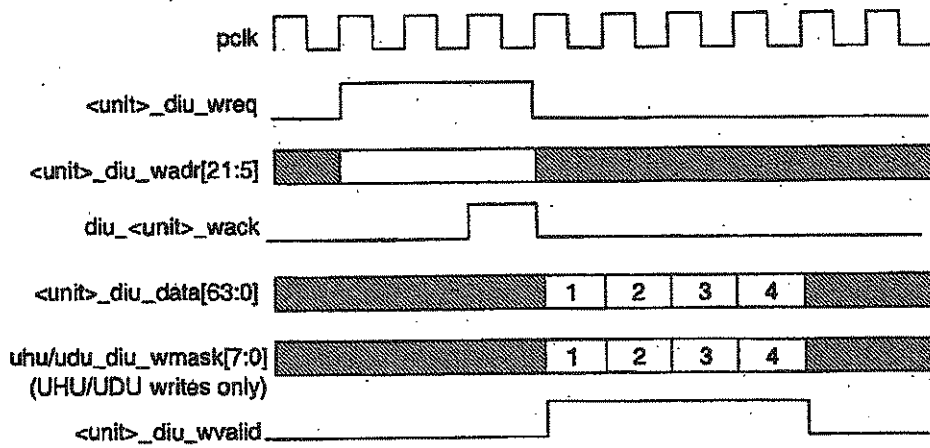


FIG. 105

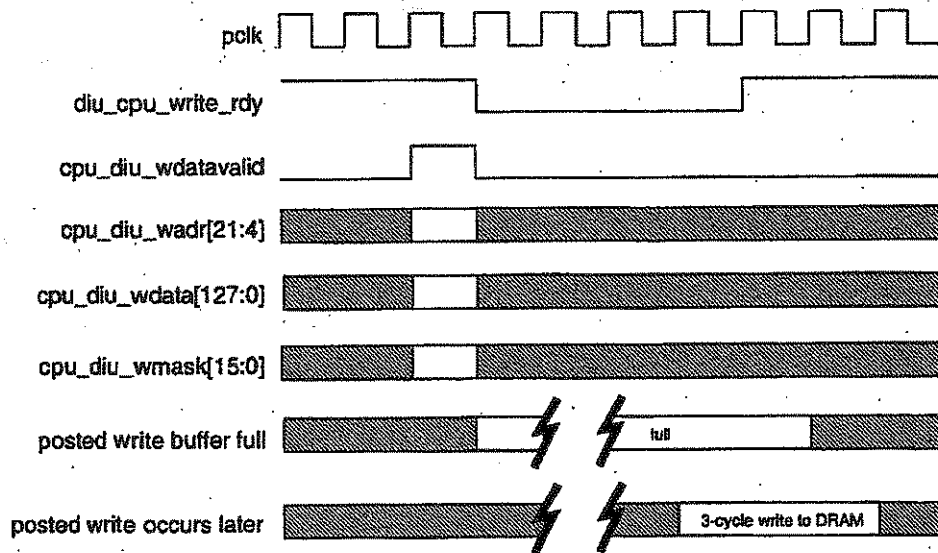


FIG. 106

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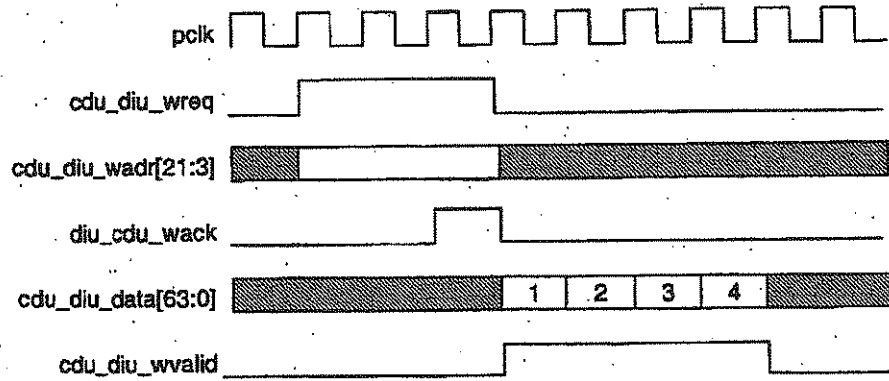


FIG. 107

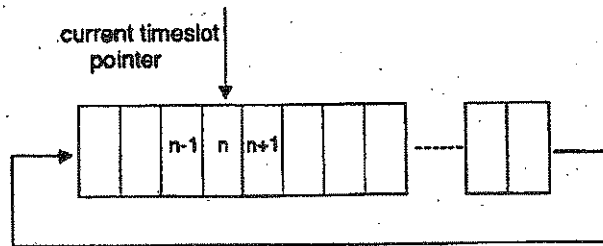


FIG. 108

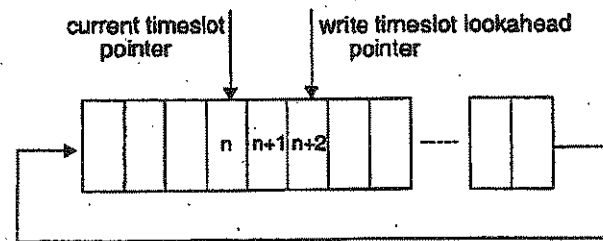


FIG. 109

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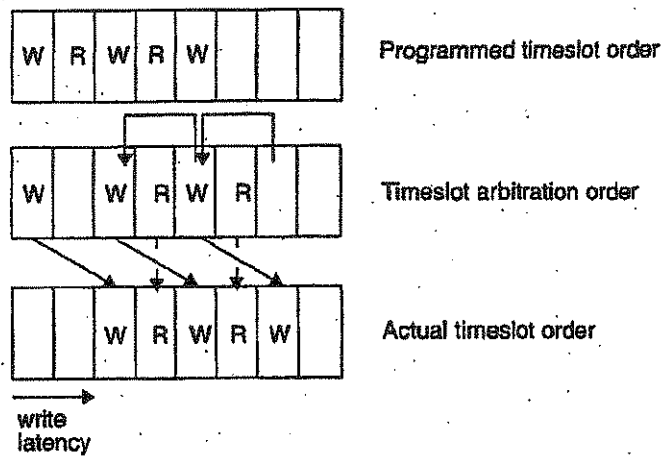


FIG. 110

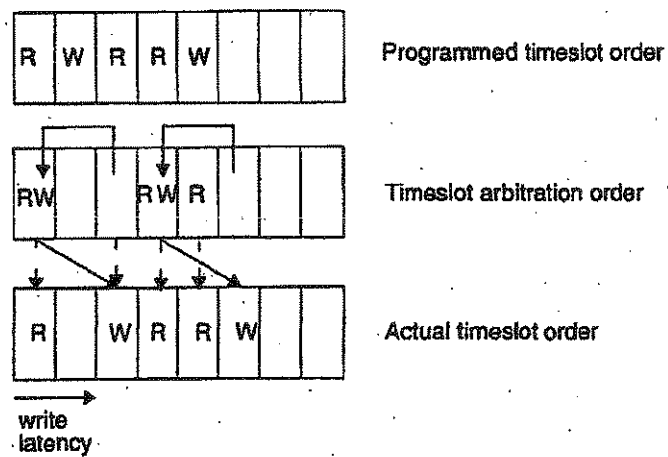


FIG. 111

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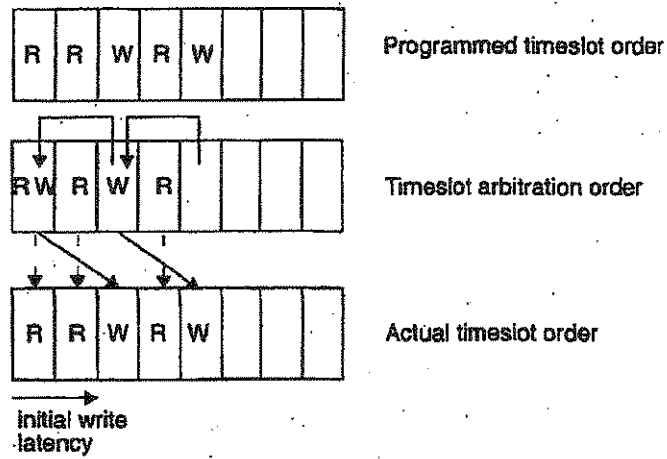


FIG. 112

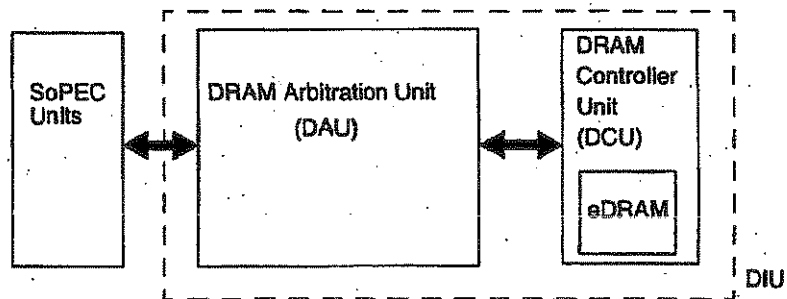


FIG. 113

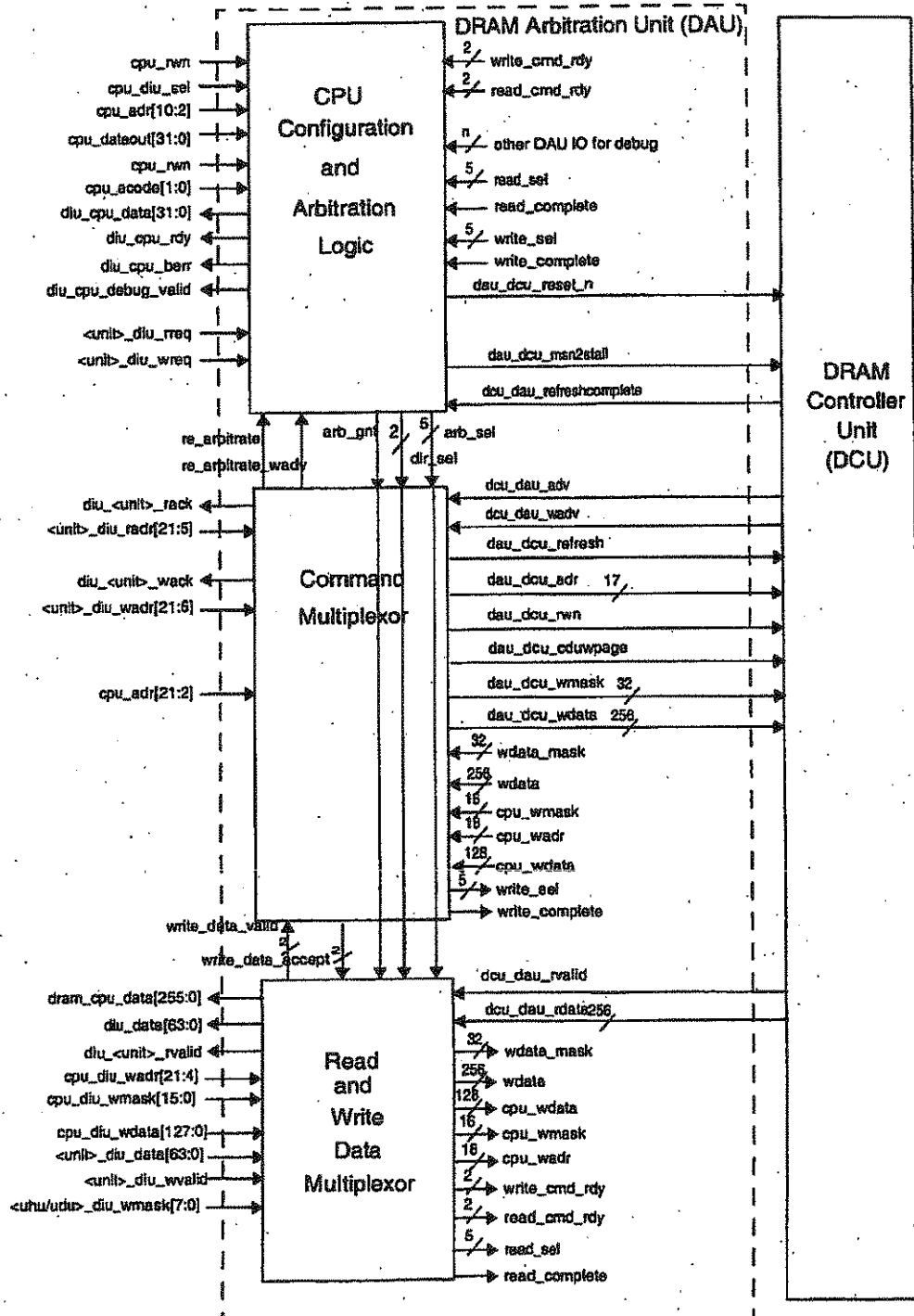


FIG. 114

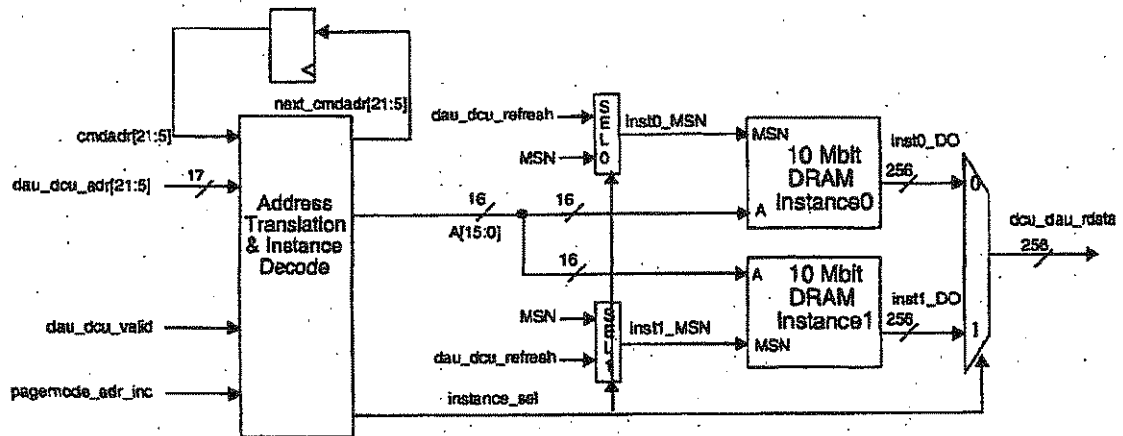


FIG. 115

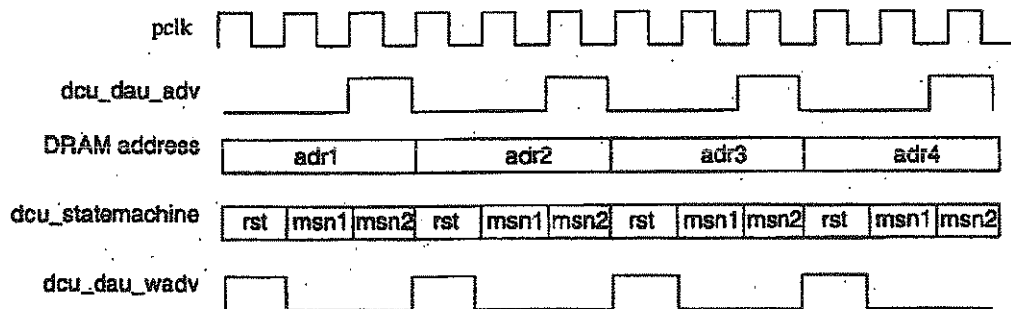


FIG. 116

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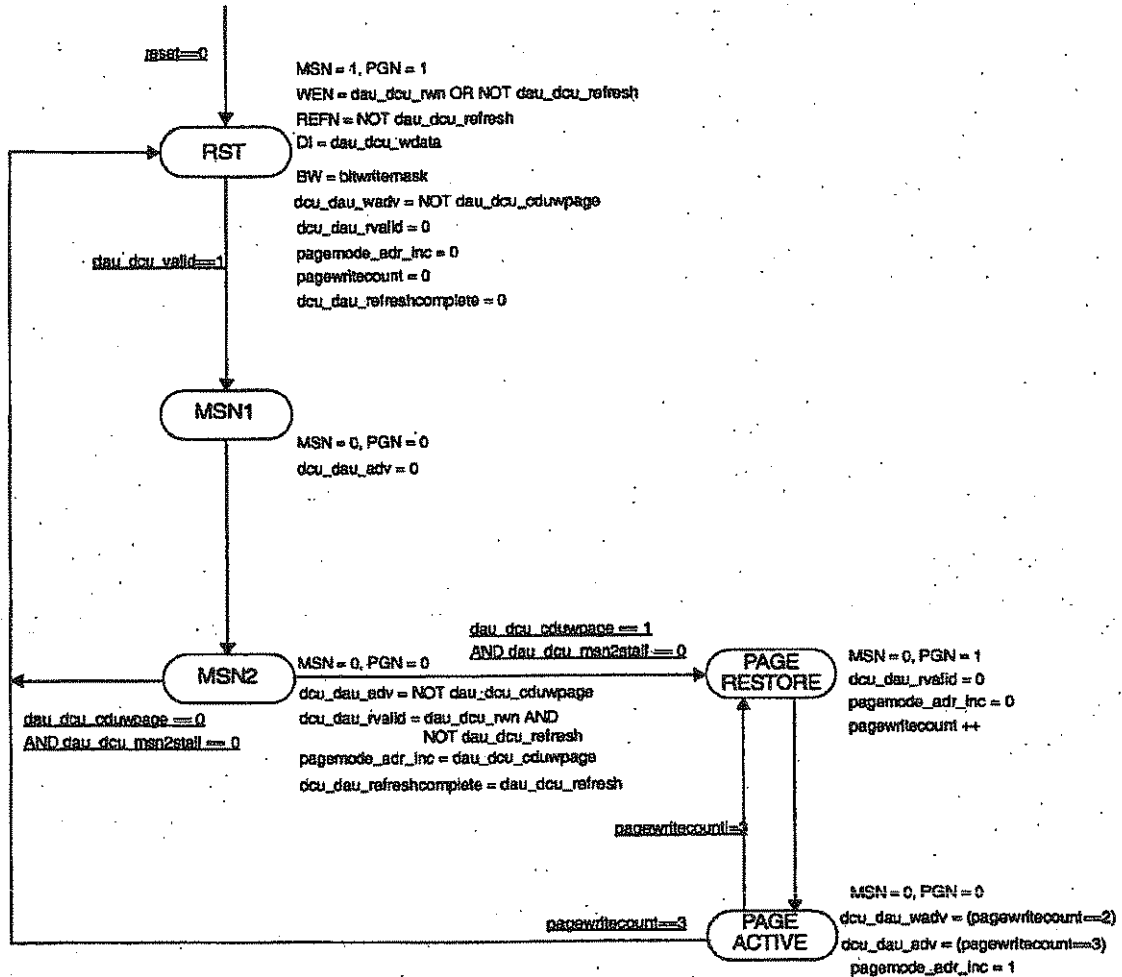


FIG. 117

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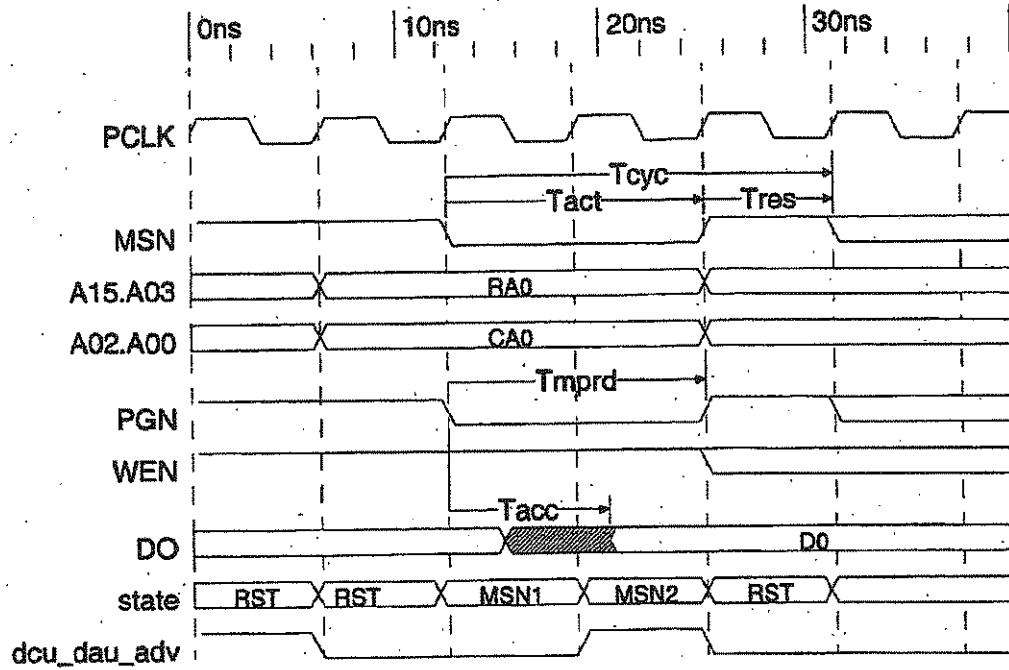


FIG. 118

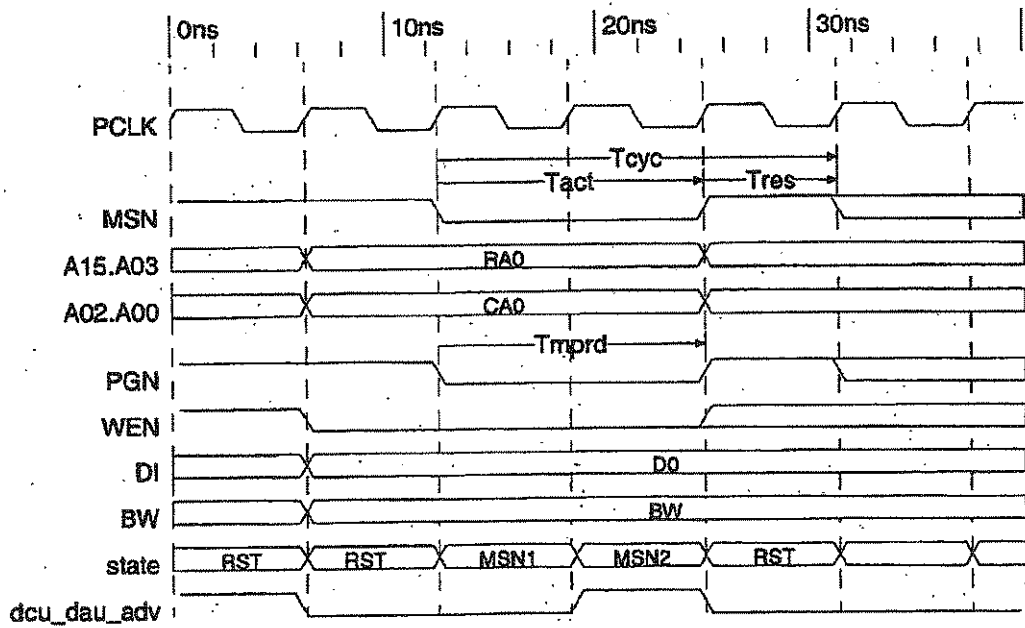


FIG. 119

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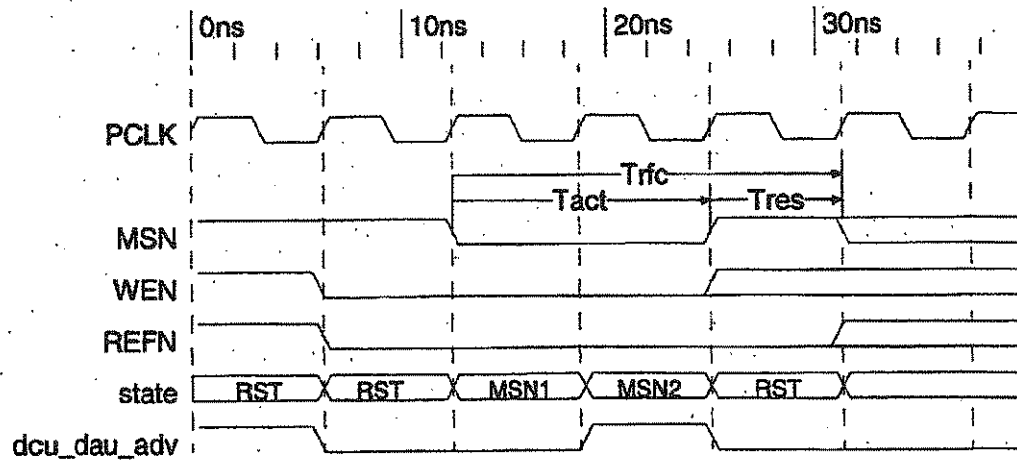


FIG. 120

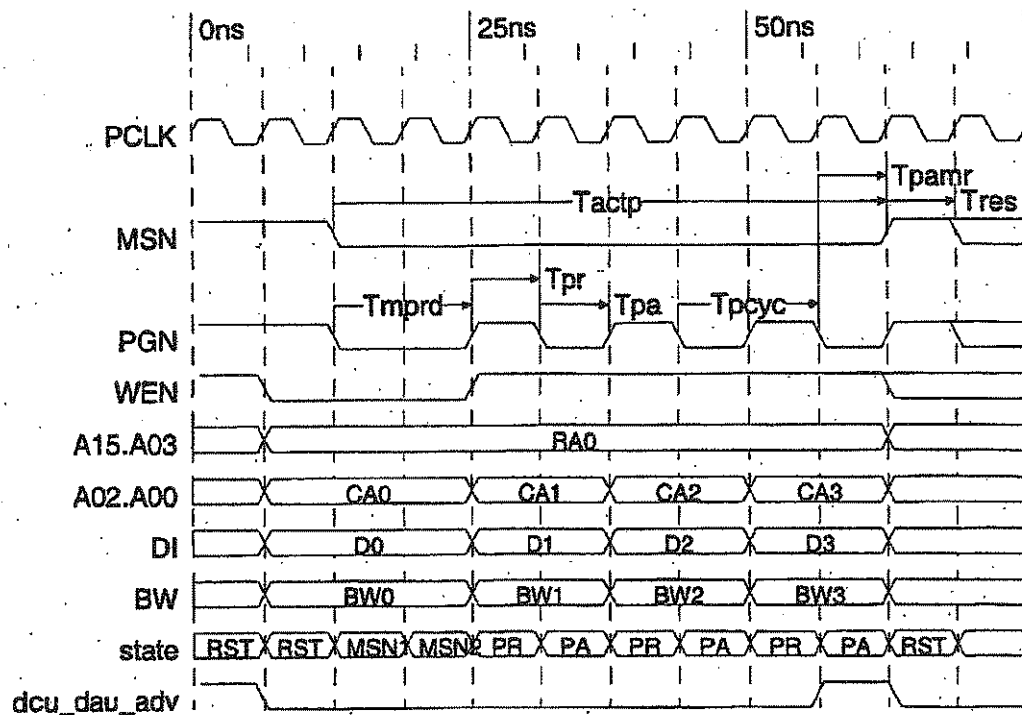


FIG. 121

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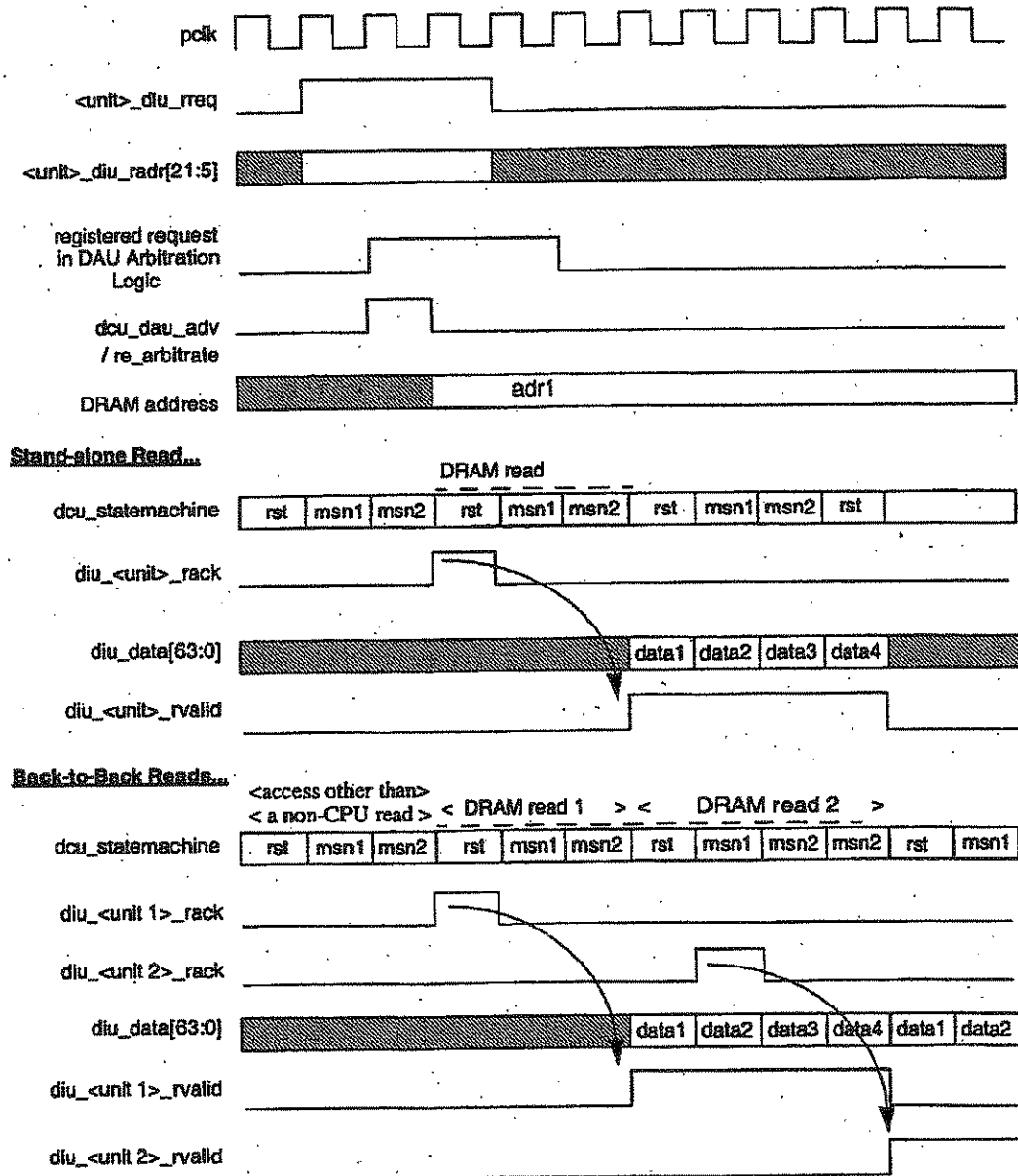


FIG. 122

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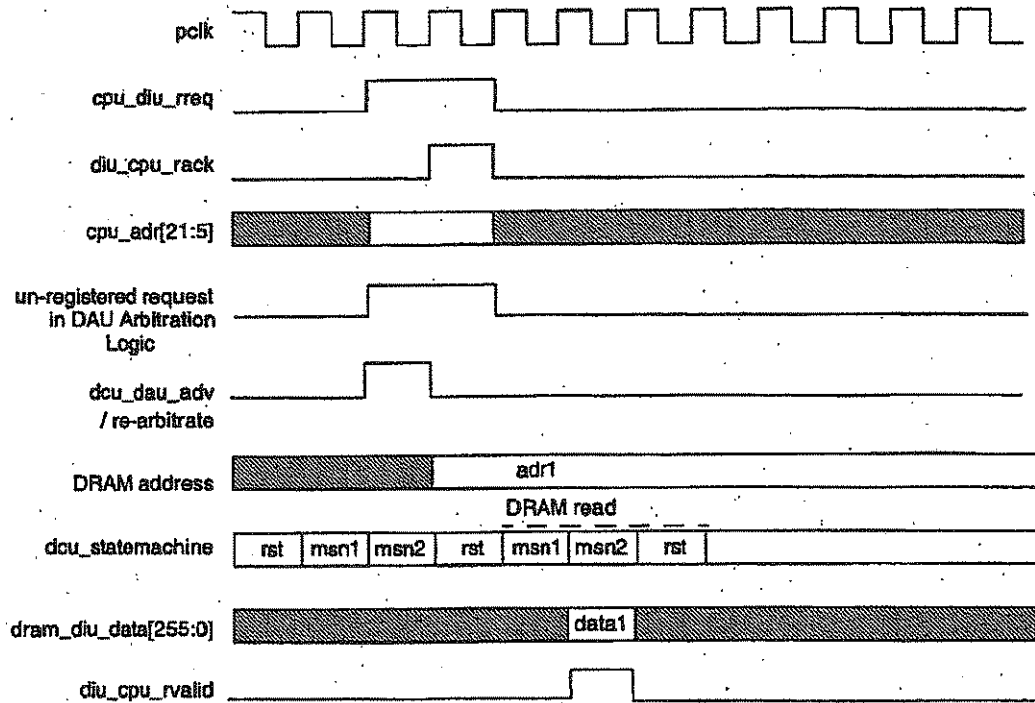


FIG. 123

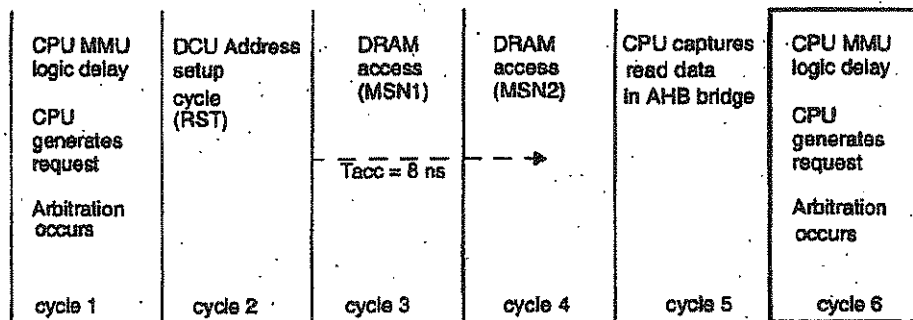


FIG. 124

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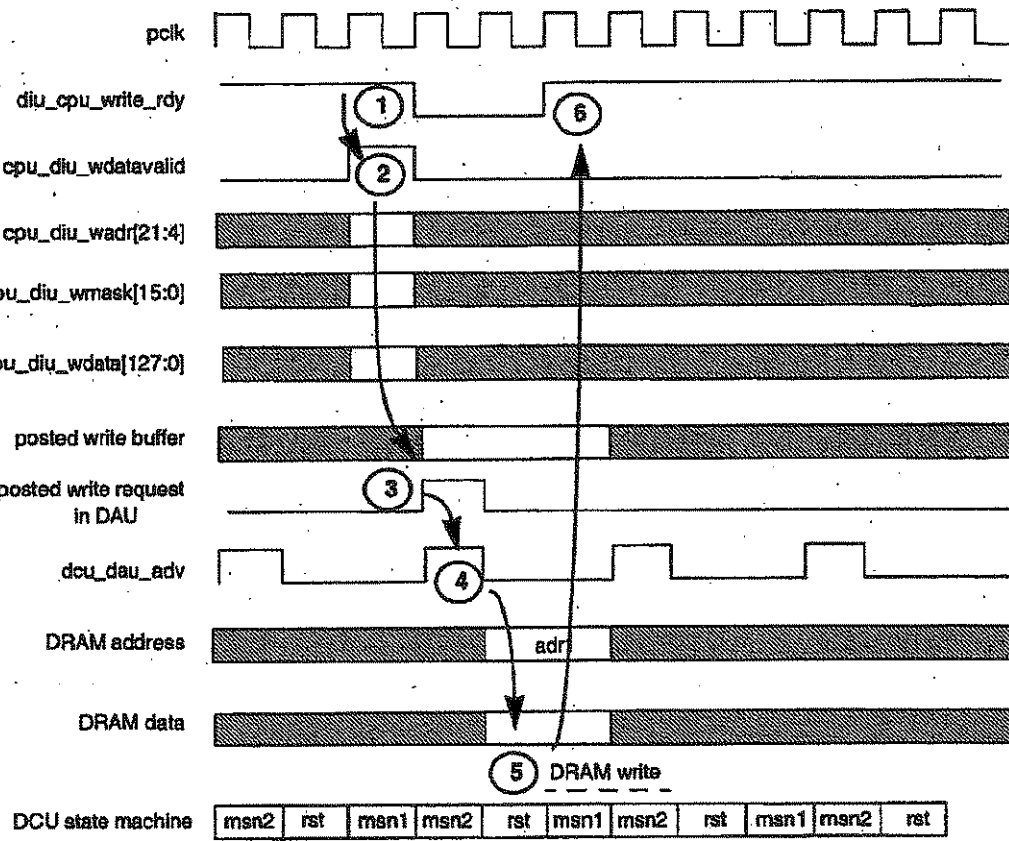


FIG. 125

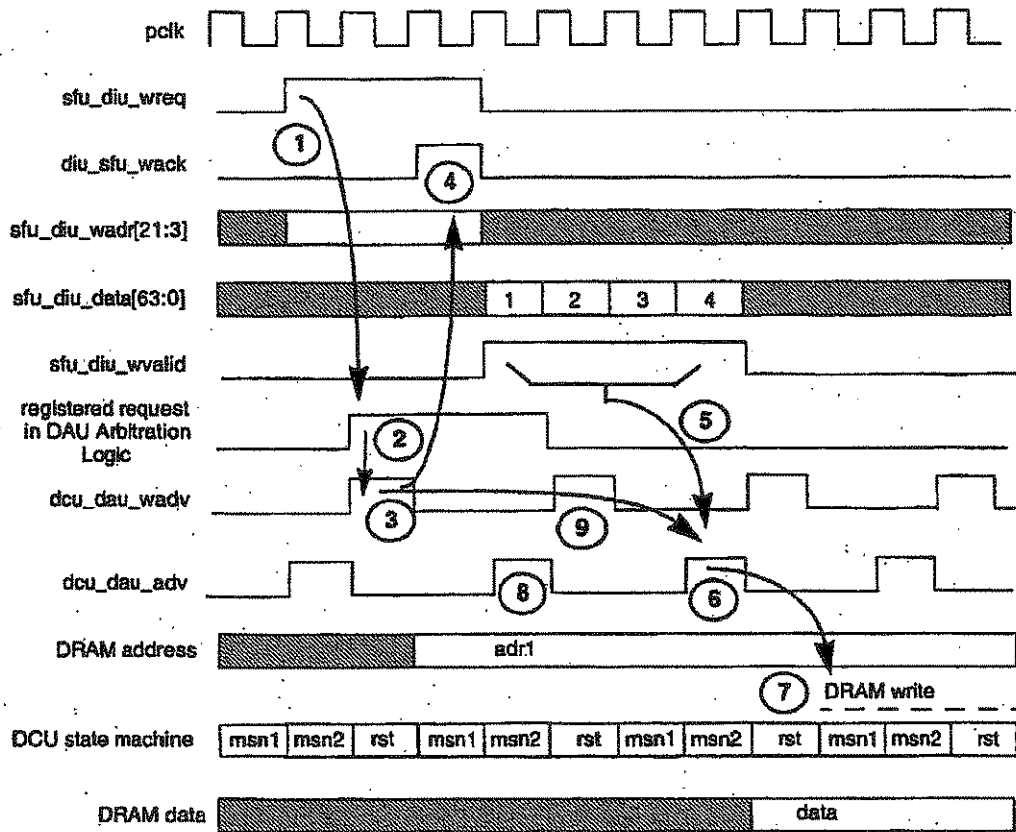


FIG. 126

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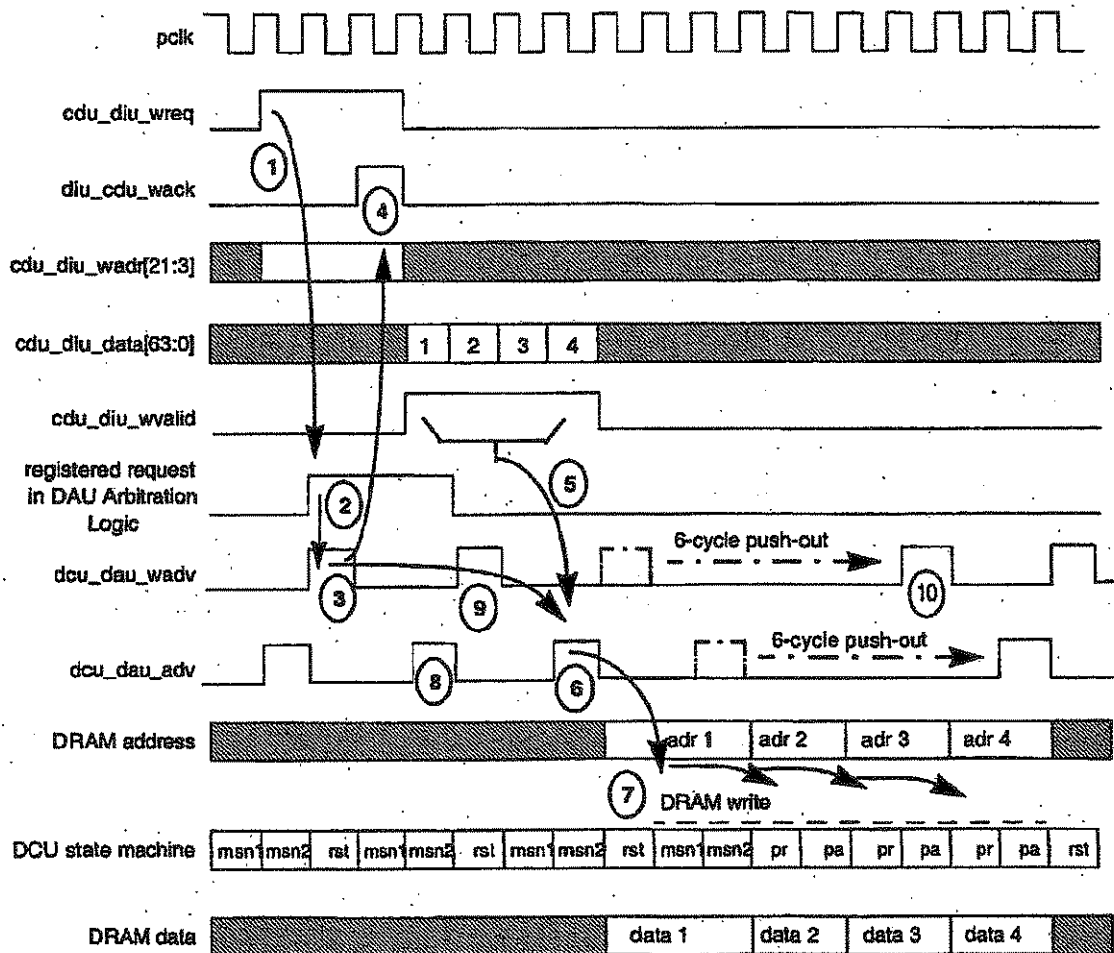


FIG. 127

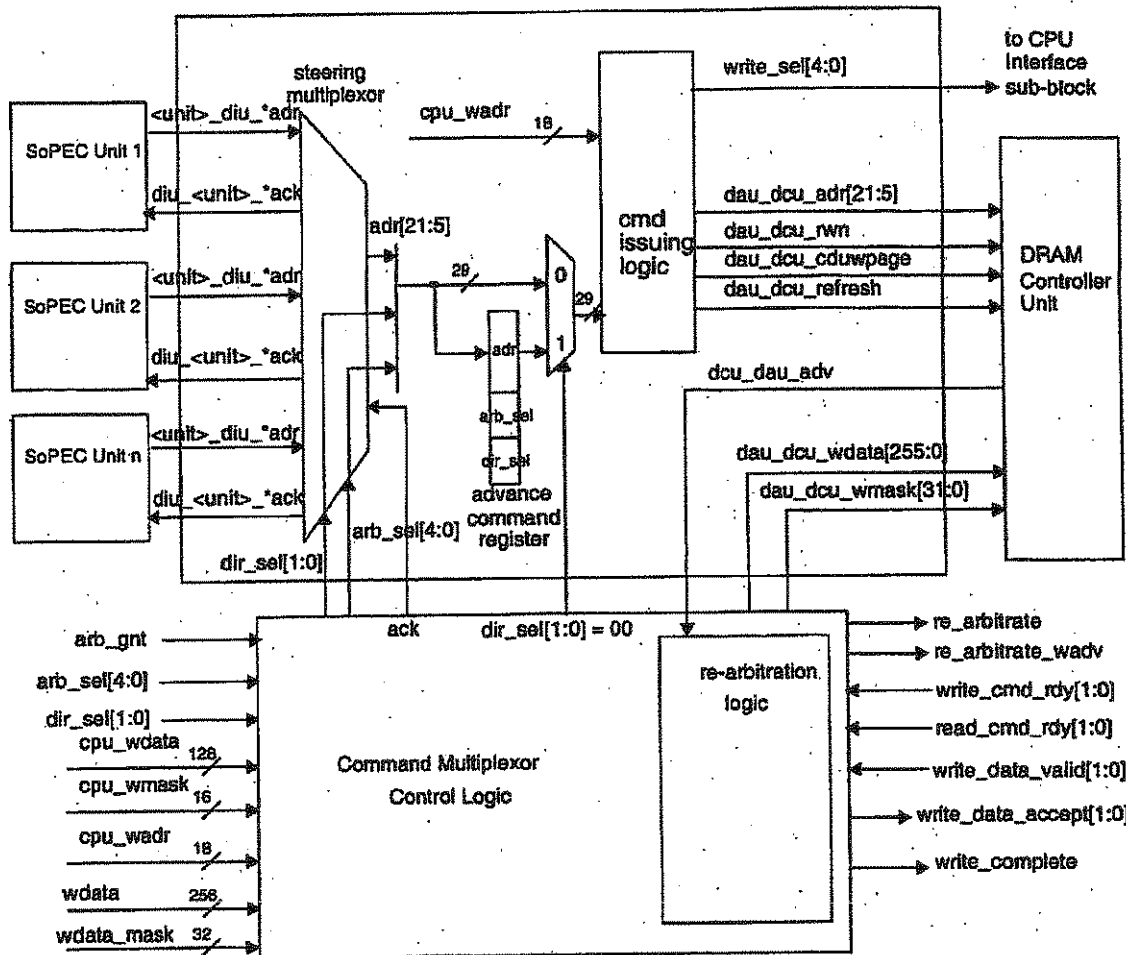


FIG. 128

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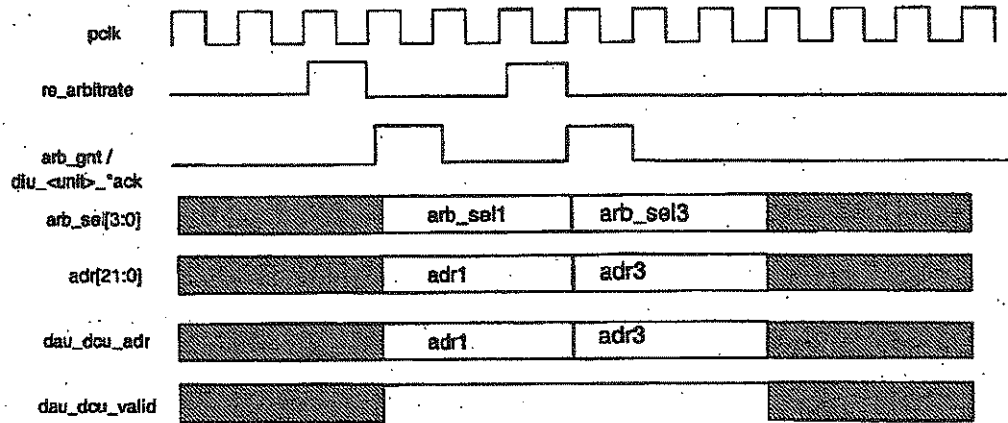


FIG. 129

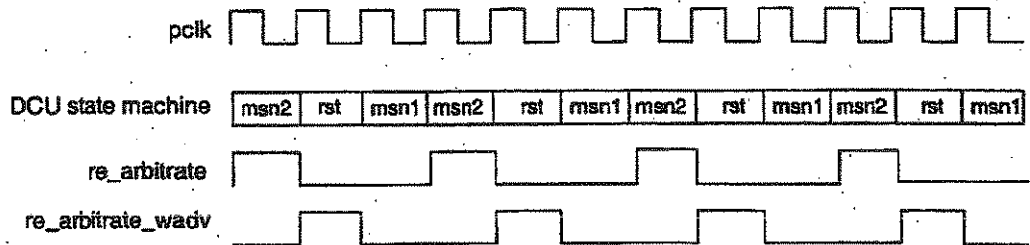


FIG. 130

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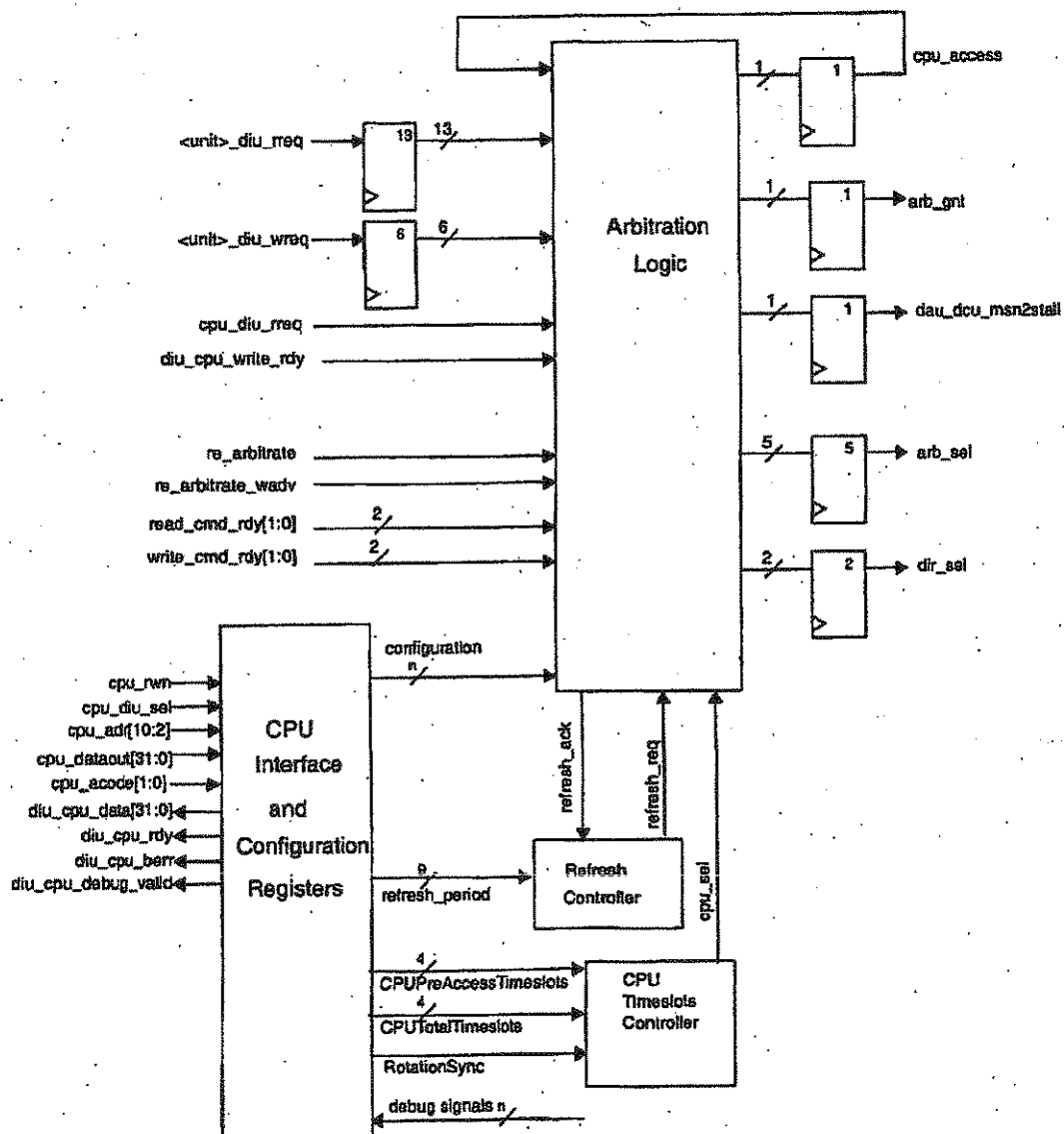


FIG. 131

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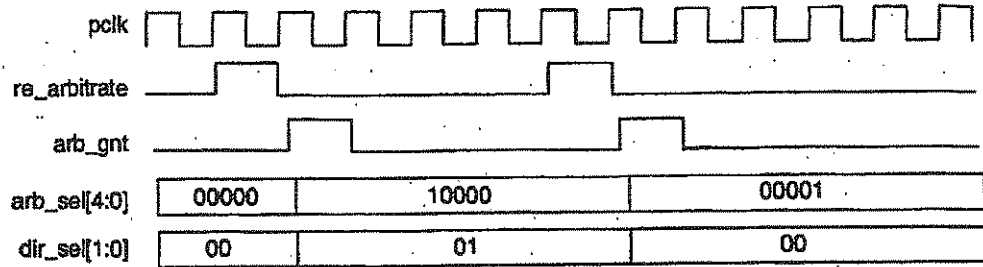


FIG. 132

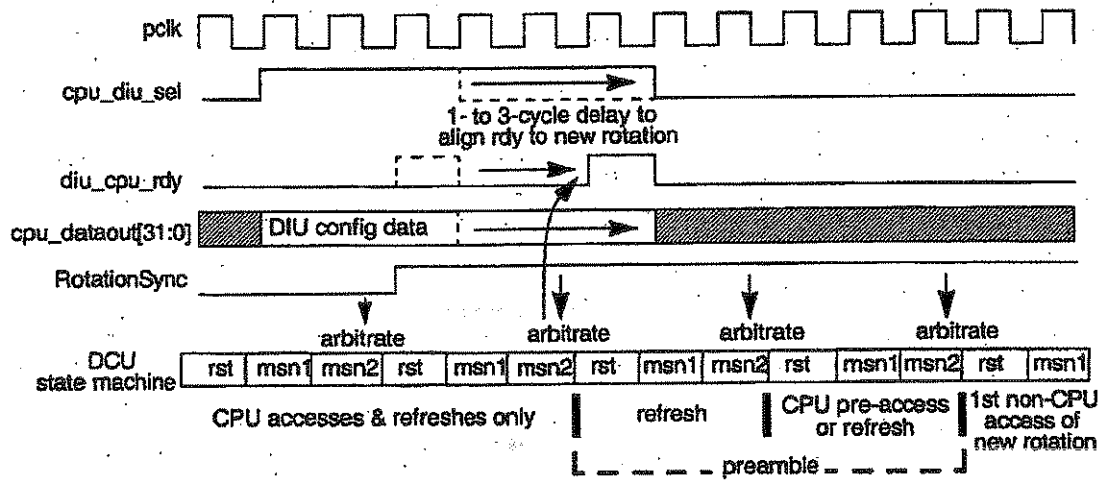


FIG. 133

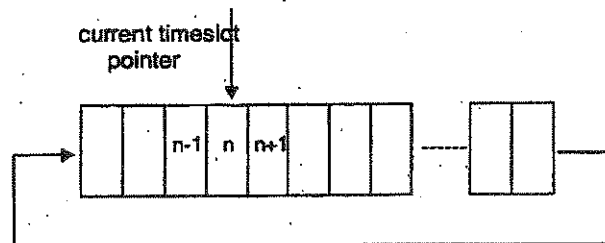


FIG. 134

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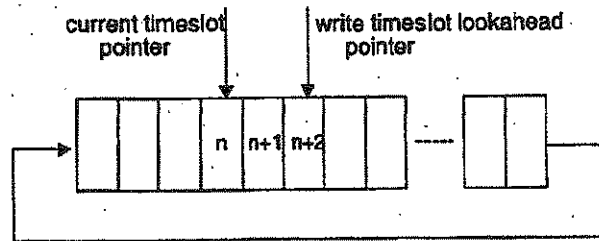


FIG. 135

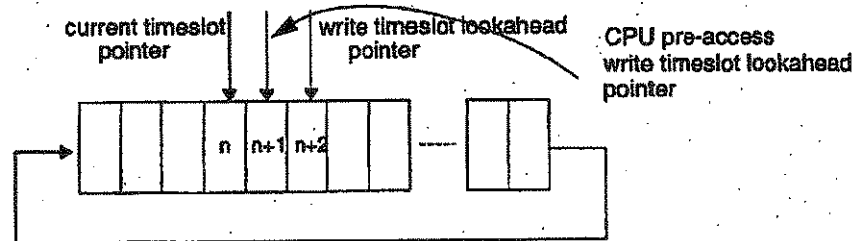


FIG. 136

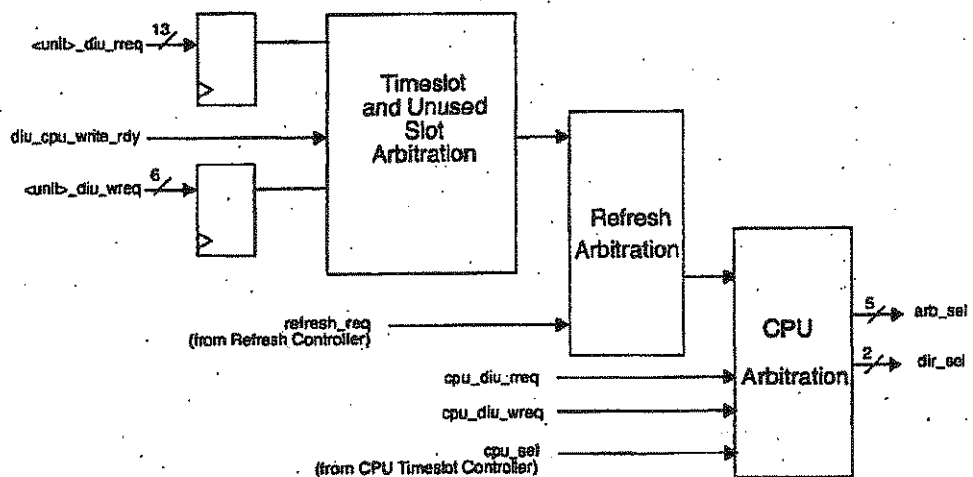


FIG. 137

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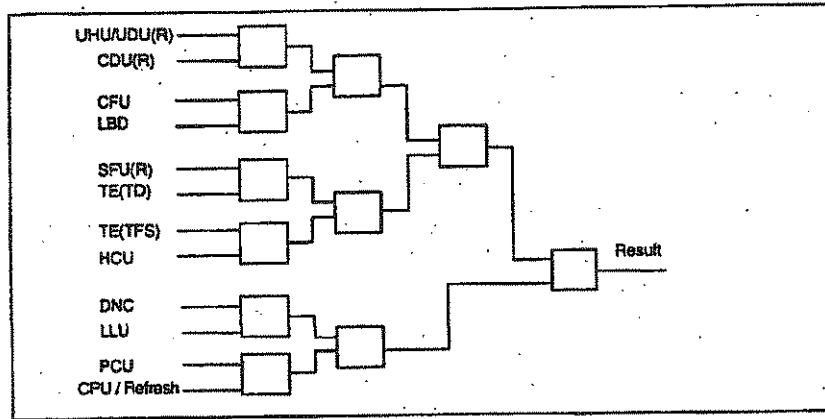


FIG. 138

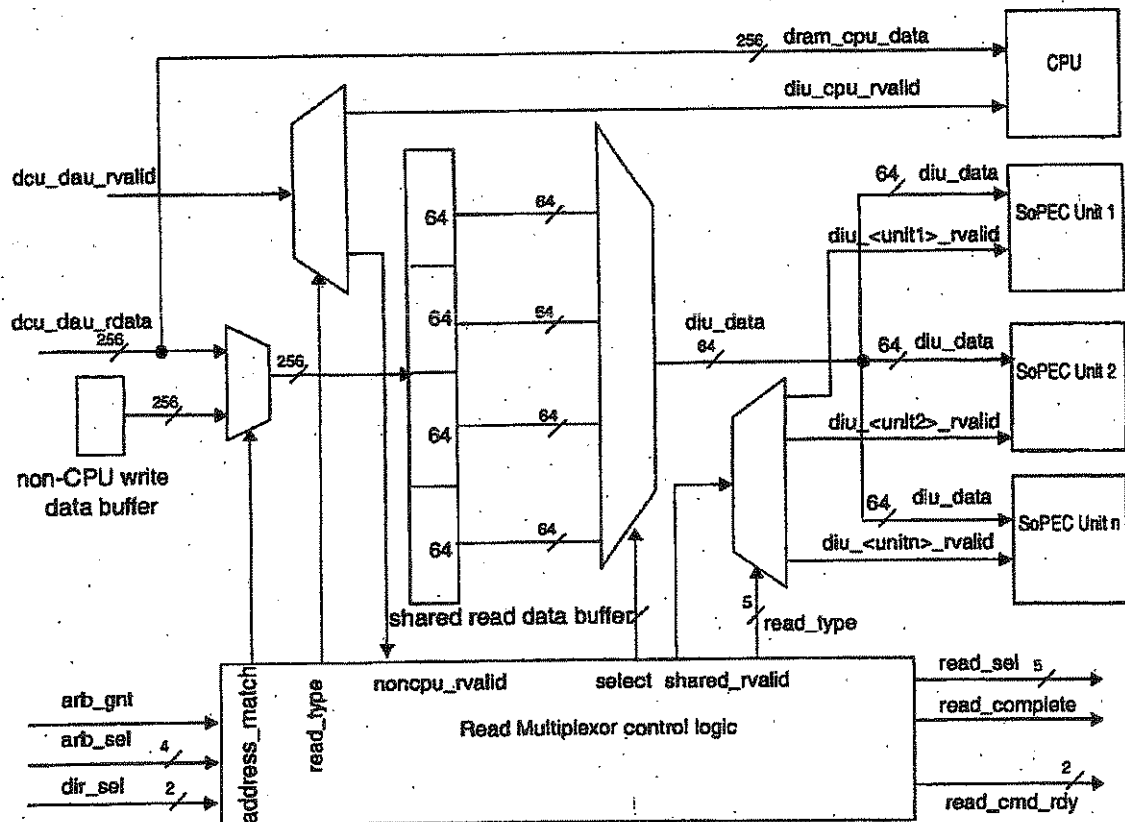


FIG. 139

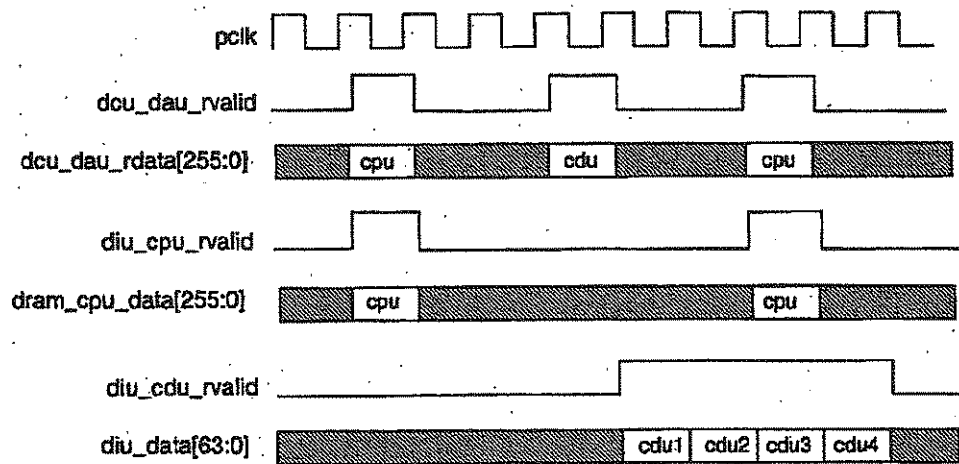


FIG. 140

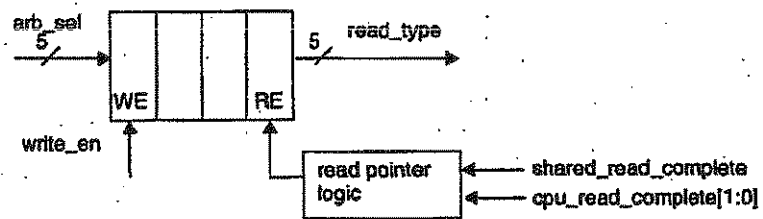


FIG. 141

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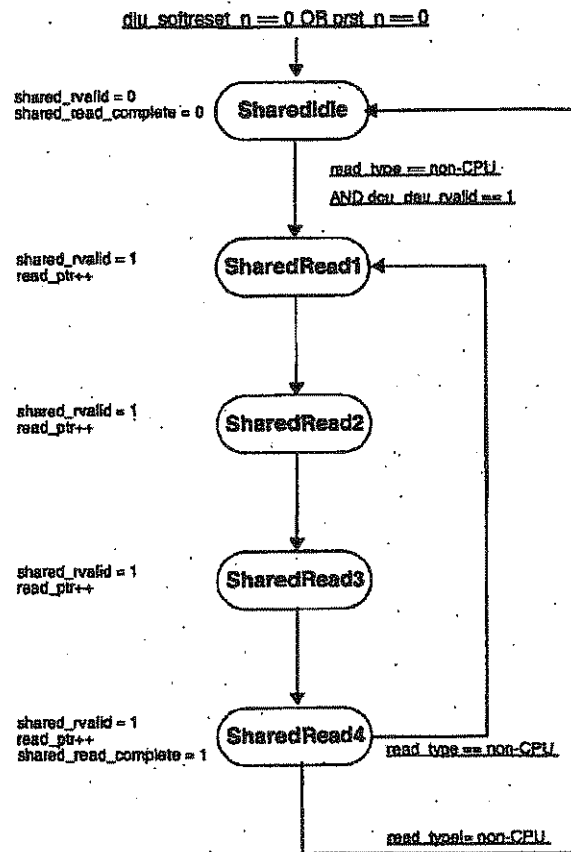


FIG. 142

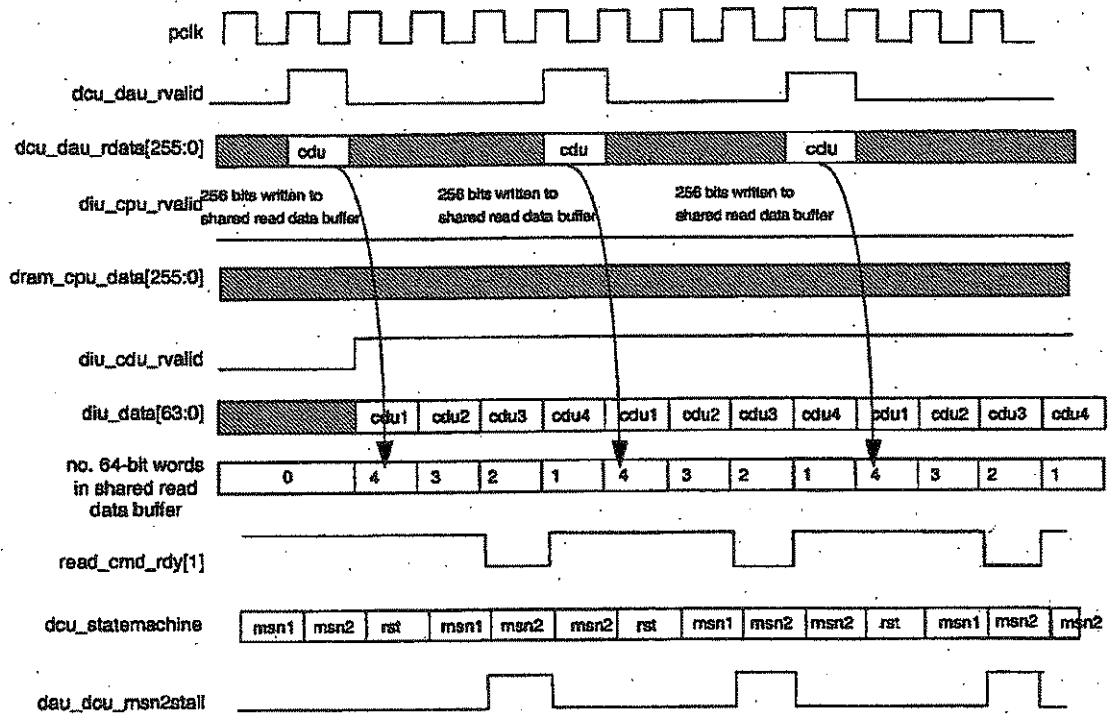


FIG. 143

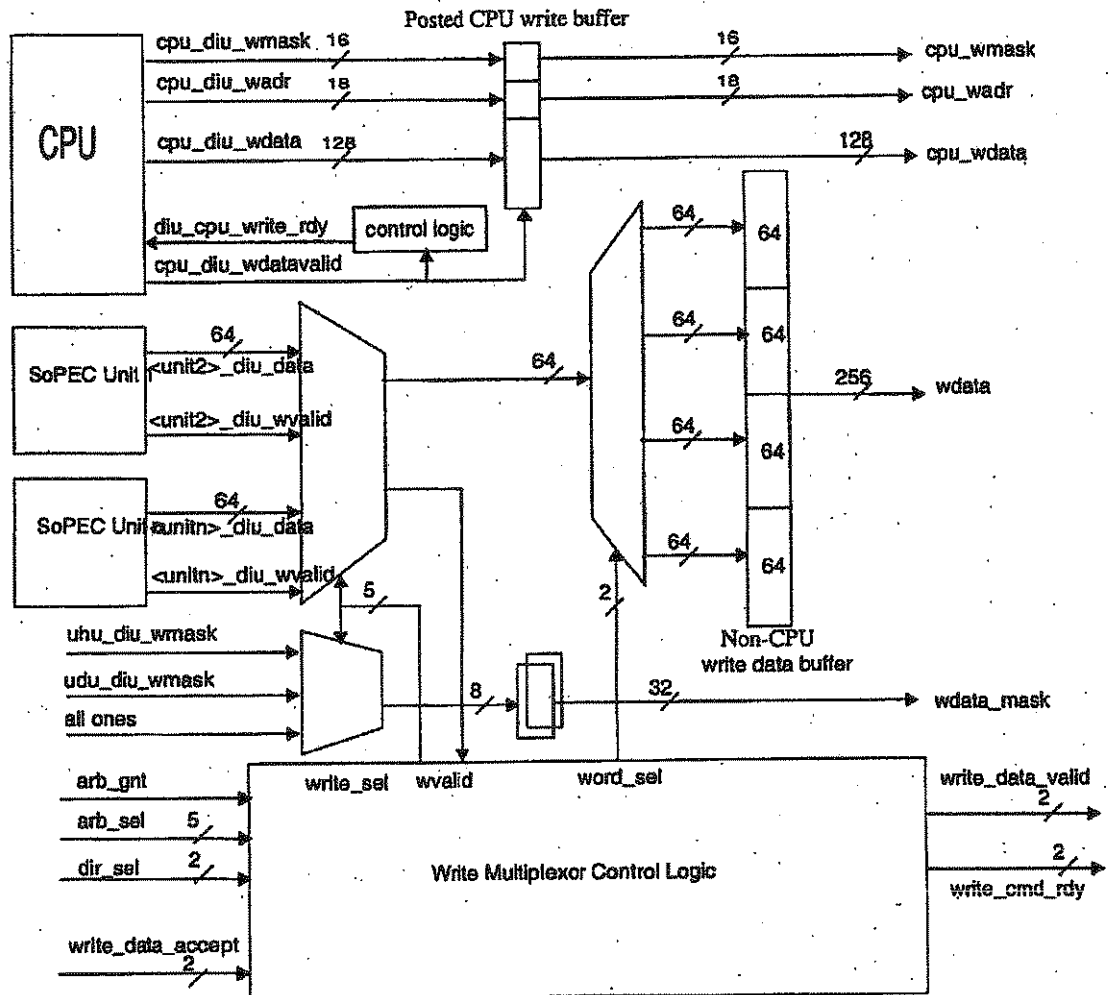


FIG. 144

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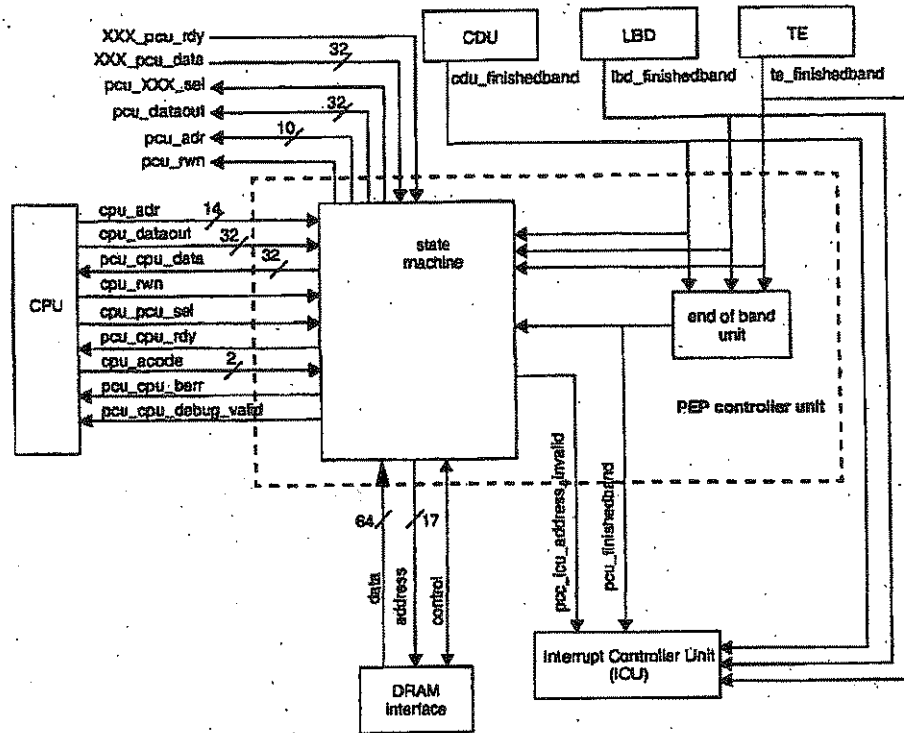


FIG. 145

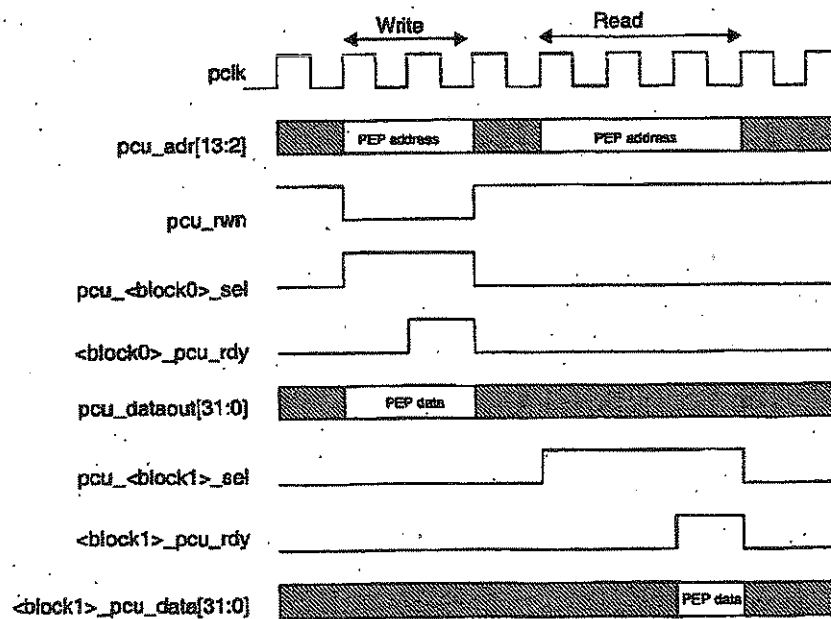


FIG. 146

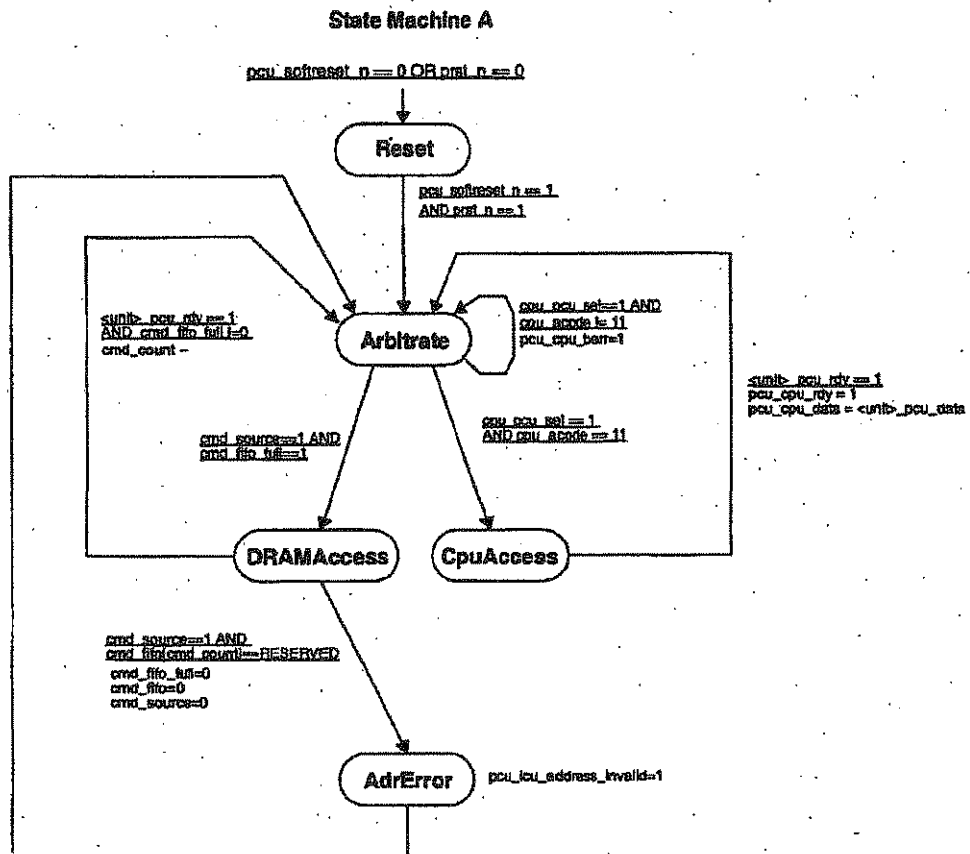


FIG. 147

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State Machine B

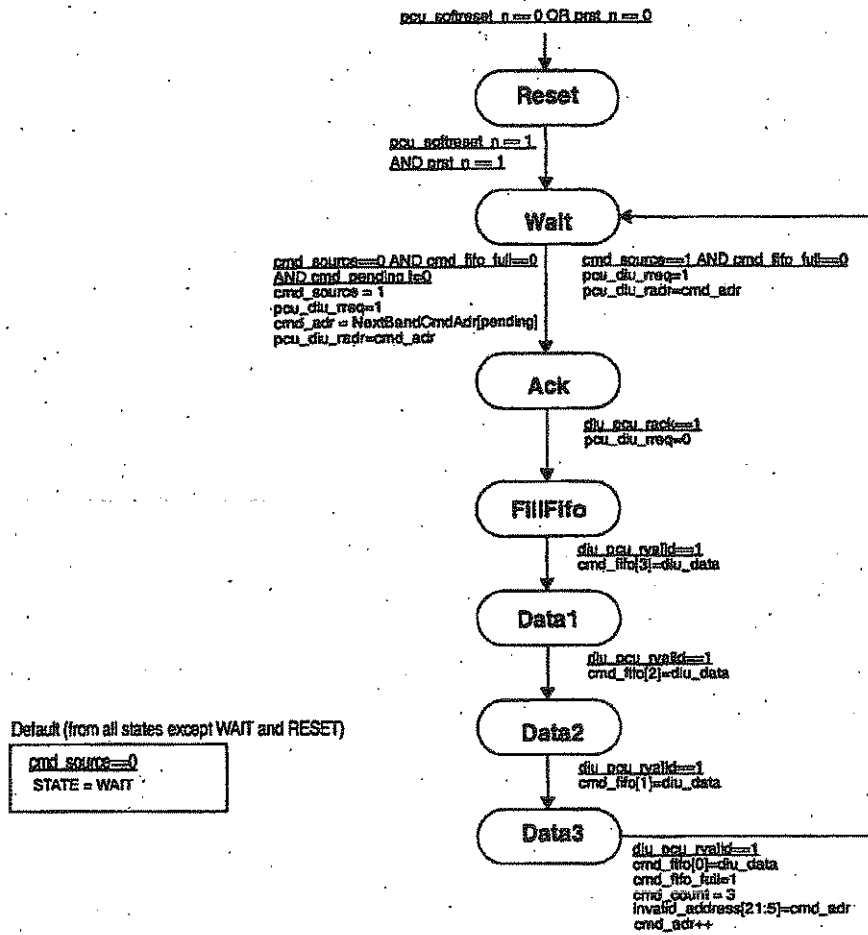


FIG. 148

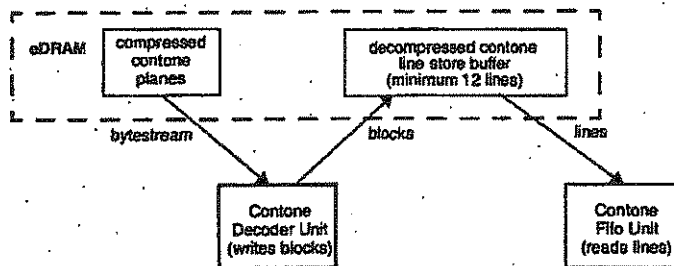


FIG. 149

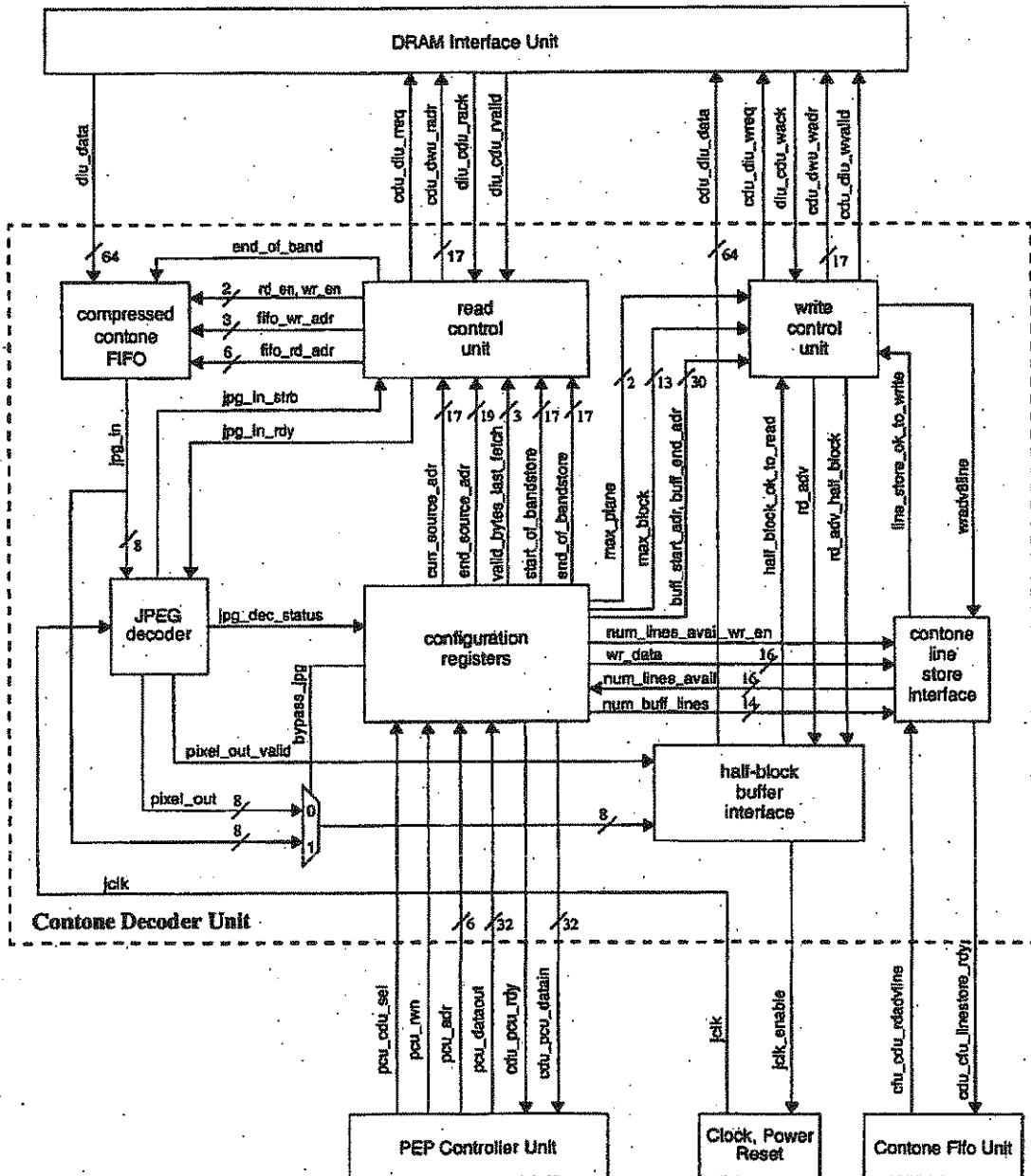


FIG. 150

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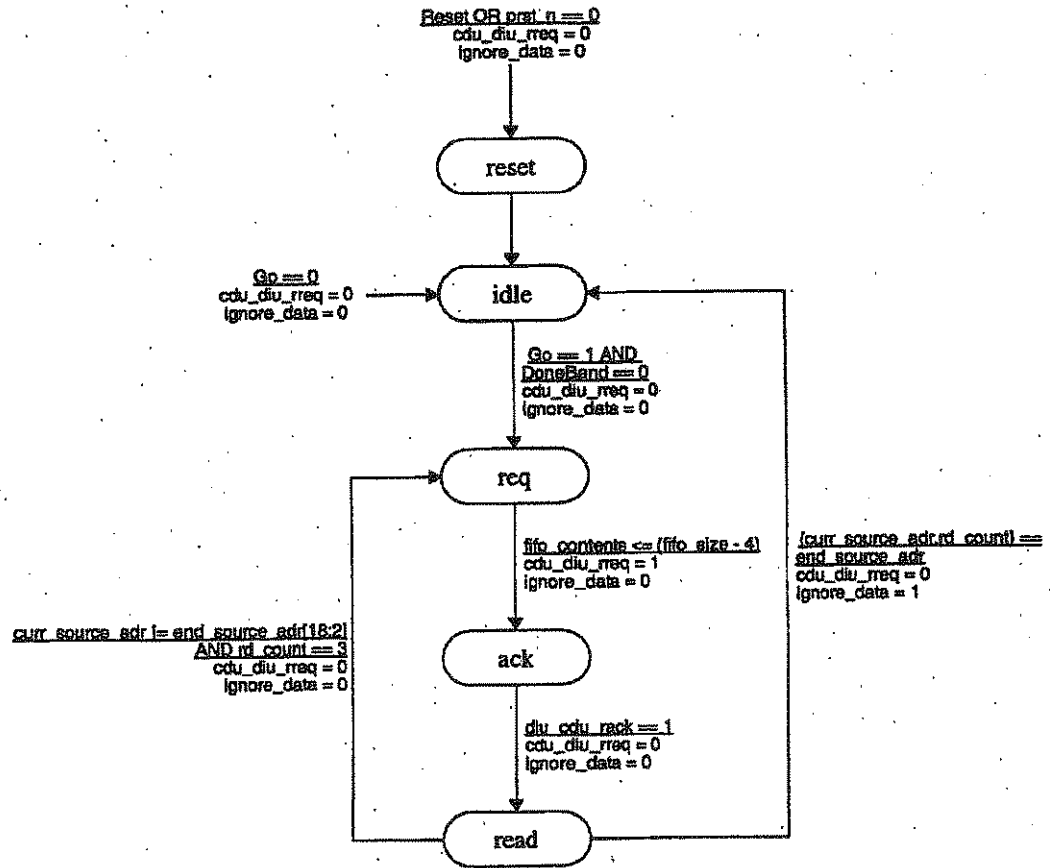


FIG. 151

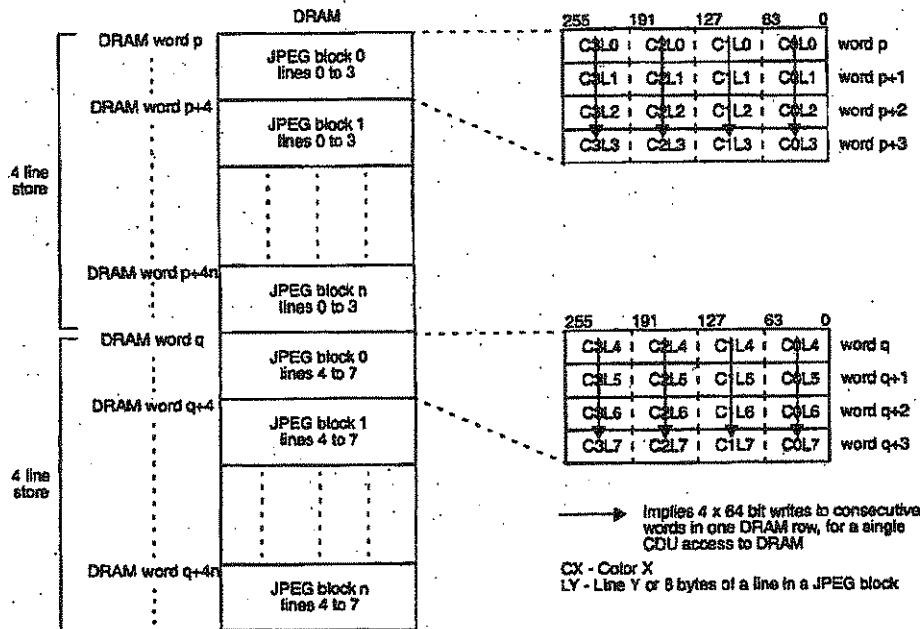


FIG. 152

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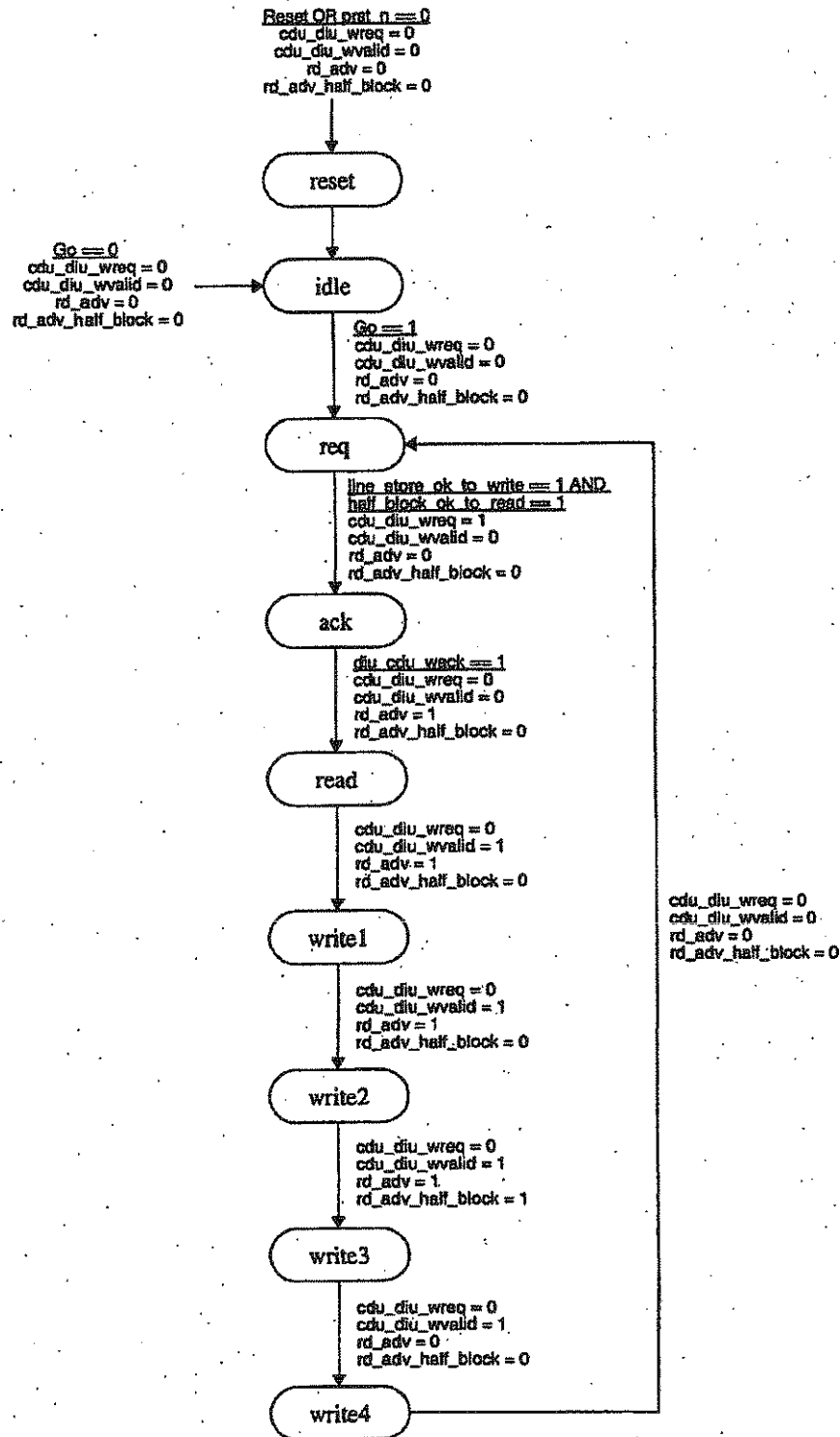


FIG. 153

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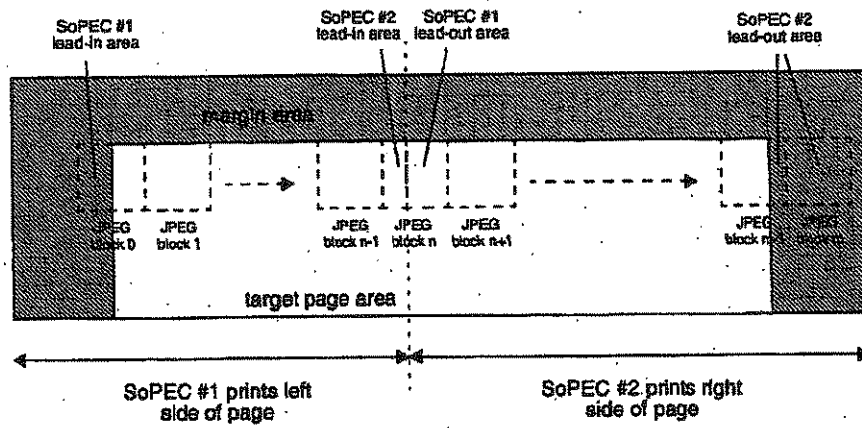


FIG. 154

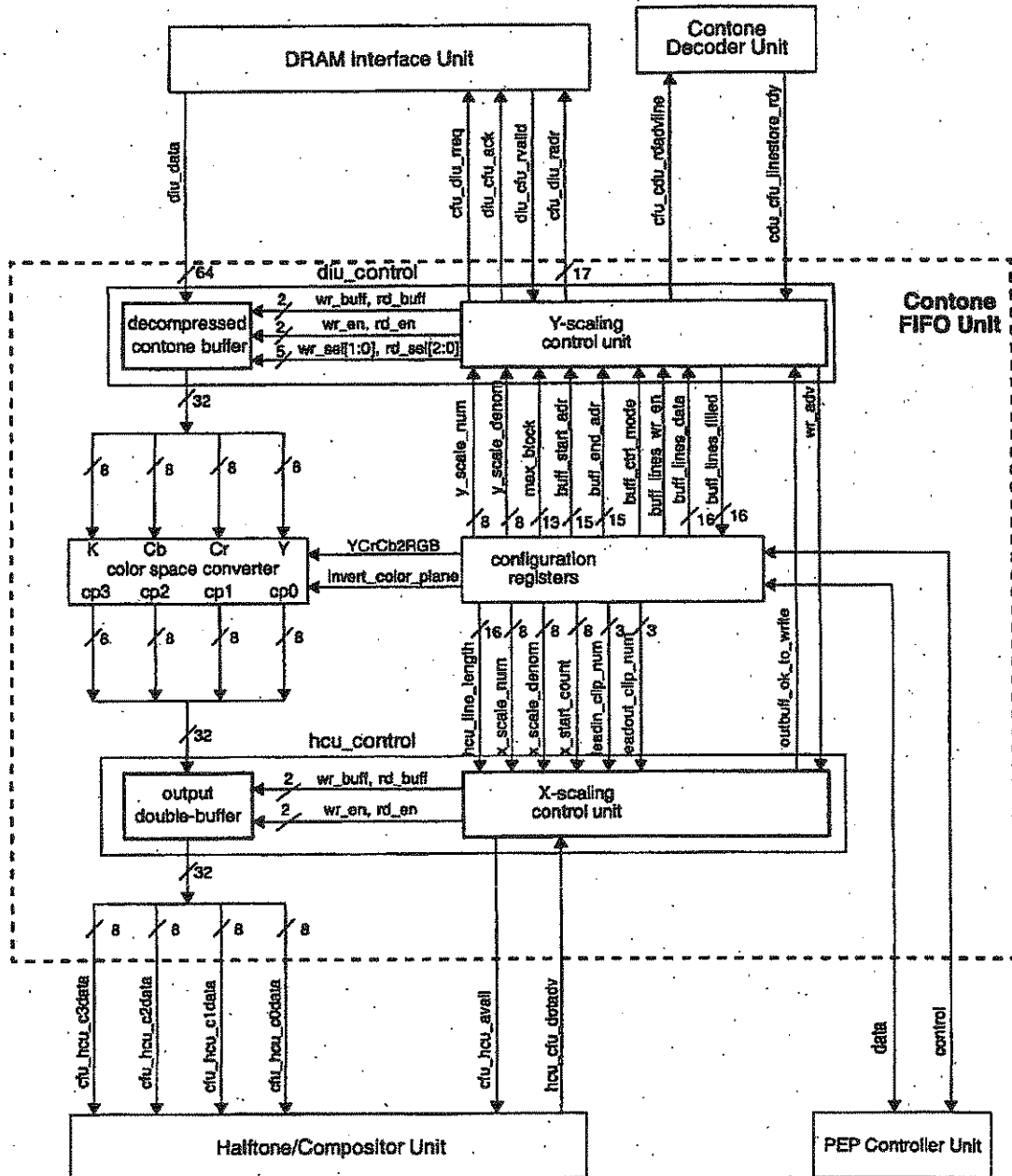


FIG. 155

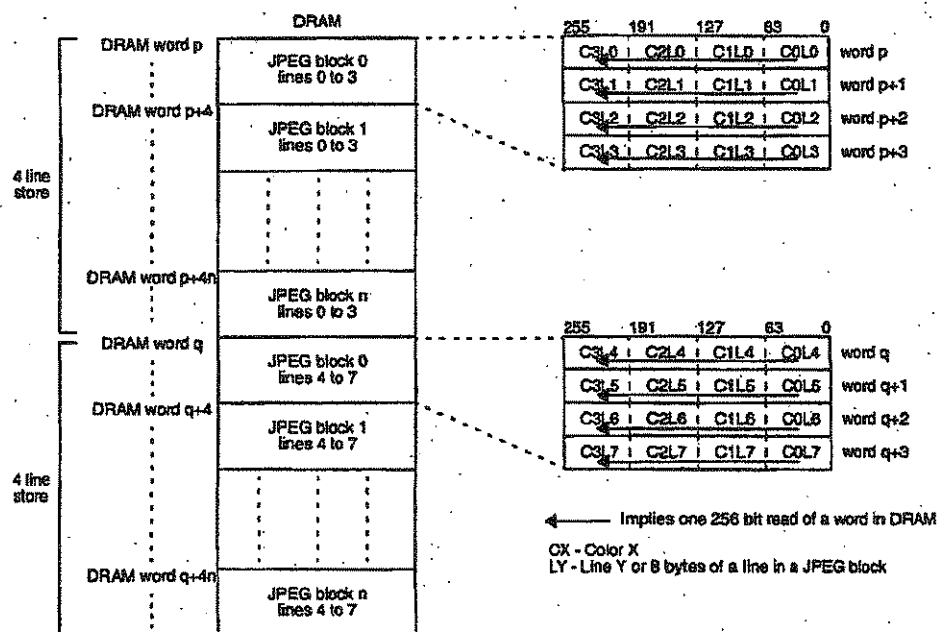


FIG. 156

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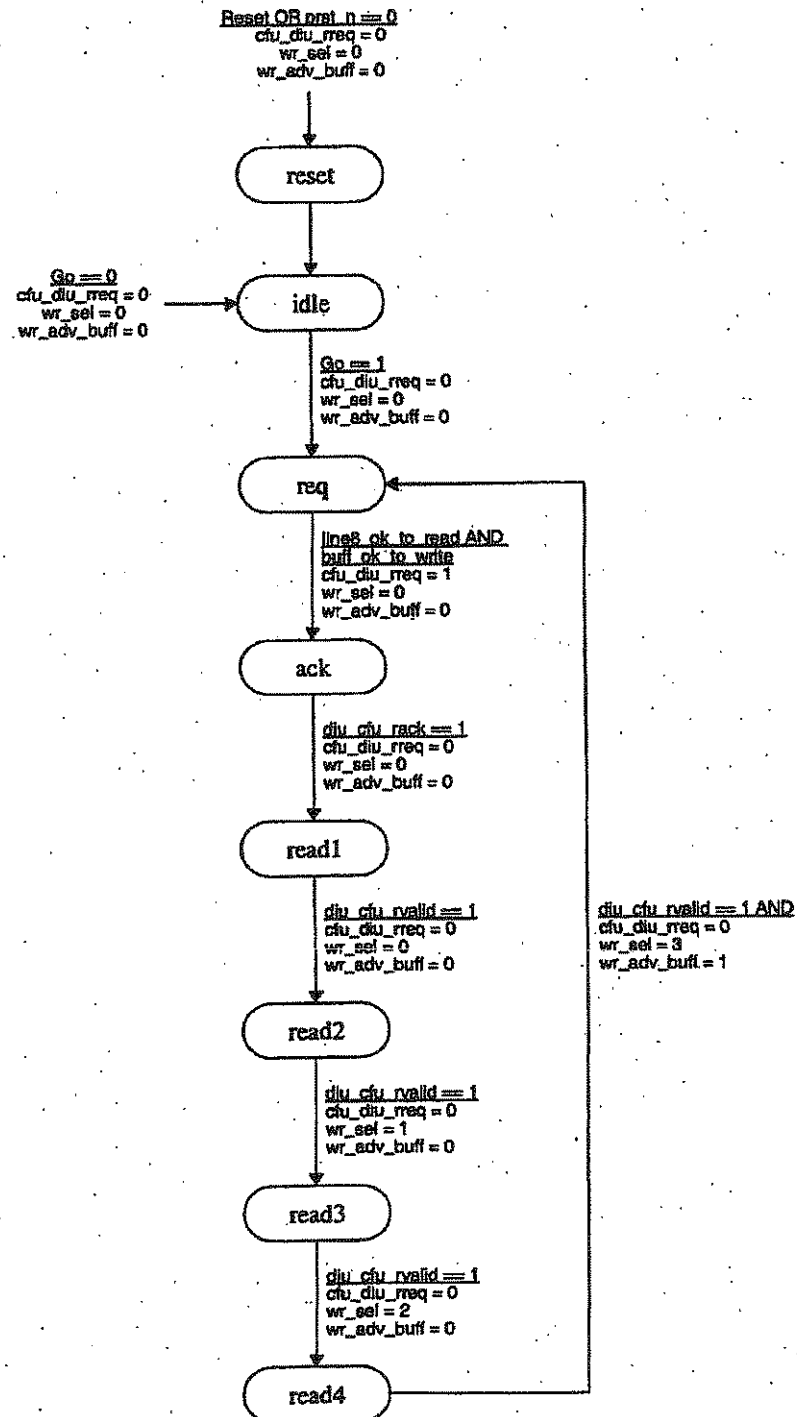


FIG. 157

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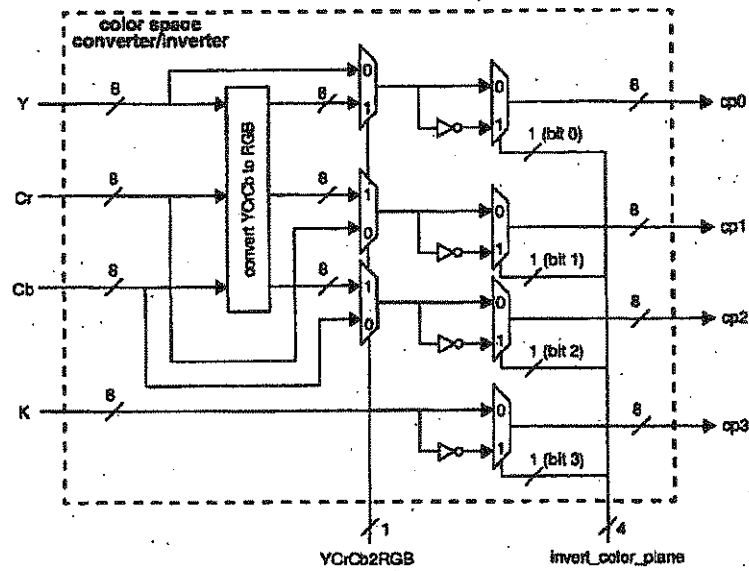


FIG. 158

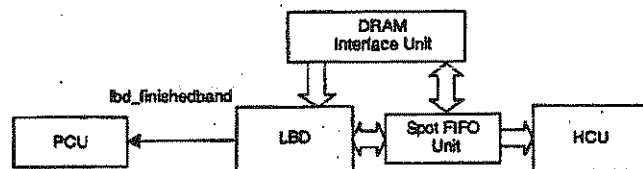


FIG. 159

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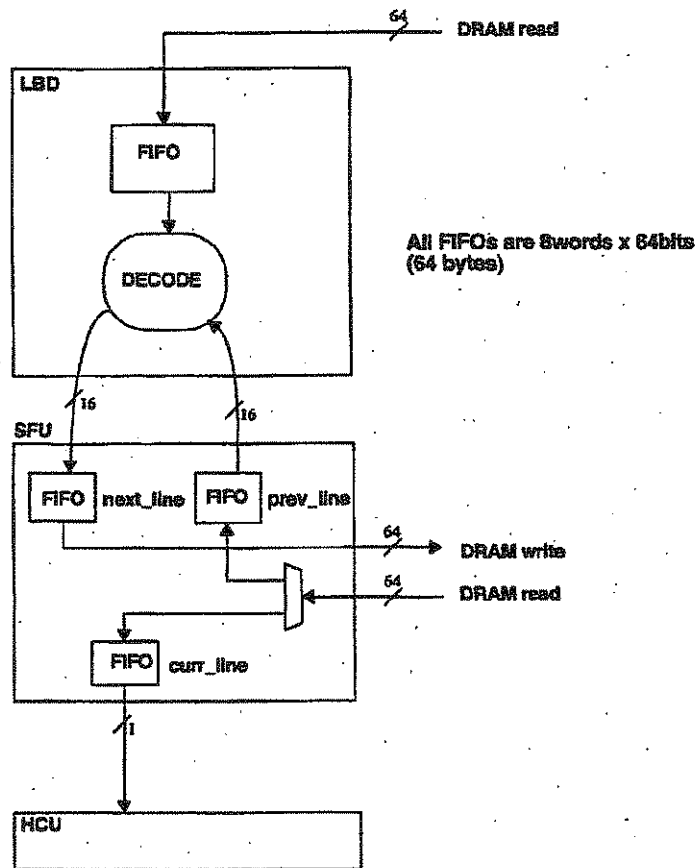


FIG. 160

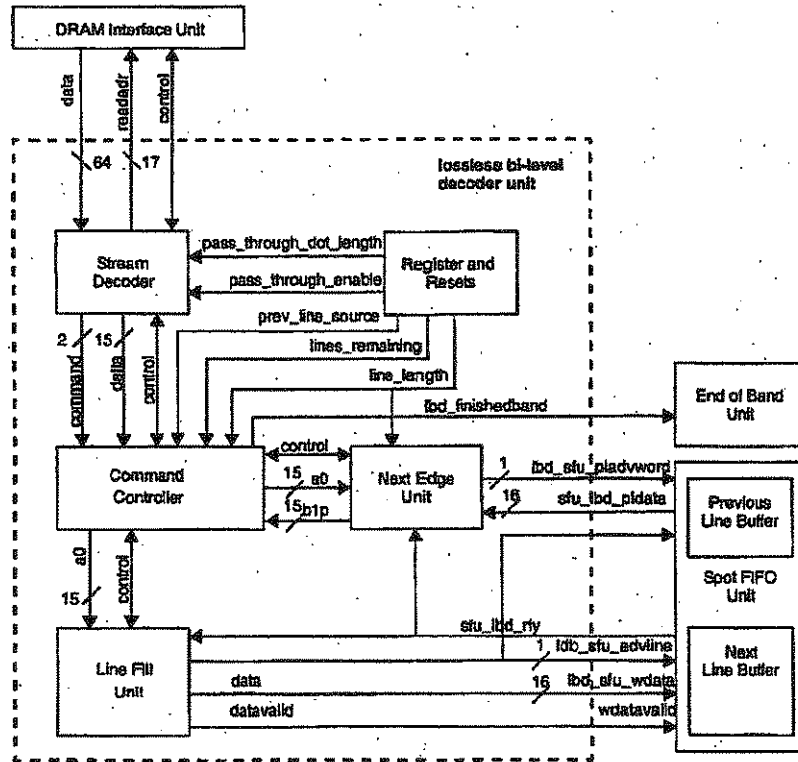


FIG. 161

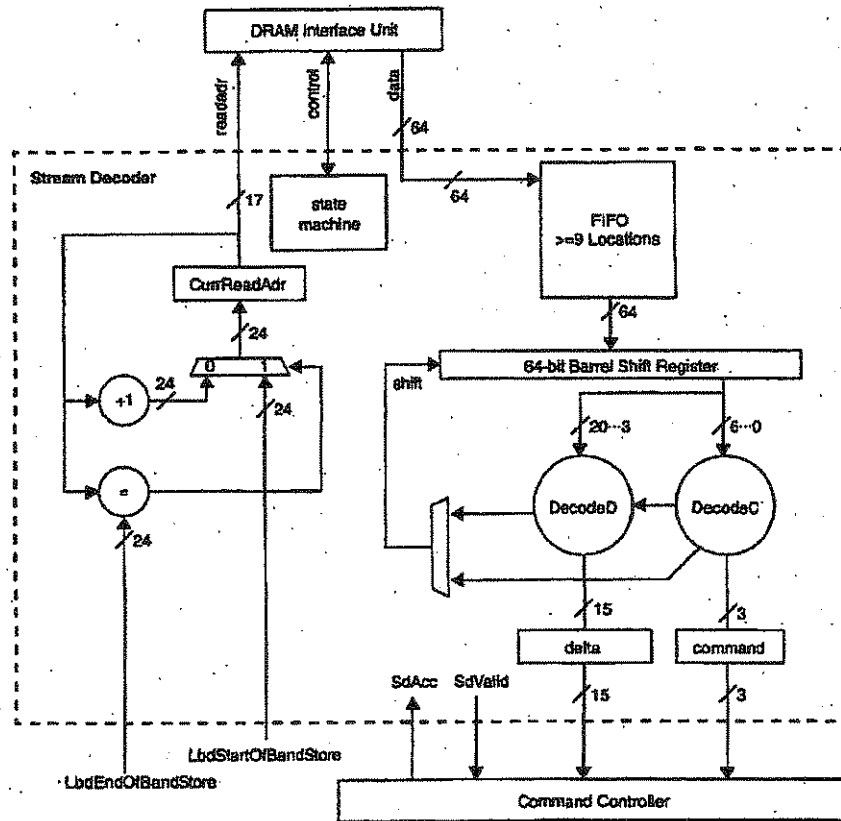


FIG. 162

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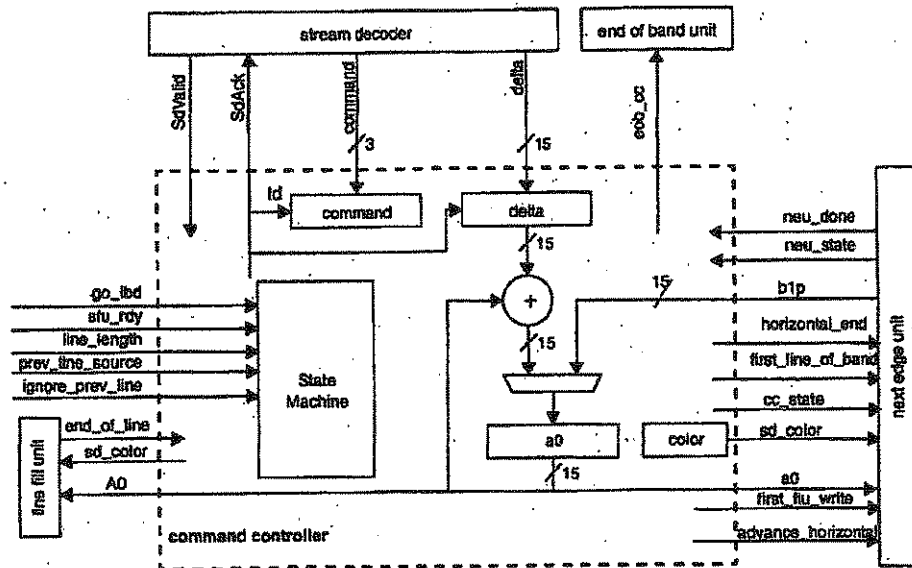


FIG. 163

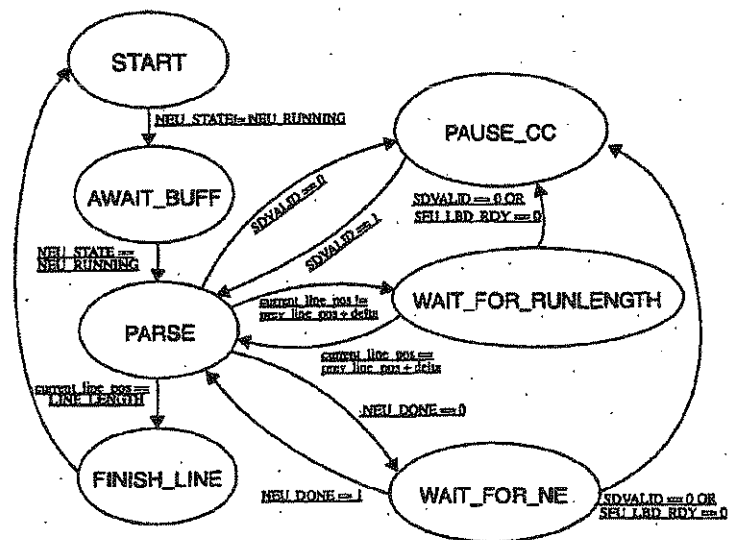


FIG. 164

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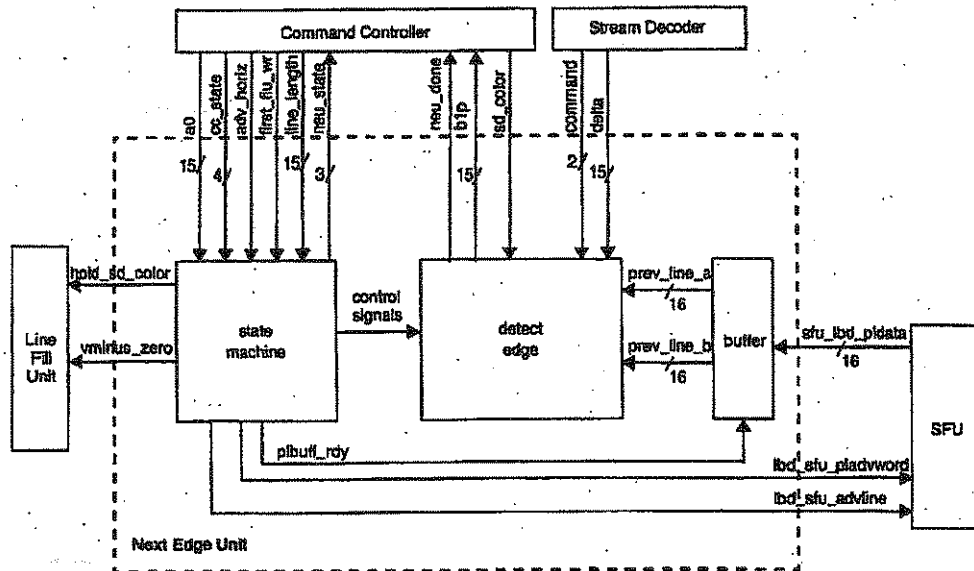


FIG. 165

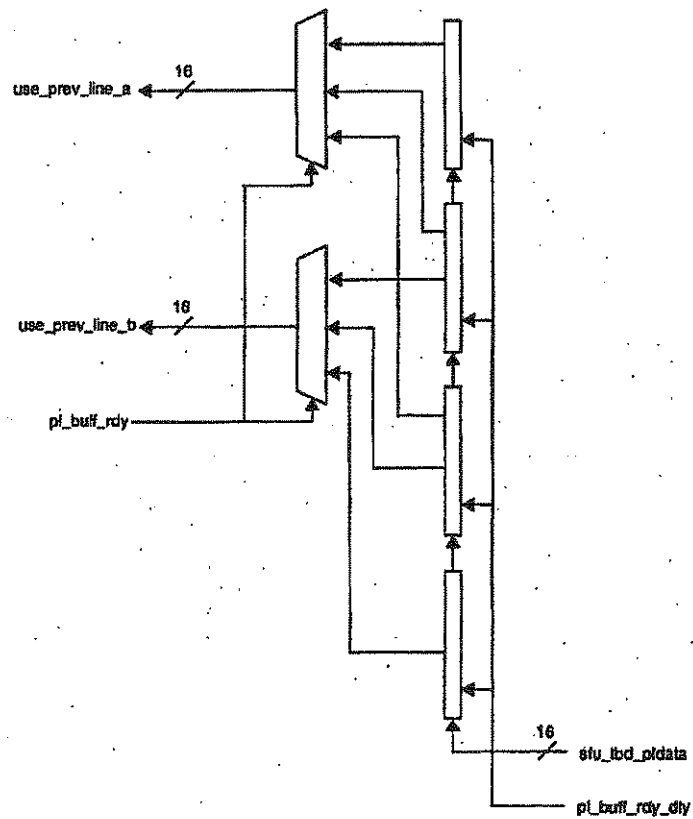


FIG. 166

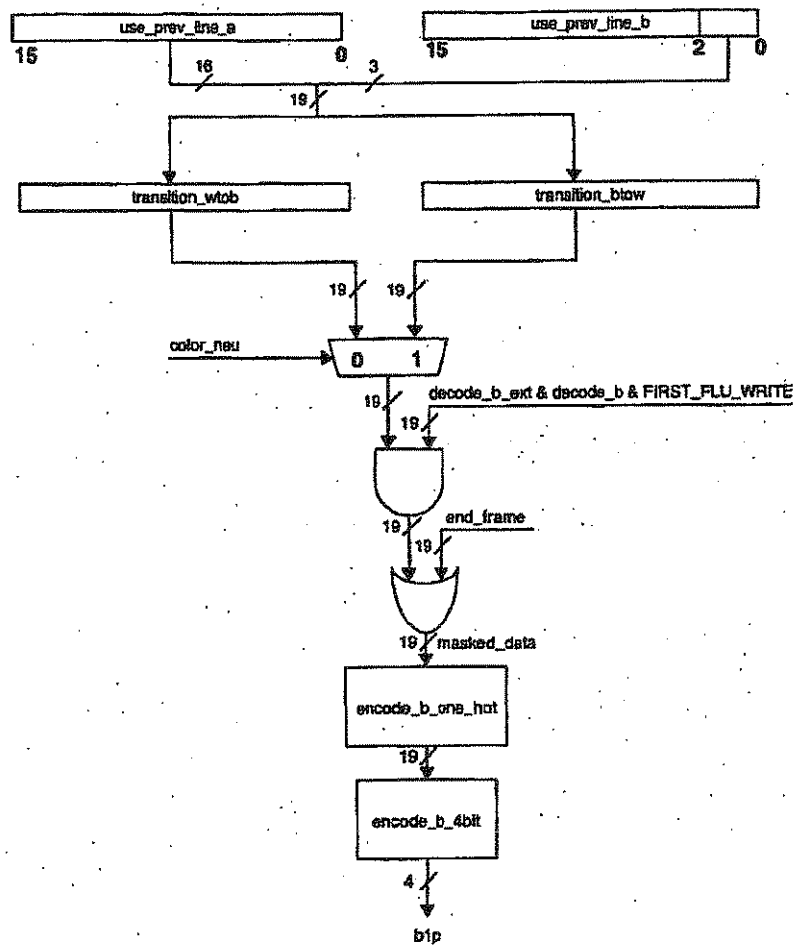


FIG. 167

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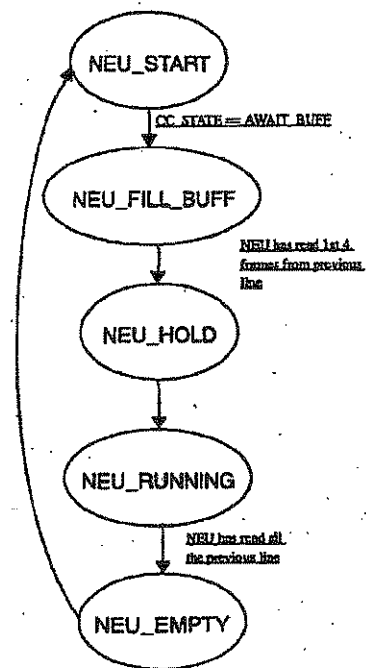


FIG. 168

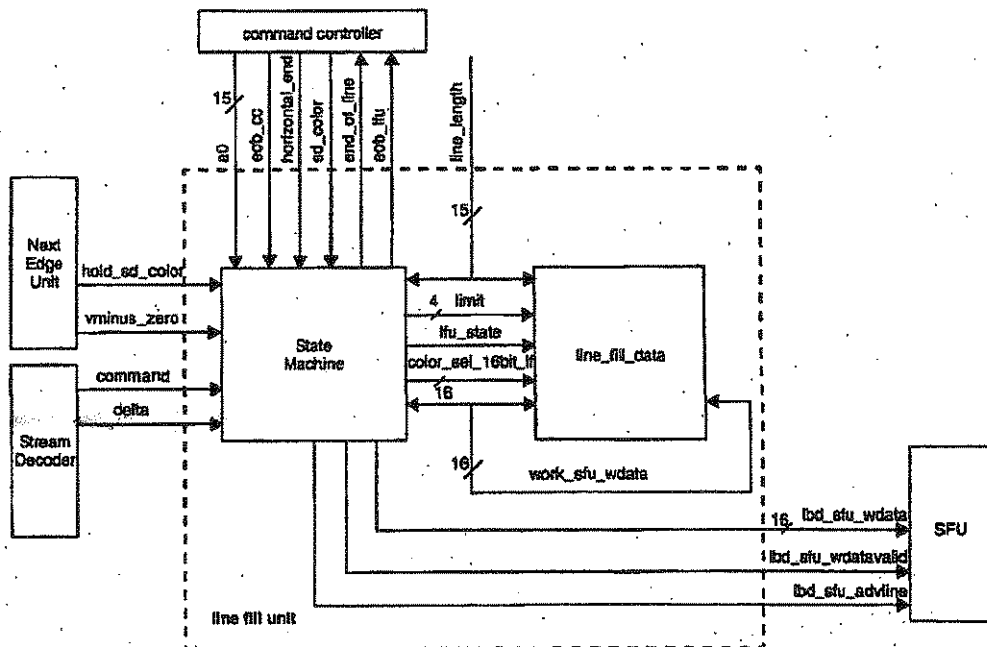


FIG. 169

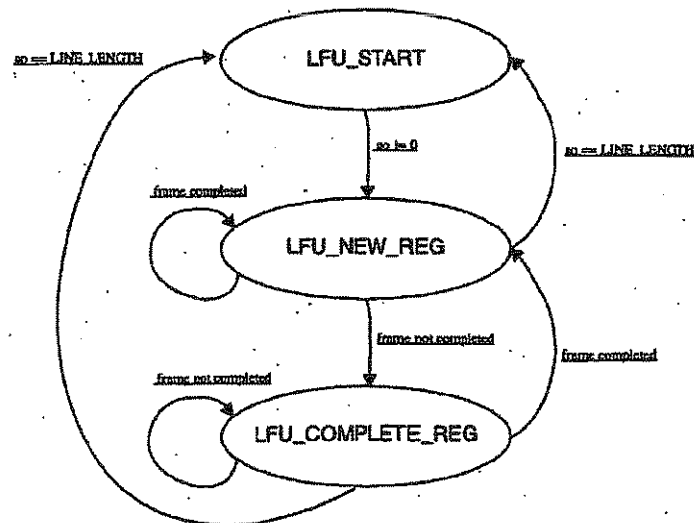
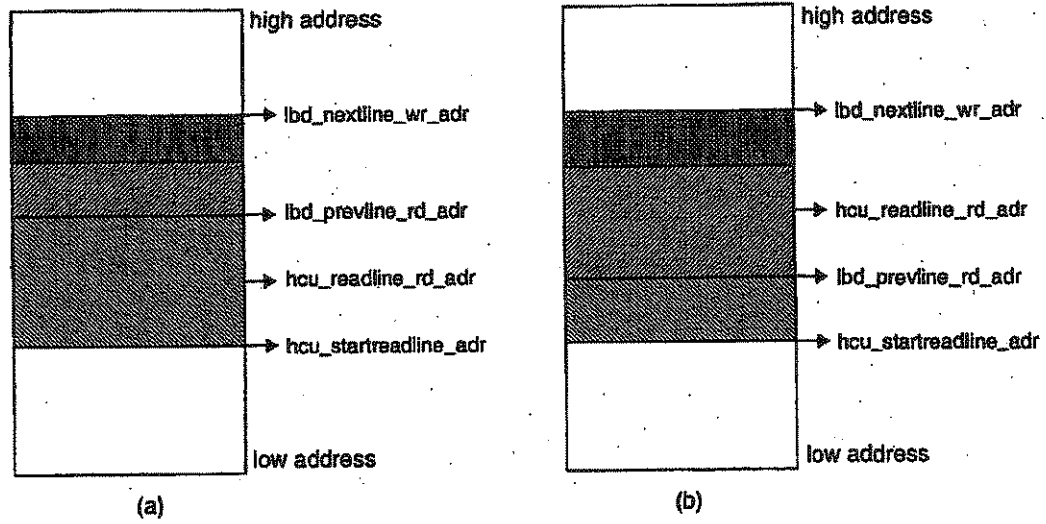


FIG. 170

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Key:

- Free buffer space
- Filled buffer space accessed by LBD Interface FIFOs
- Filled Buffer space read by HCU Read Line FIFO
- Filled Buffer space read by both HCU Read Line FIFO and LBD Interface FIFOs

FIG. 171

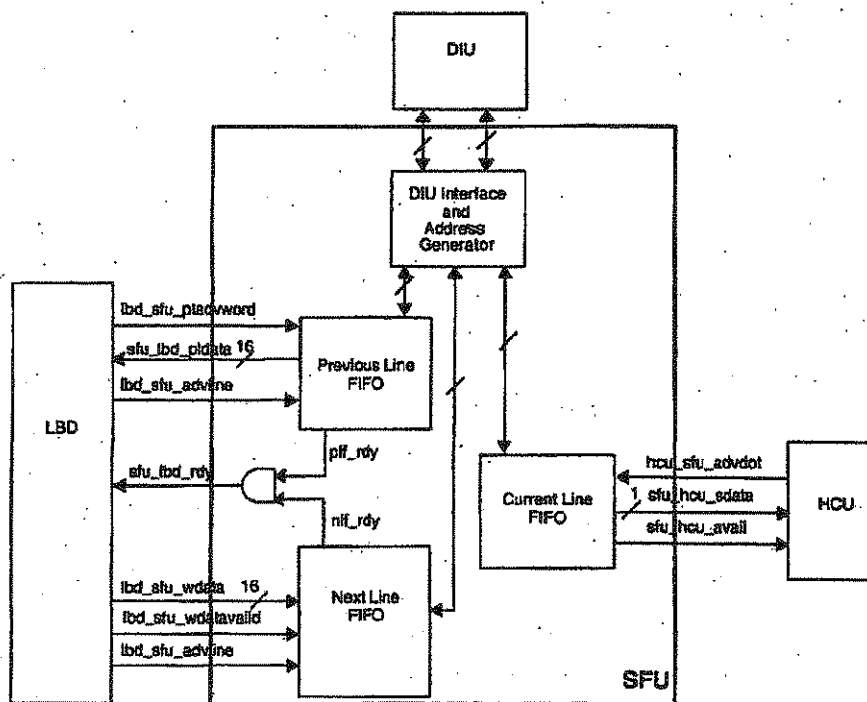


FIG. 172

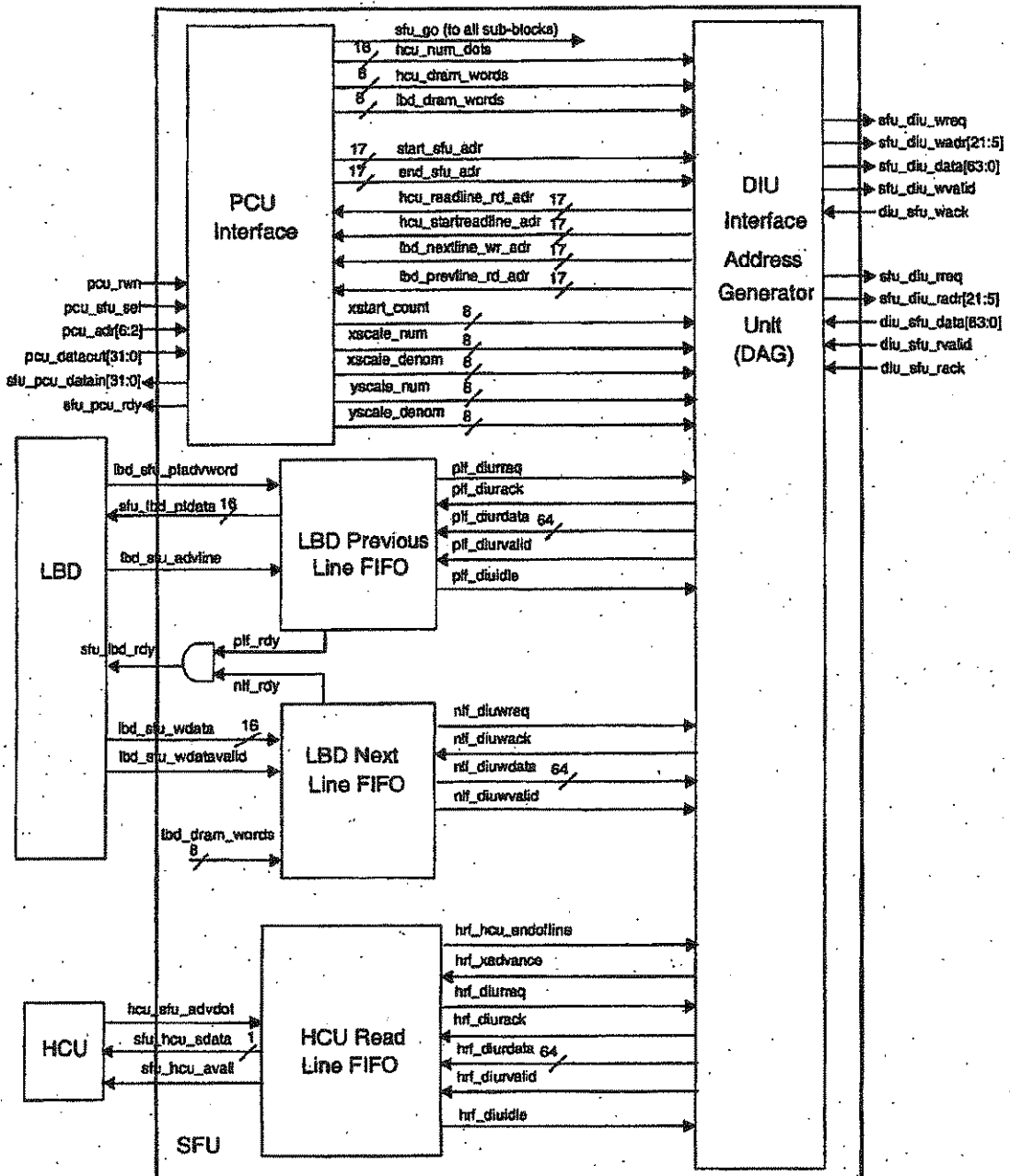


FIG. 173

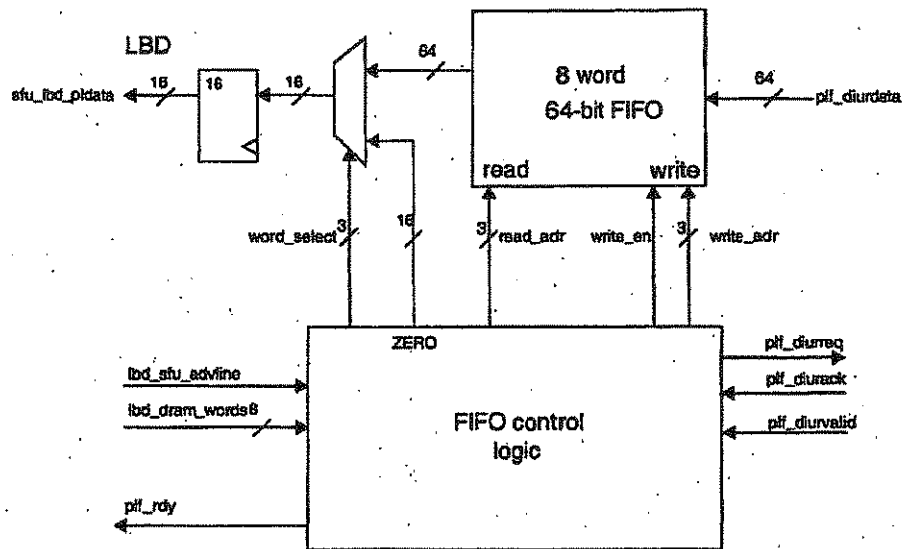


FIG. 174

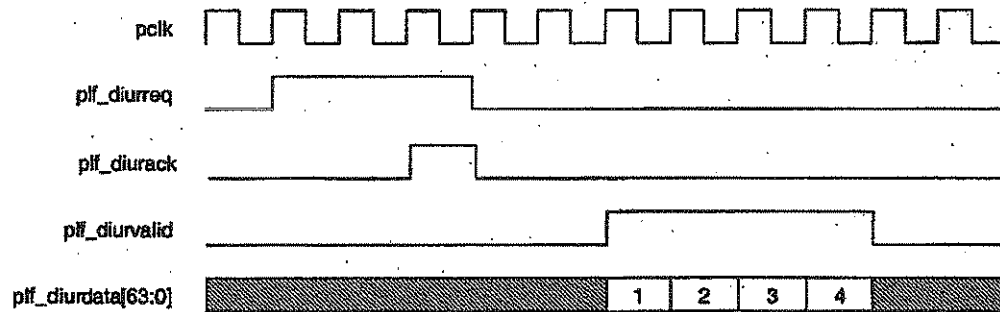


FIG. 175

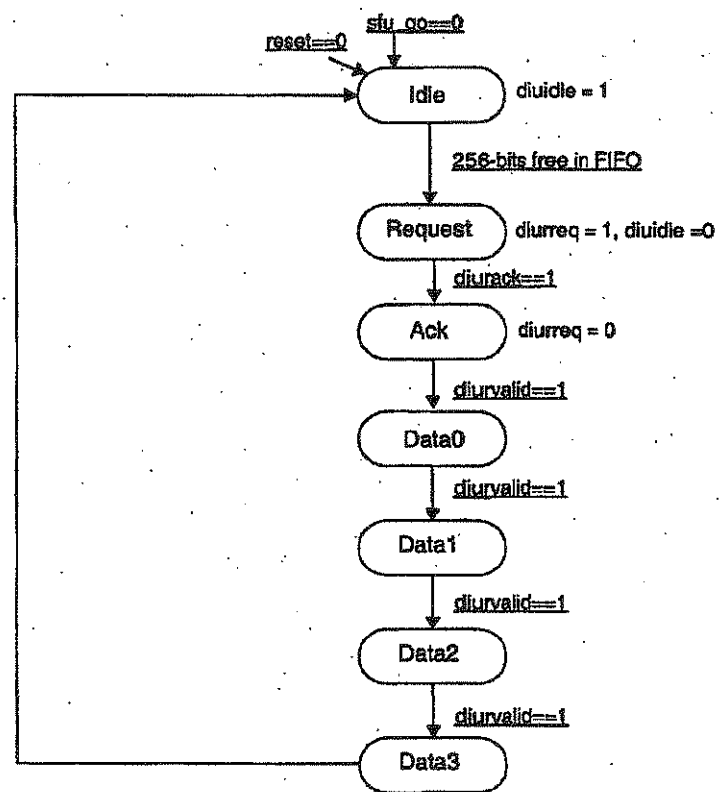


FIG. 176

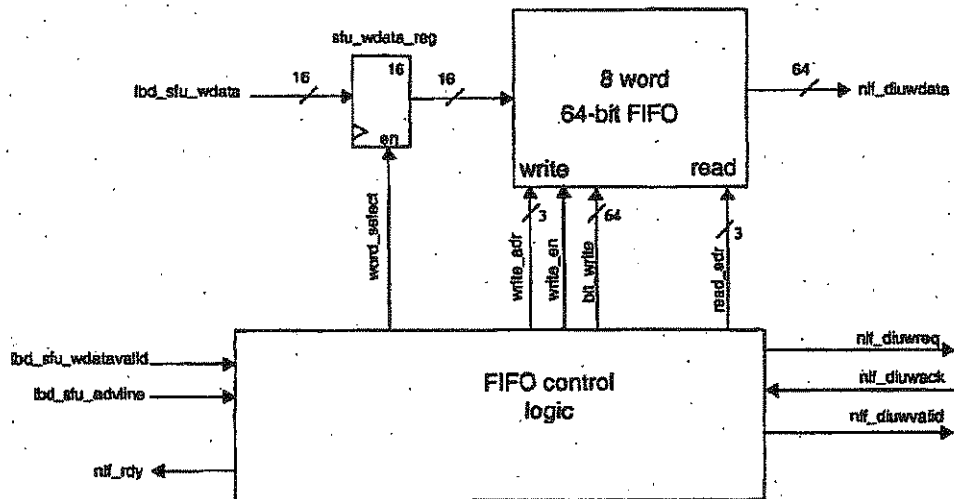


FIG. 177

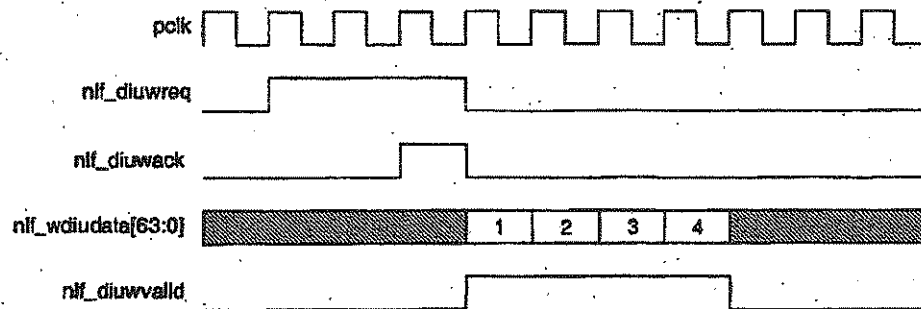


FIG. 178

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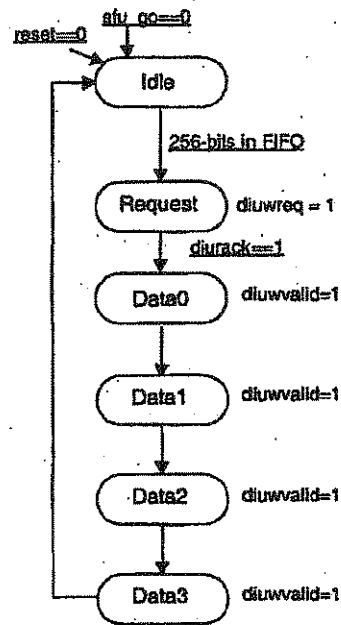


FIG. 179

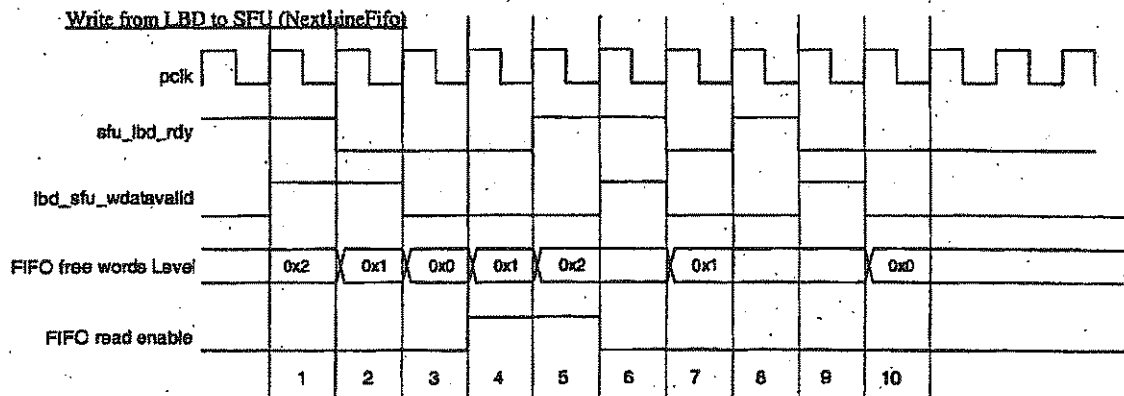


FIG. 180

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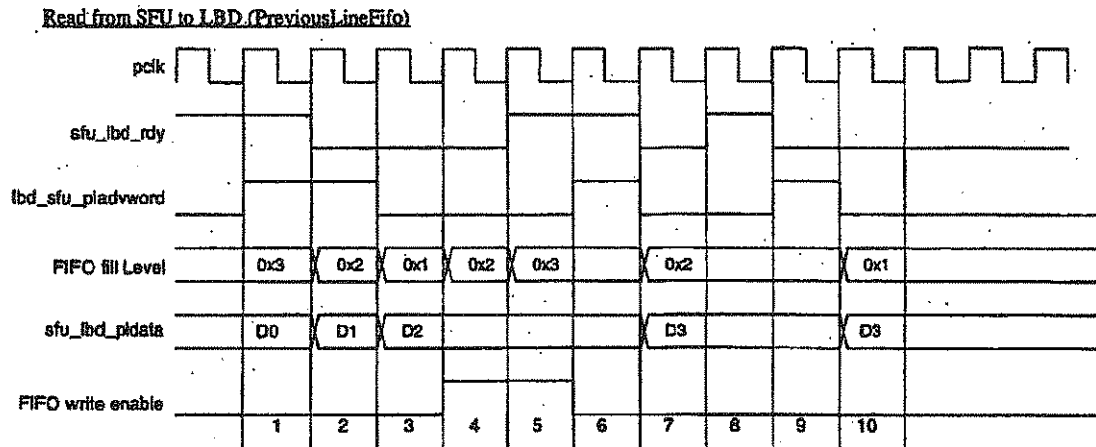


FIG. 181

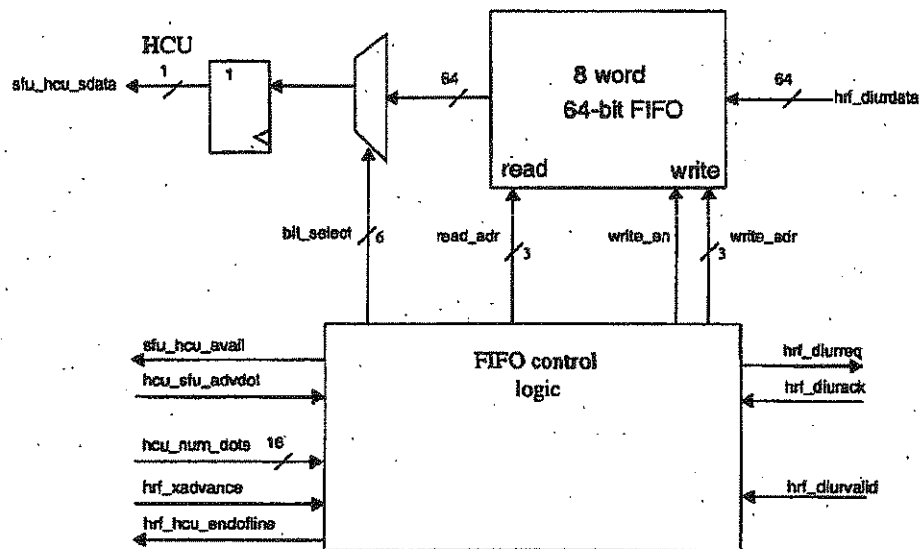


FIG. 182

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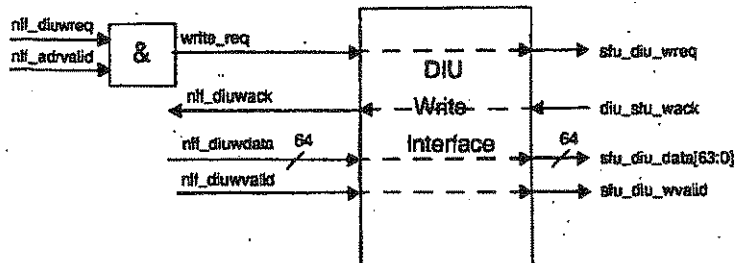


FIG. 183

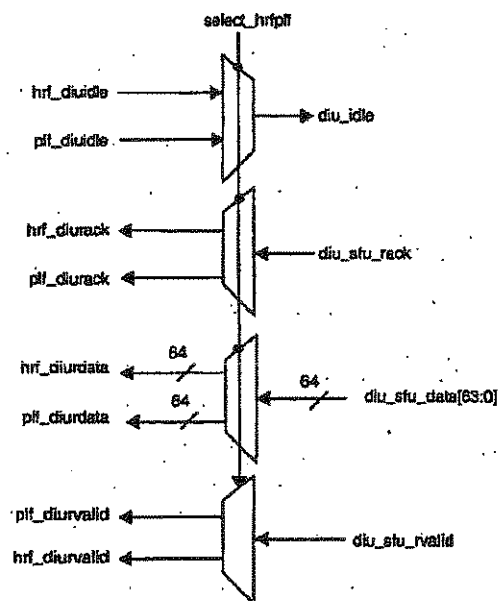


FIG. 184

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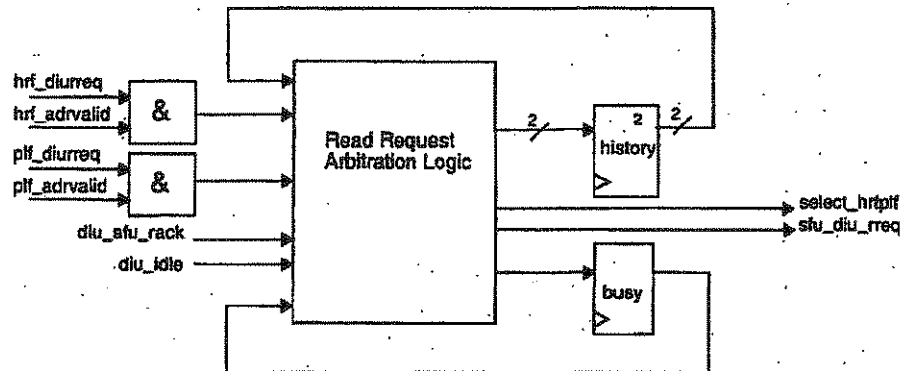


FIG. 185

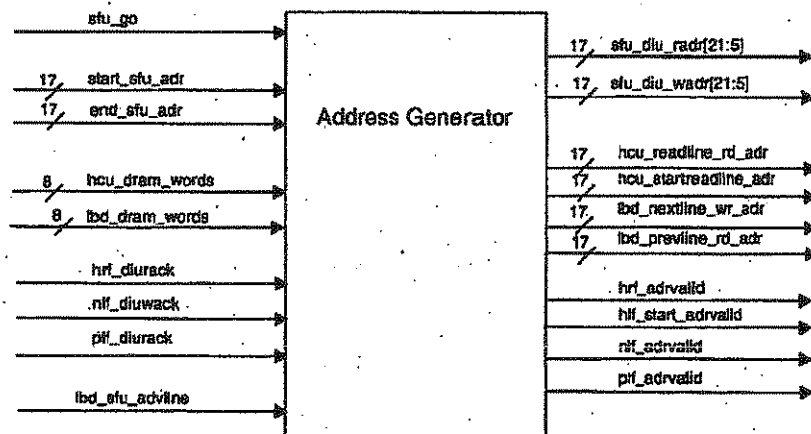


FIG. 186

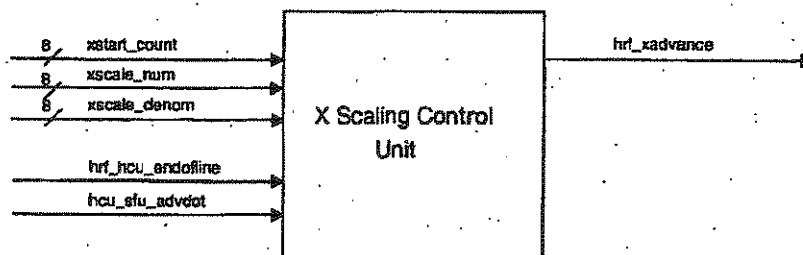


FIG. 187

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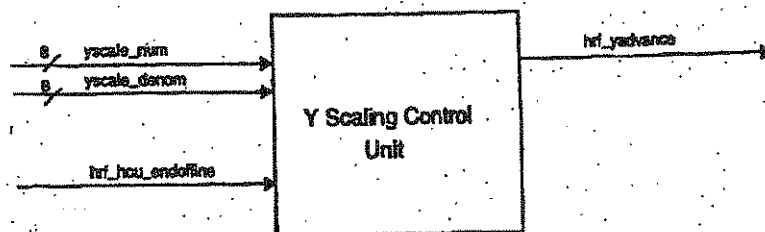


FIG. 188

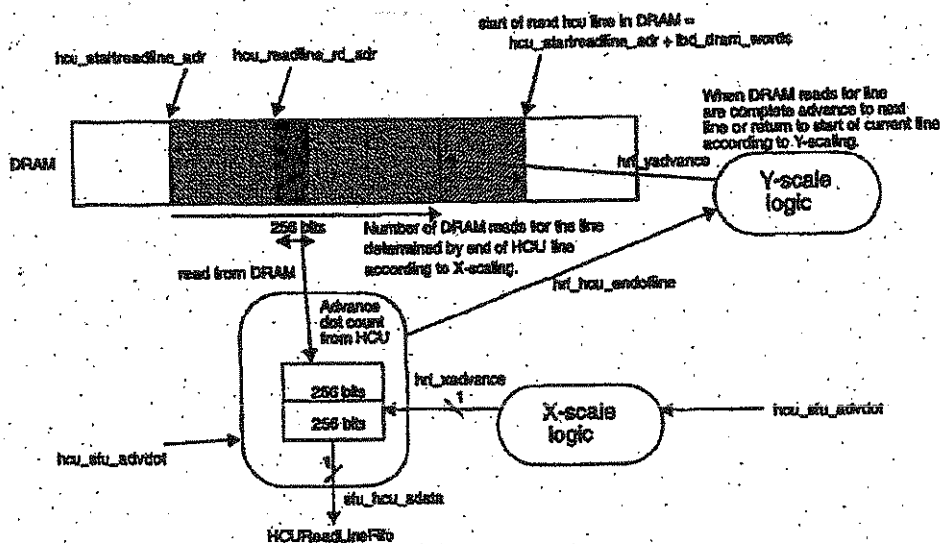


FIG. 189

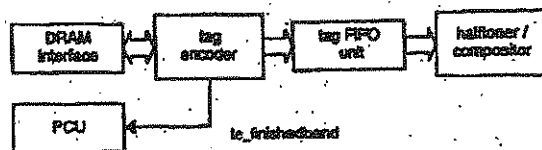


FIG. 190

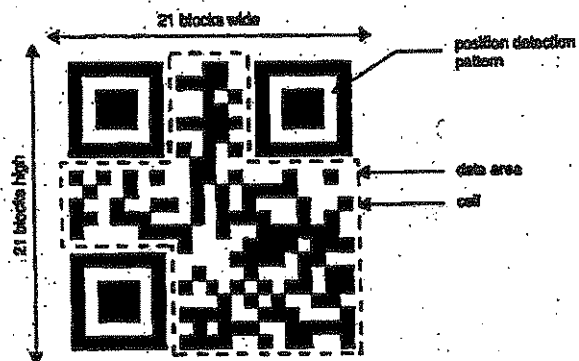


FIG. 191

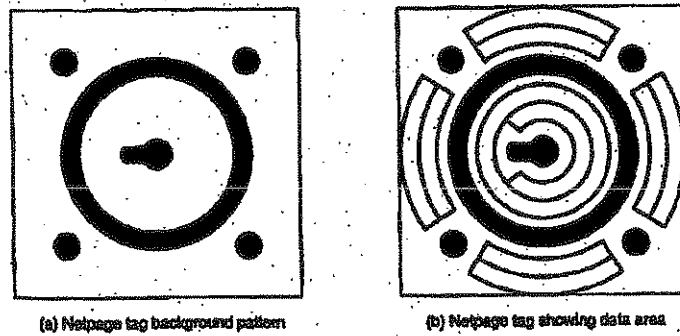


FIG. 192

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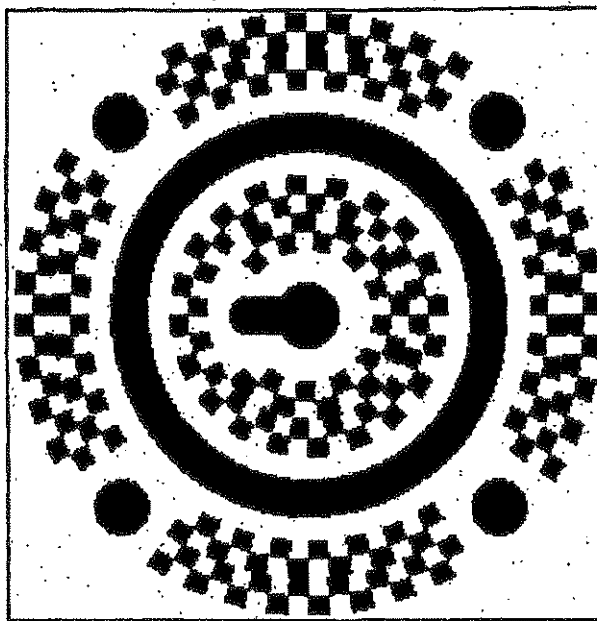


FIG. 193

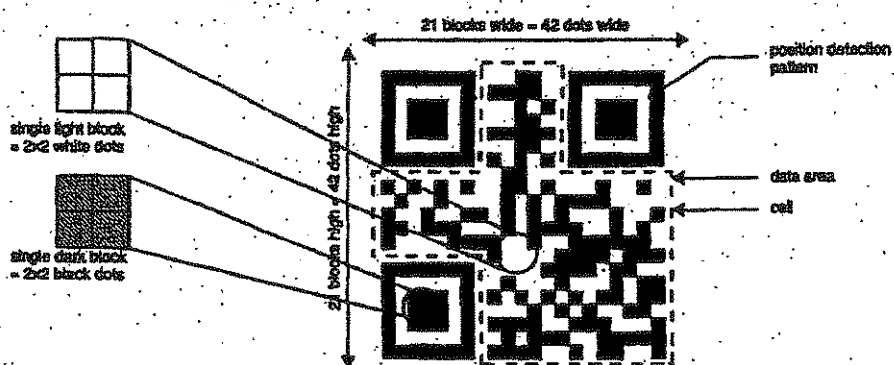


FIG. 194

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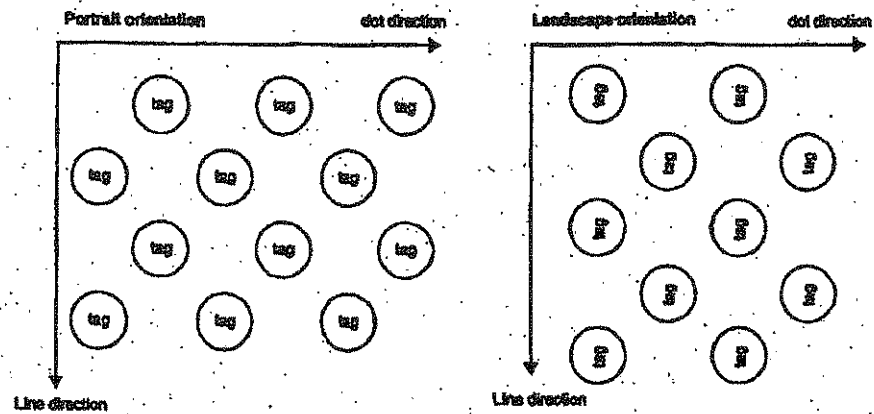


FIG. 195

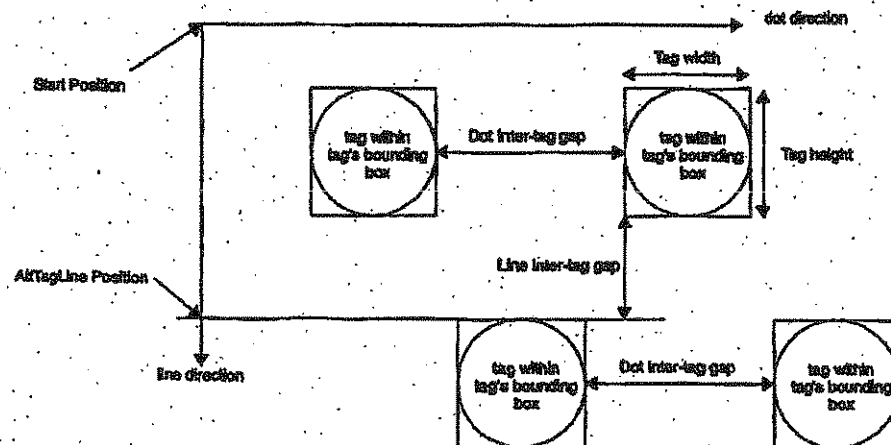


FIG. 196

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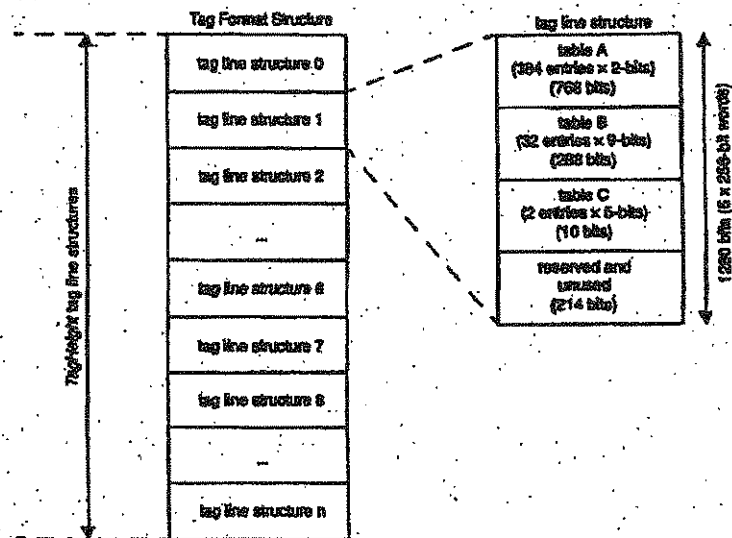


FIG. 197

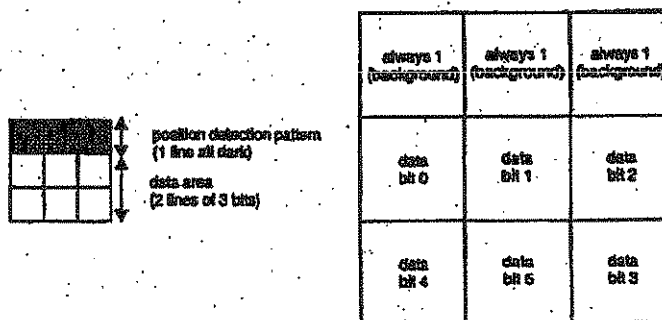


FIG. 198

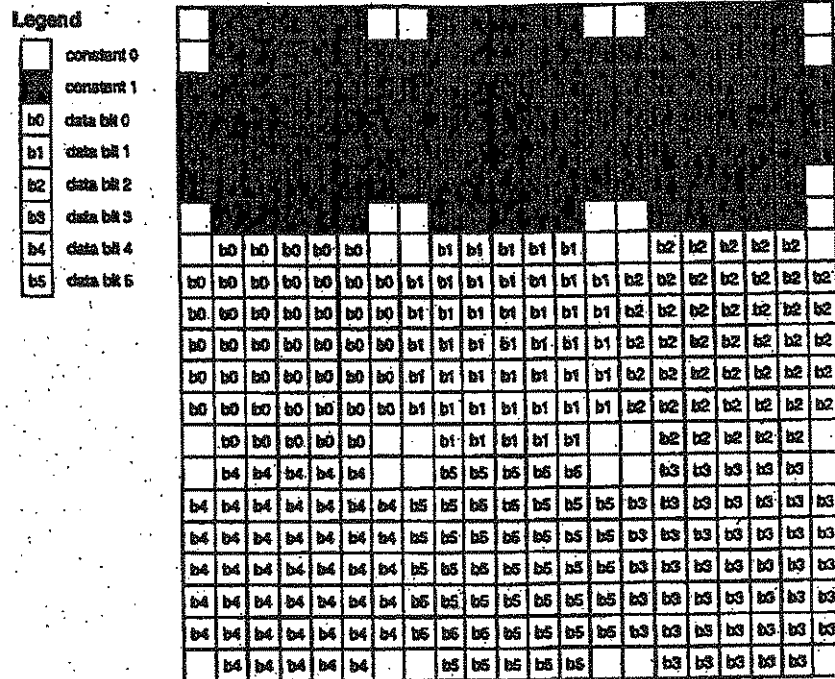


FIG. 199

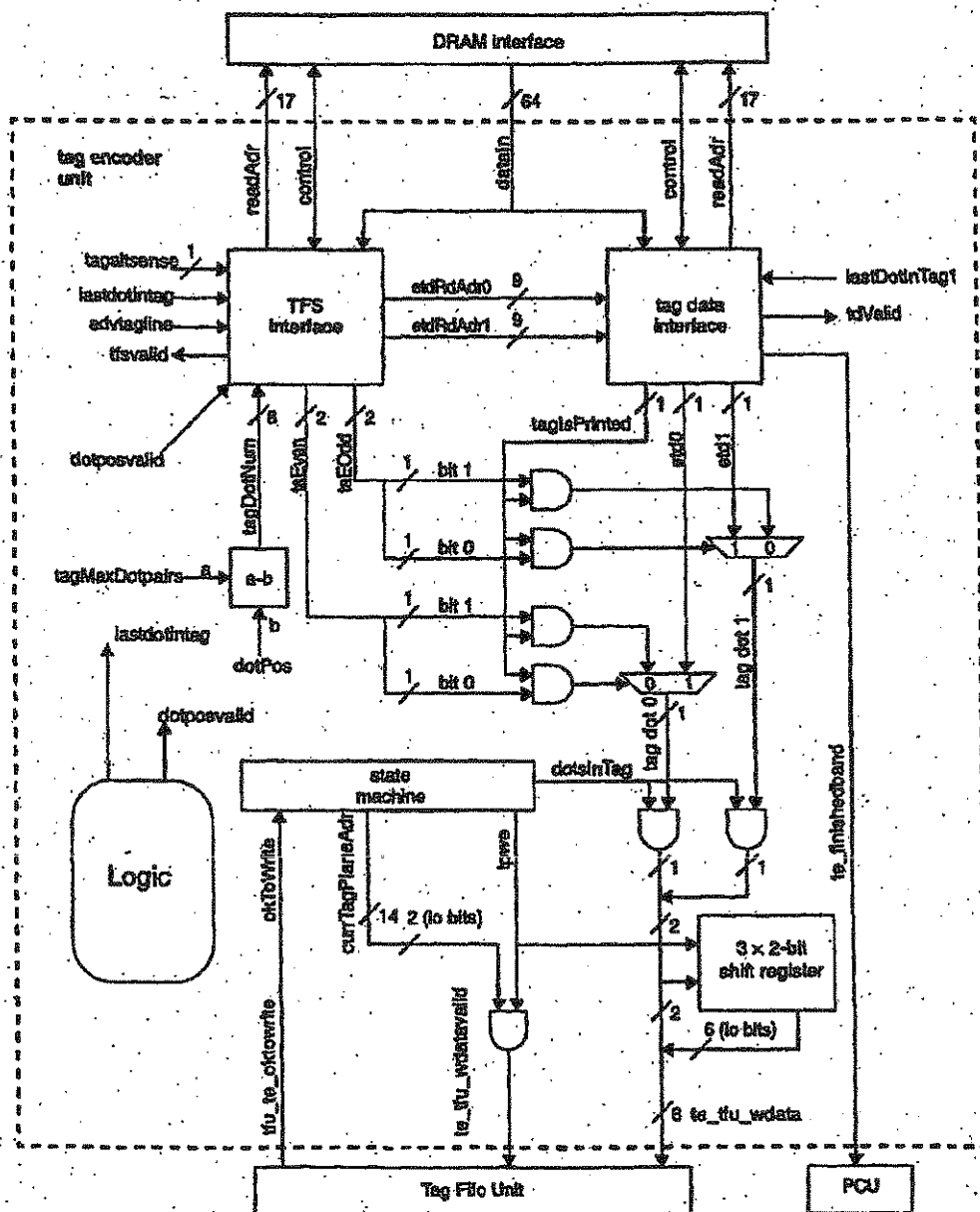


FIG. 200

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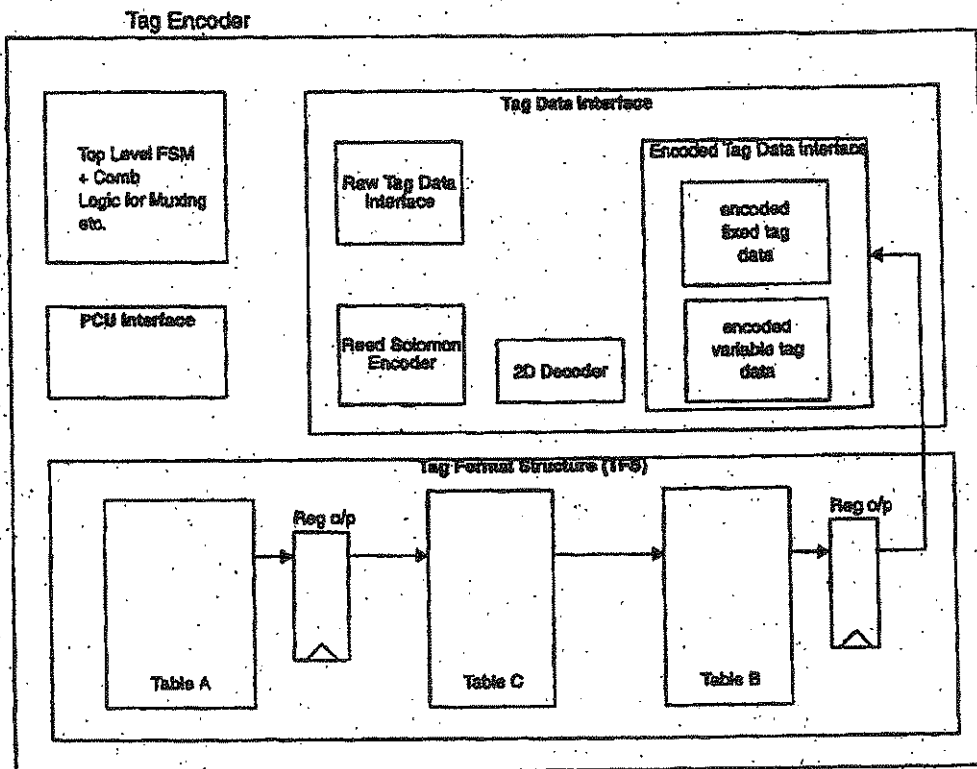


FIG. 201

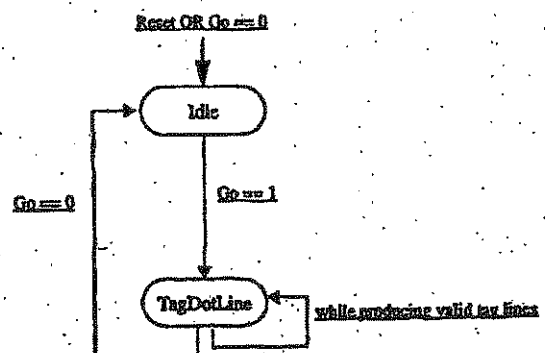


FIG. 202

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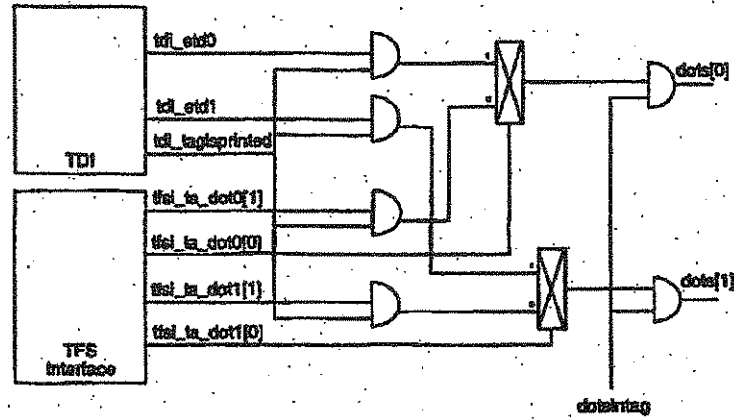


FIG. 203

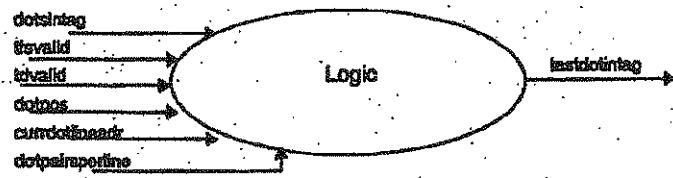


FIG. 204

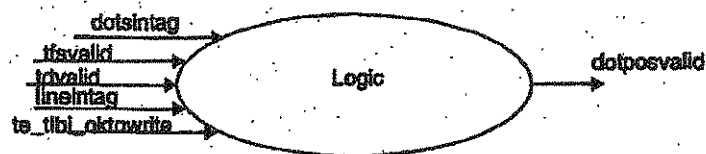


FIG. 205

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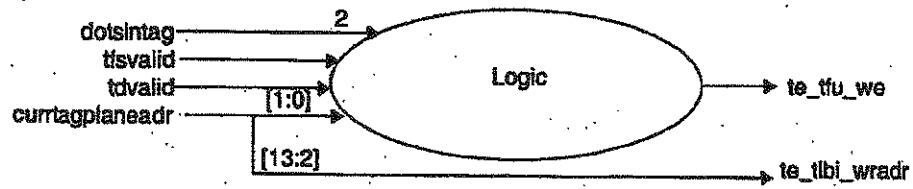


FIG. 206

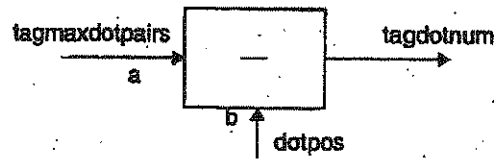


FIG. 207

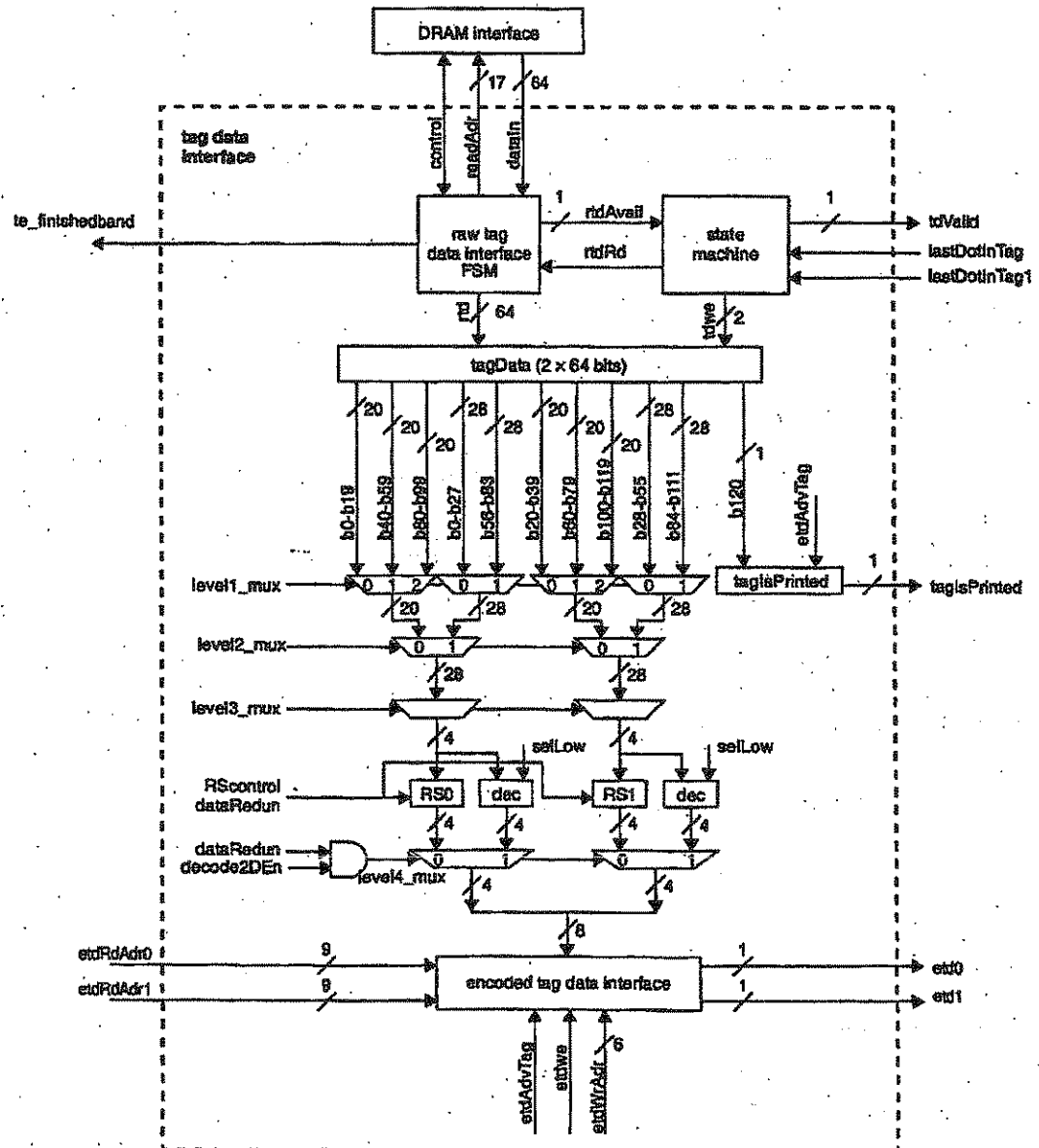


FIG. 208

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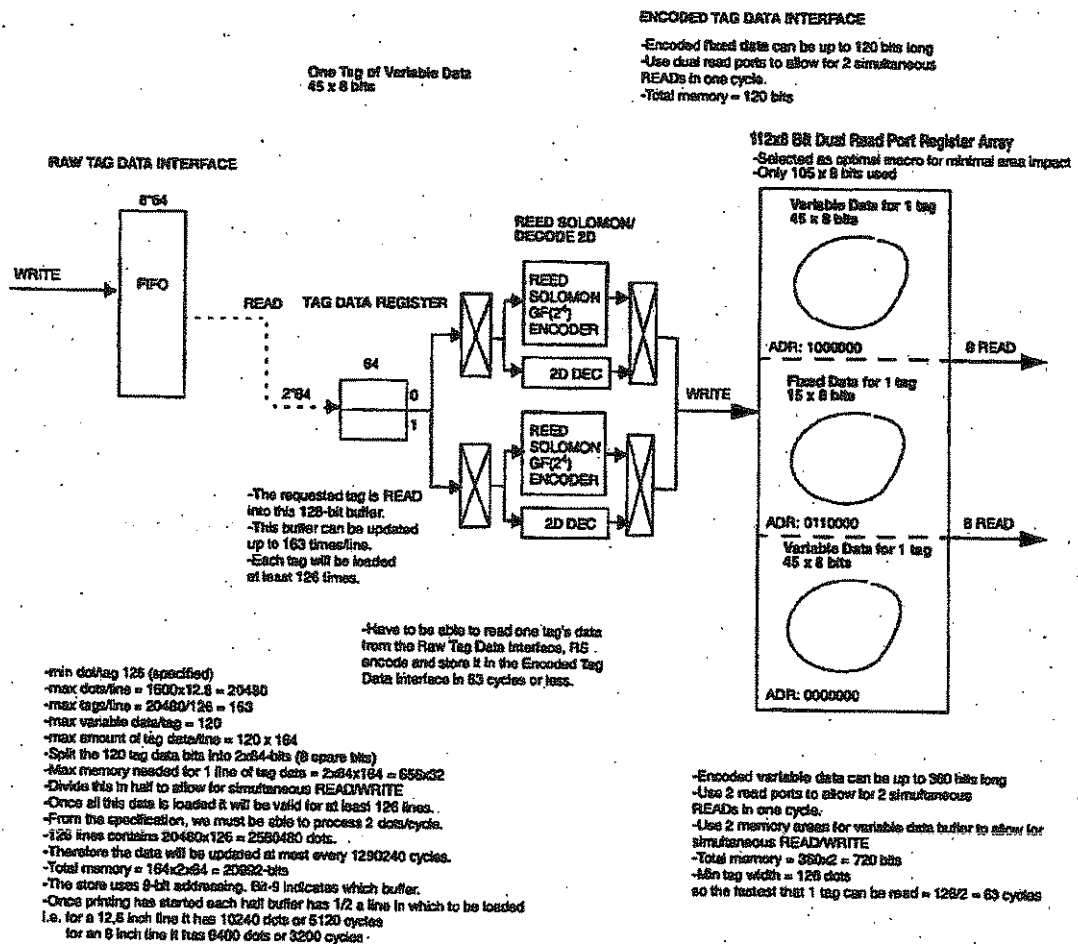


FIG. 209

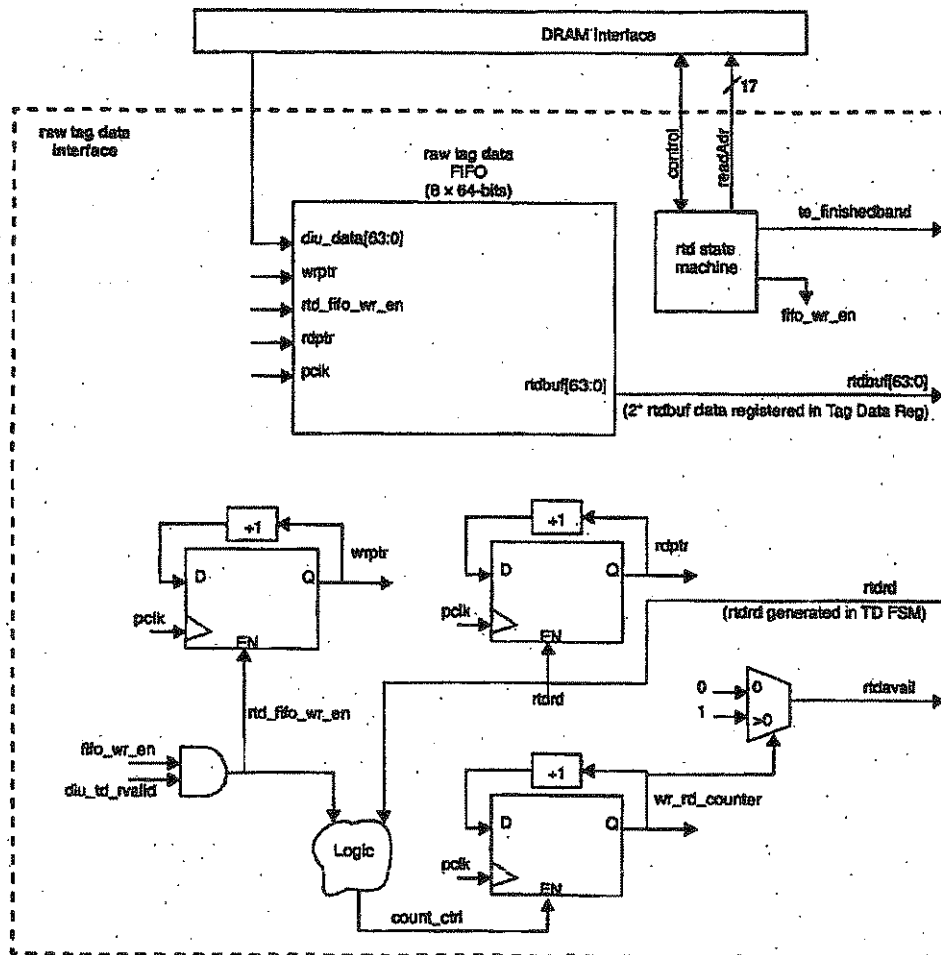


FIG. 210

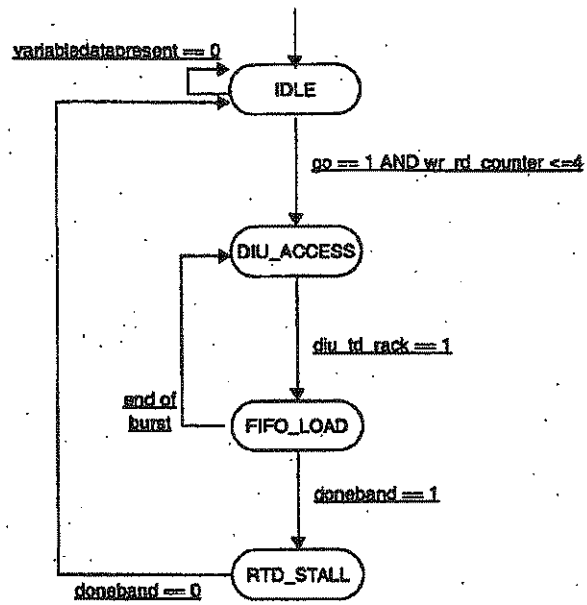


FIG. 211

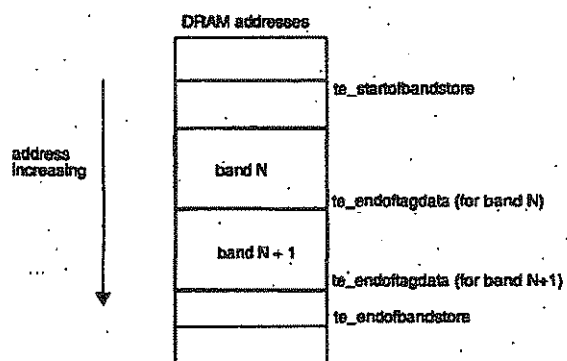


FIG. 212

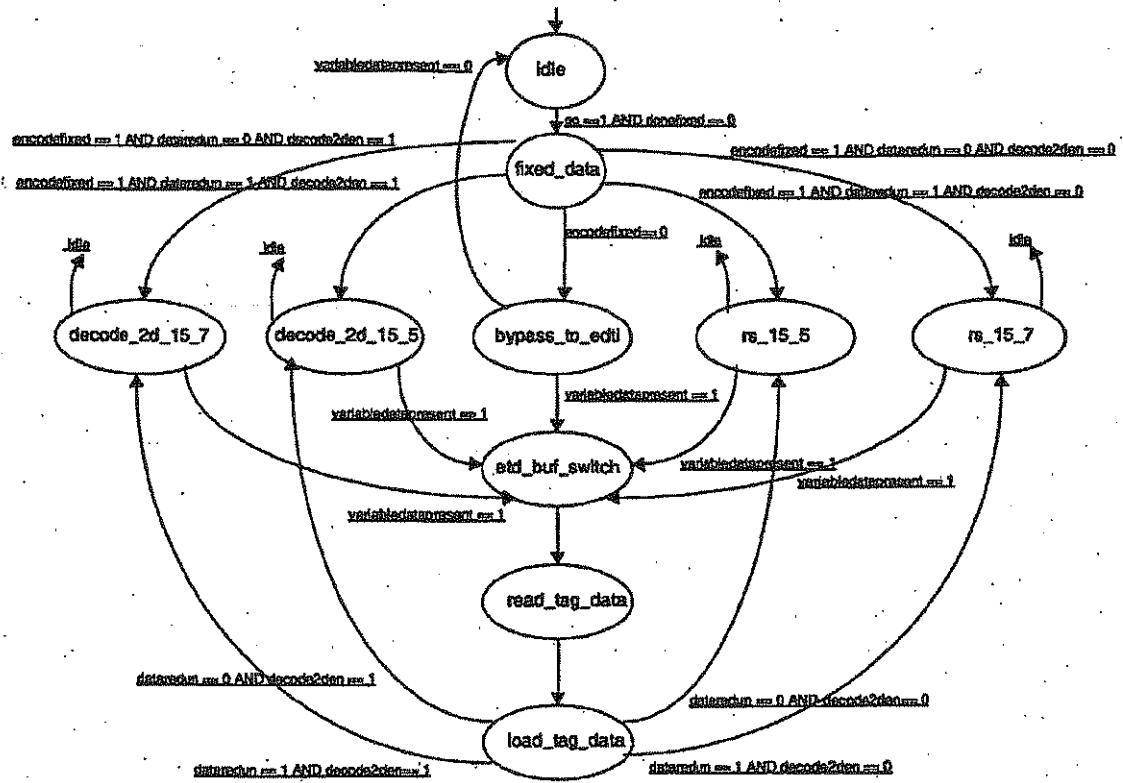


FIG. 213

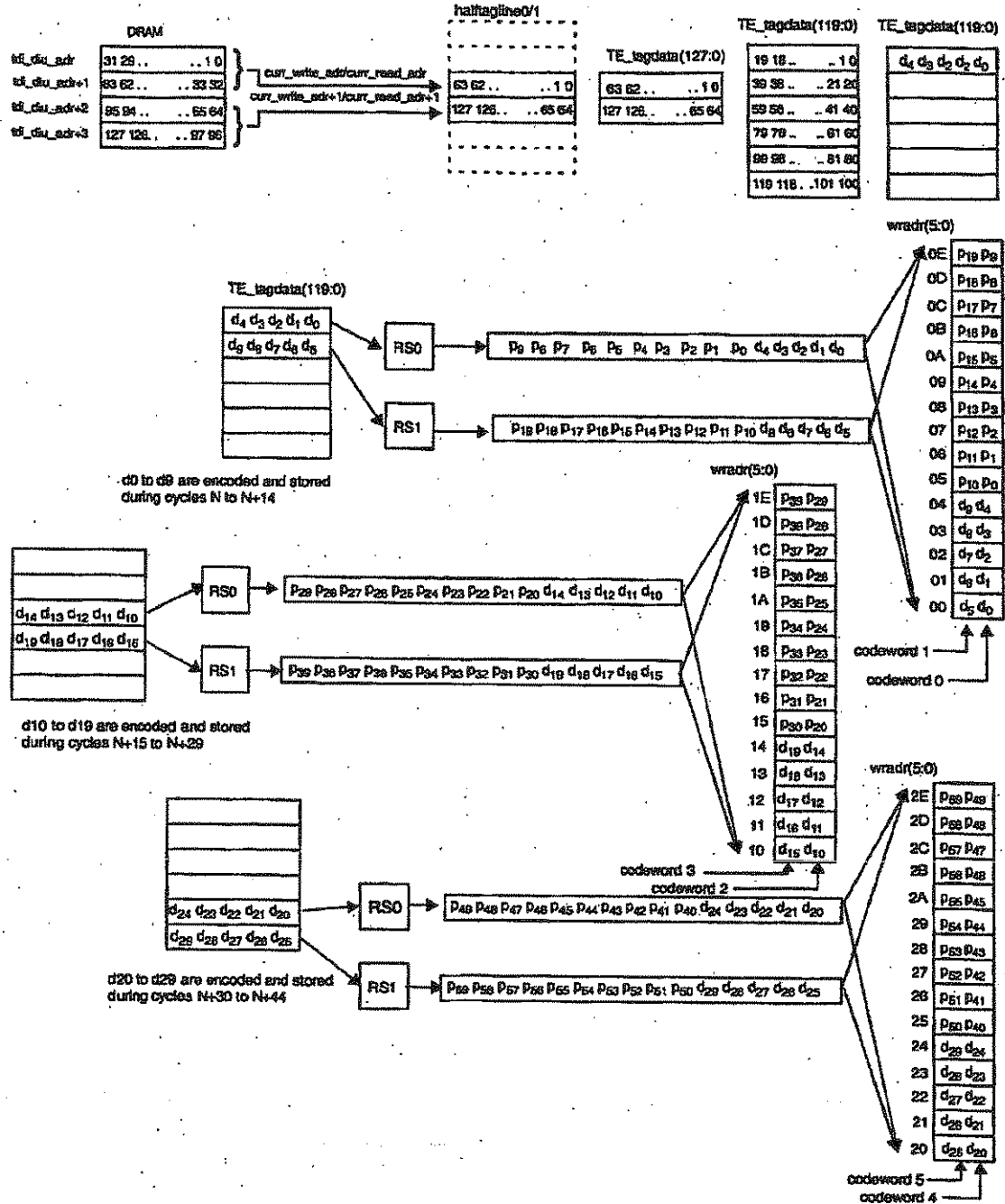


FIG. 214

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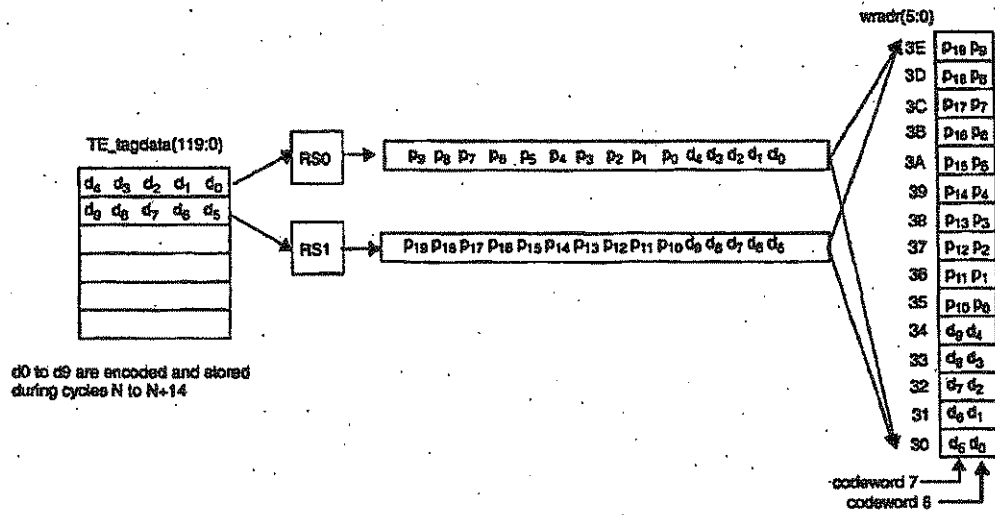


FIG. 215

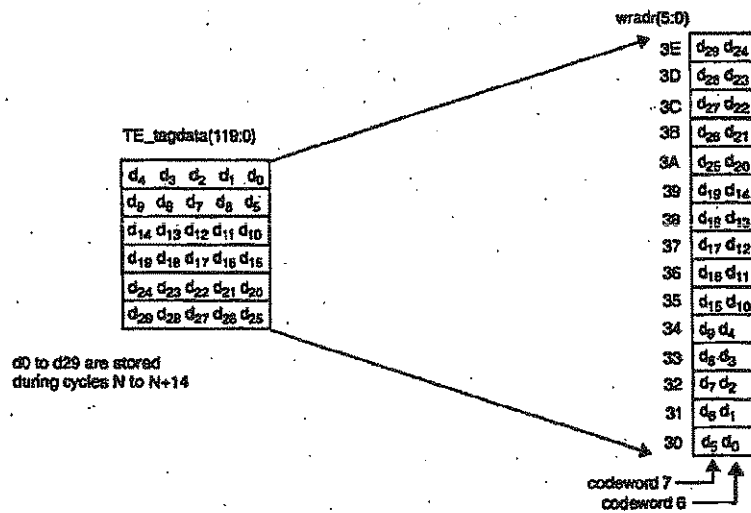


FIG. 216

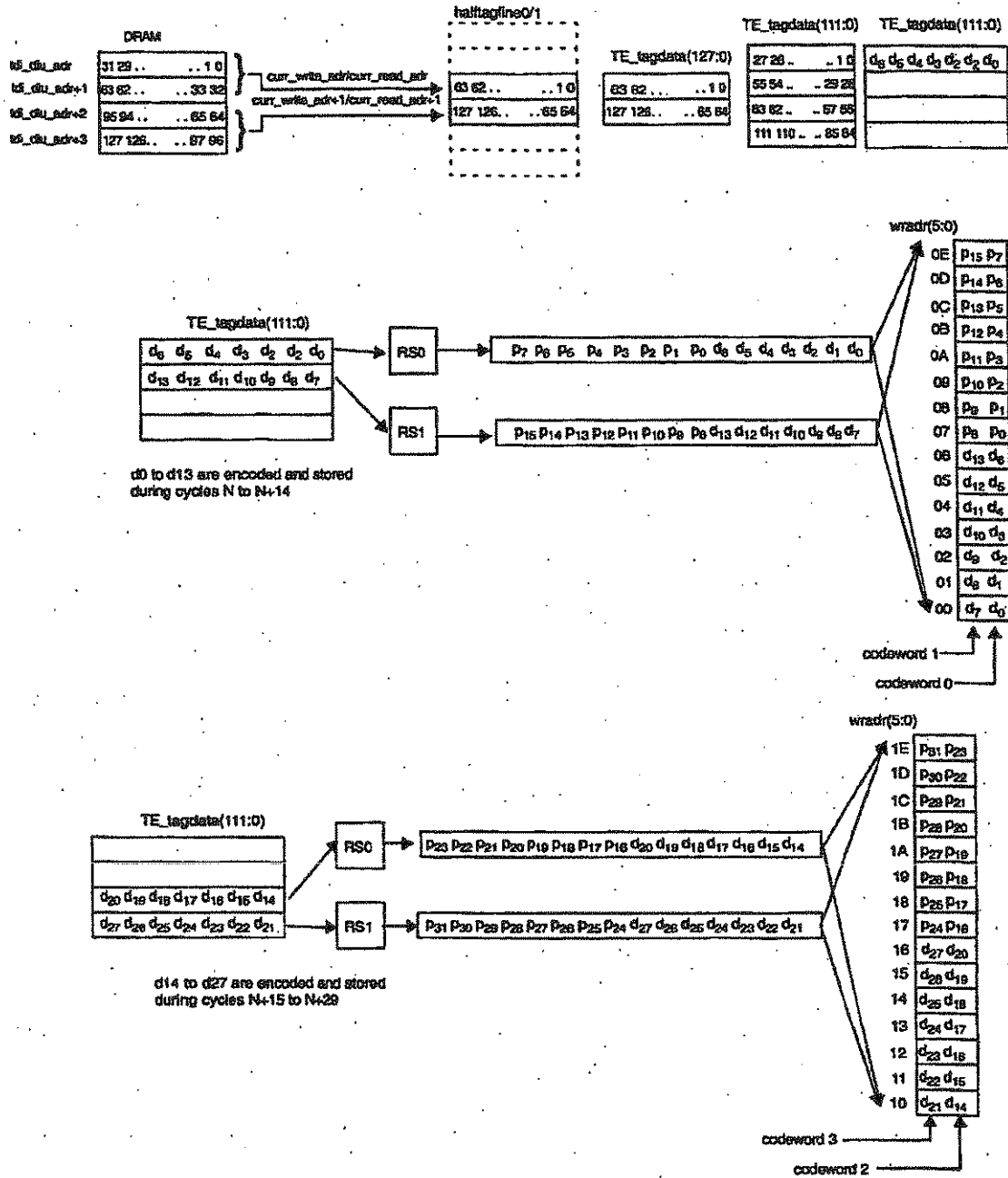


FIG. 217

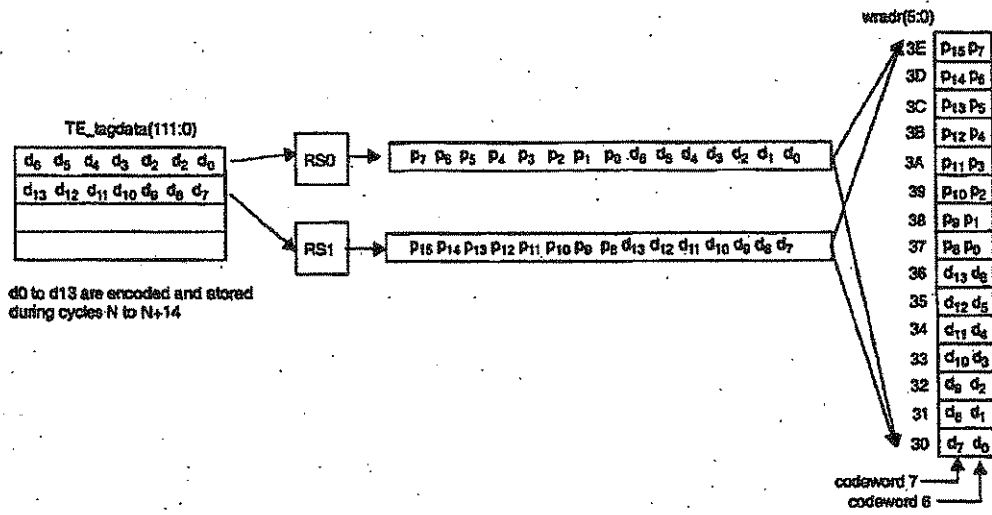


FIG. 218

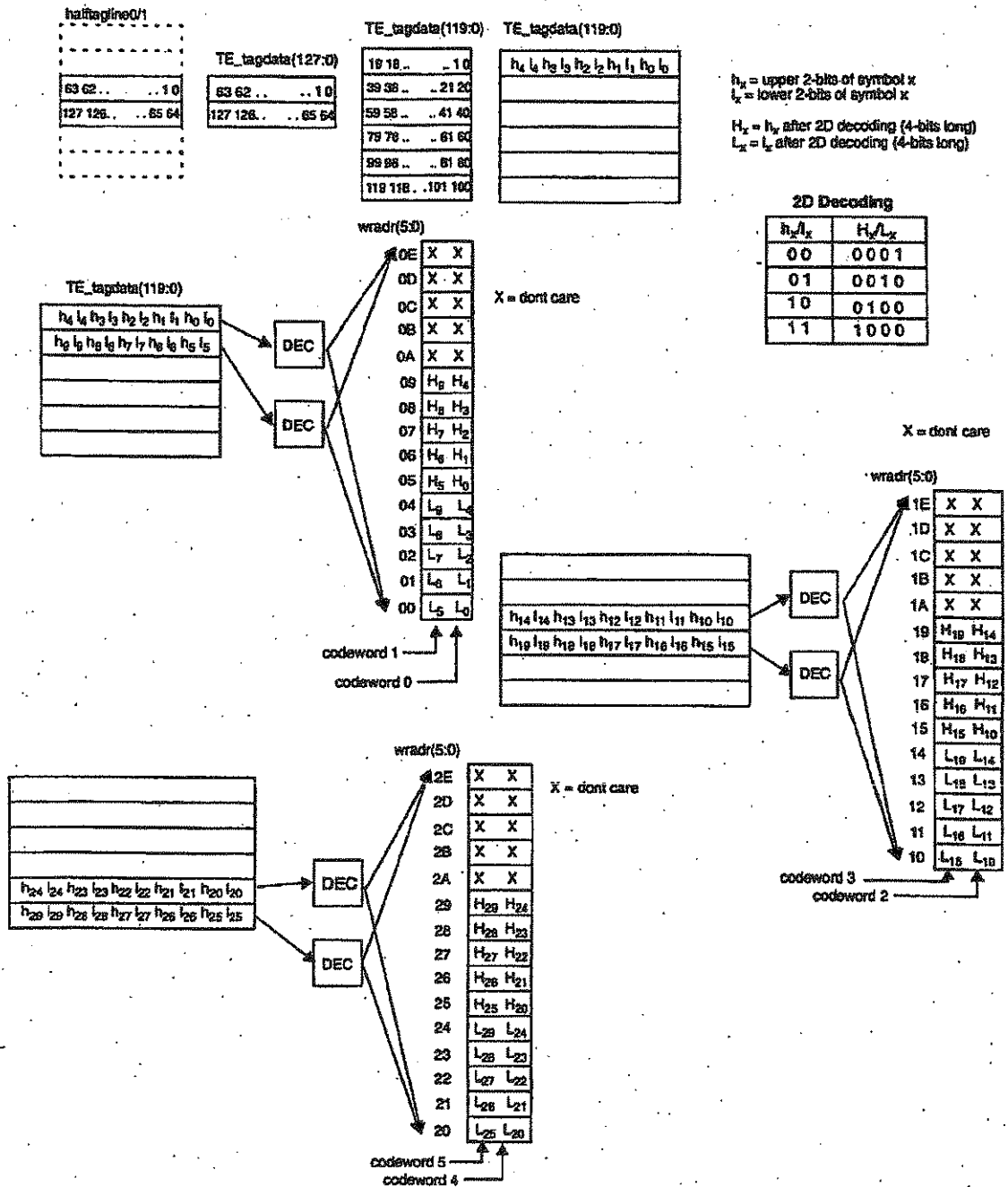


FIG. 219

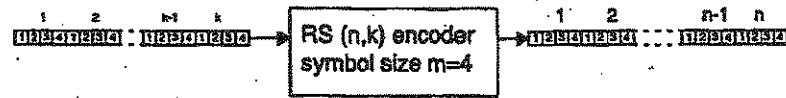


FIG. 220

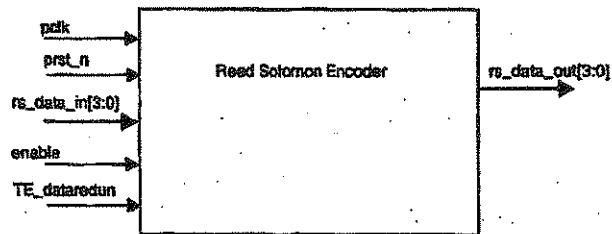


FIG. 221

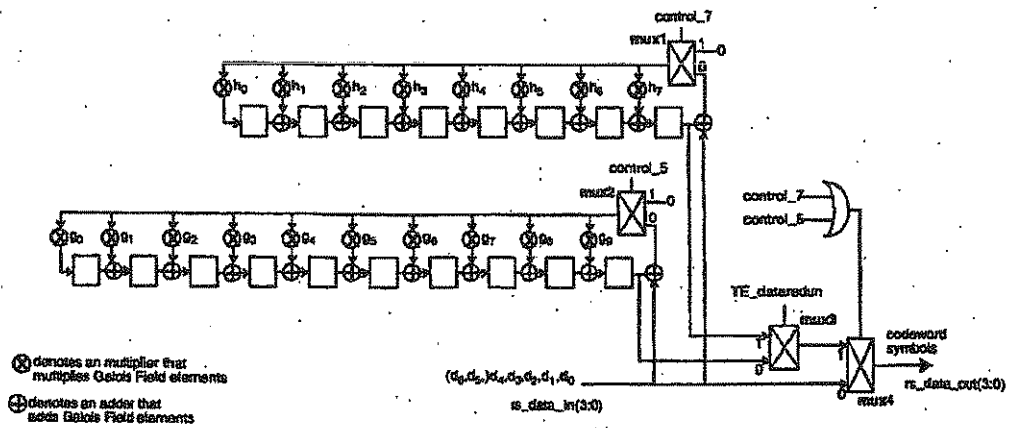


FIG. 222

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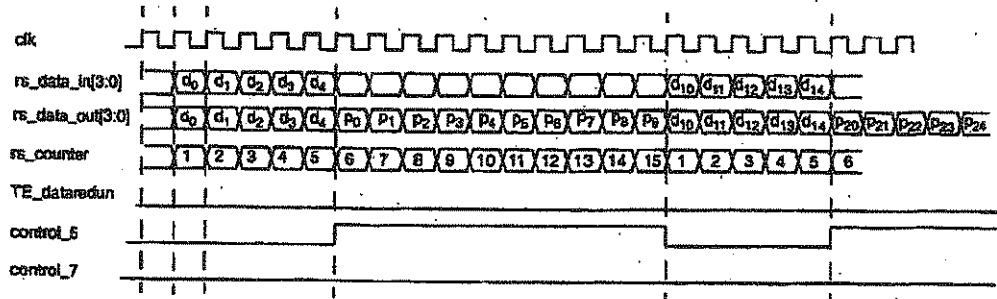


FIG. 223

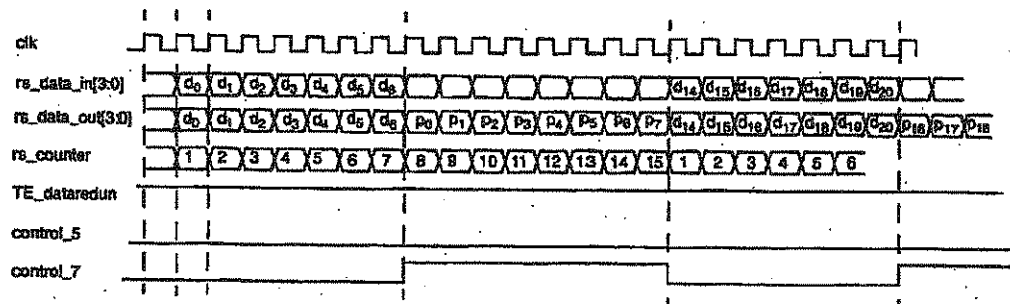


FIG. 224

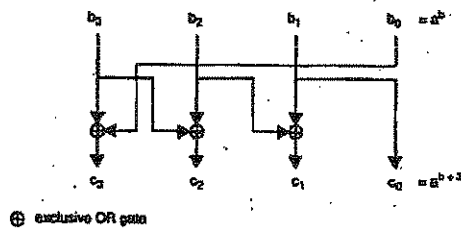


FIG. 225

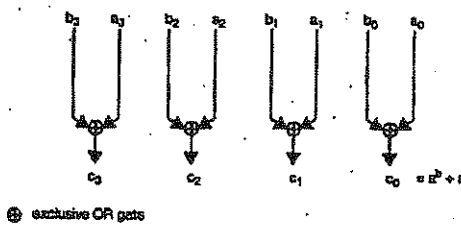


FIG. 226

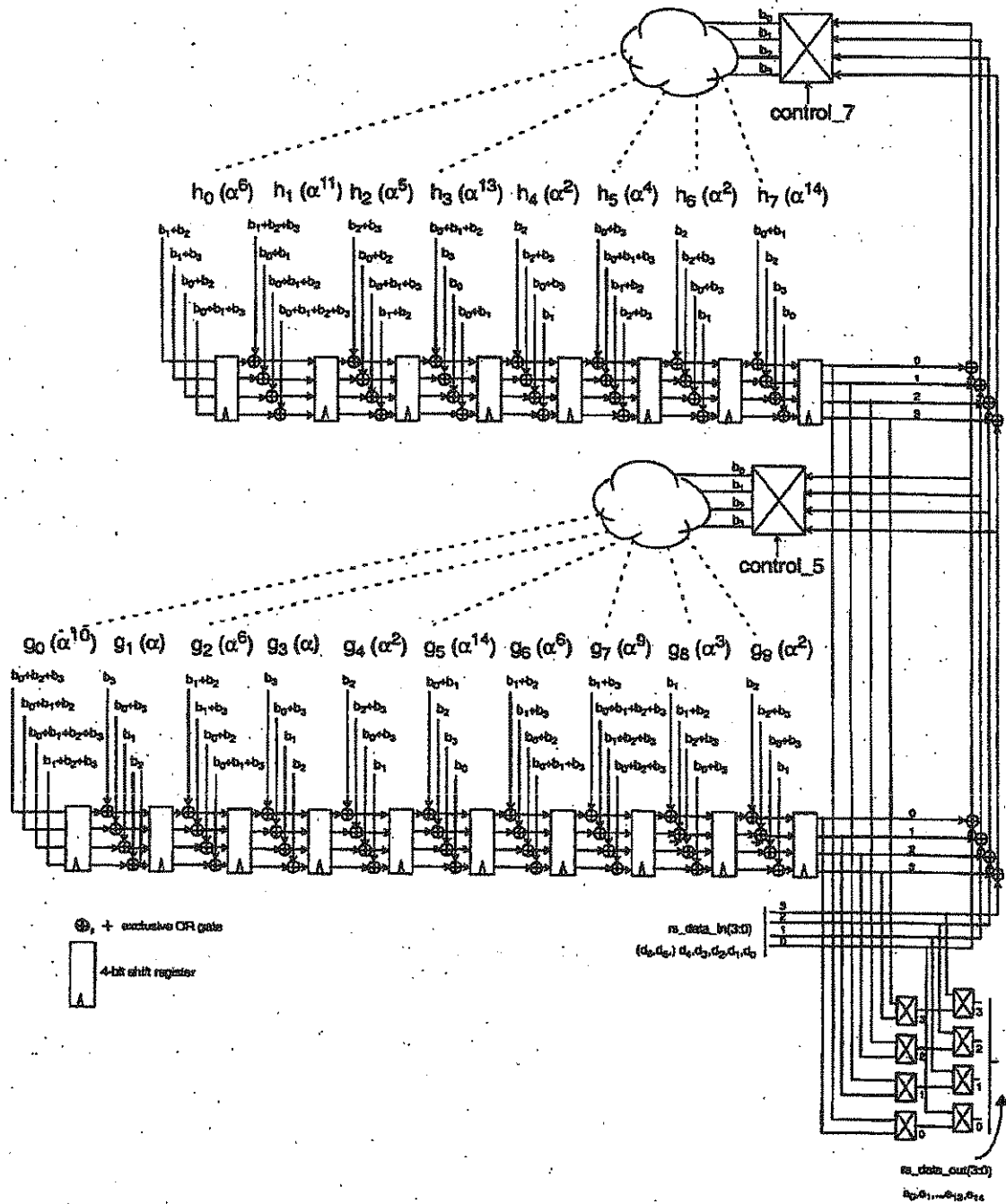


FIG. 227

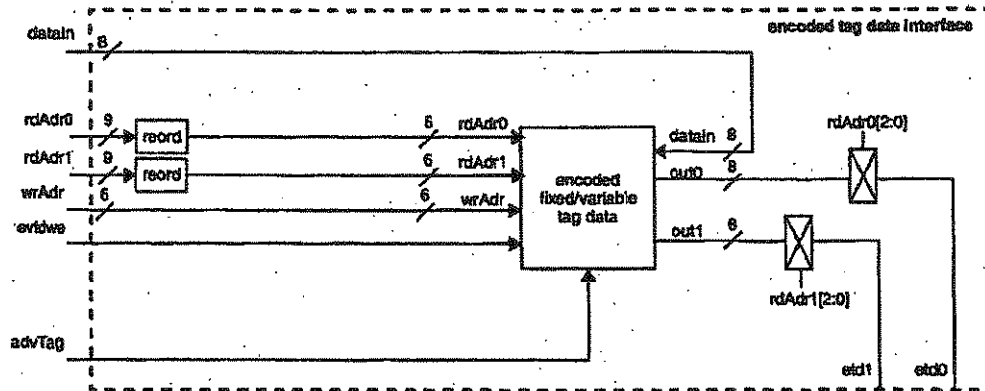


FIG. 228

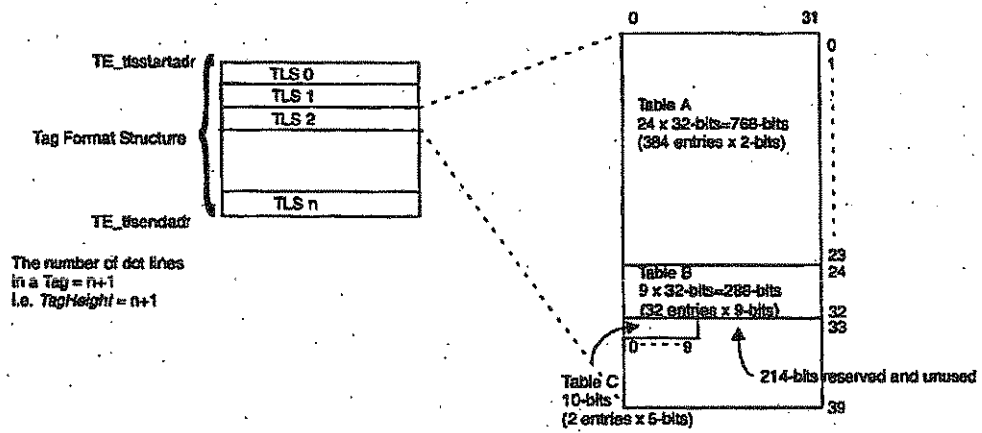


FIG. 229

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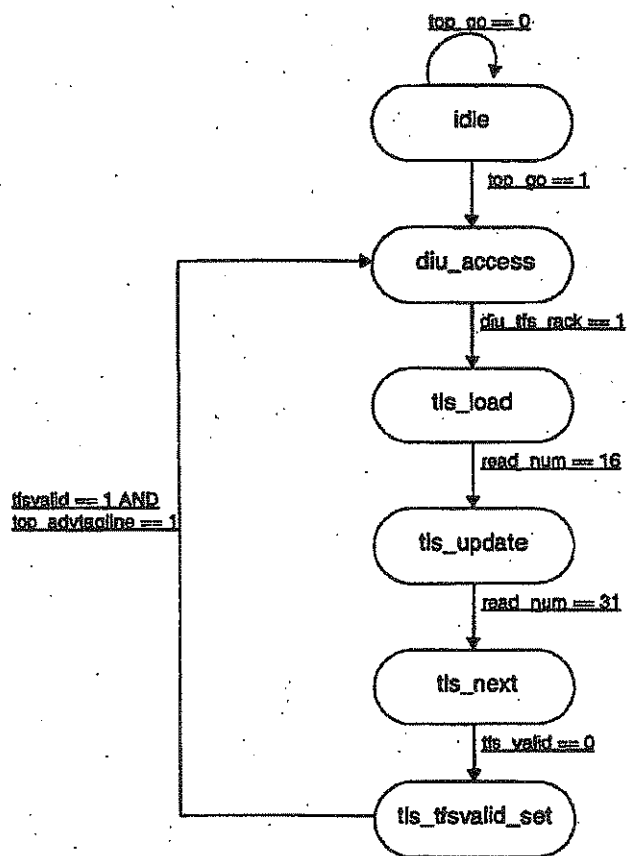


FIG. 230

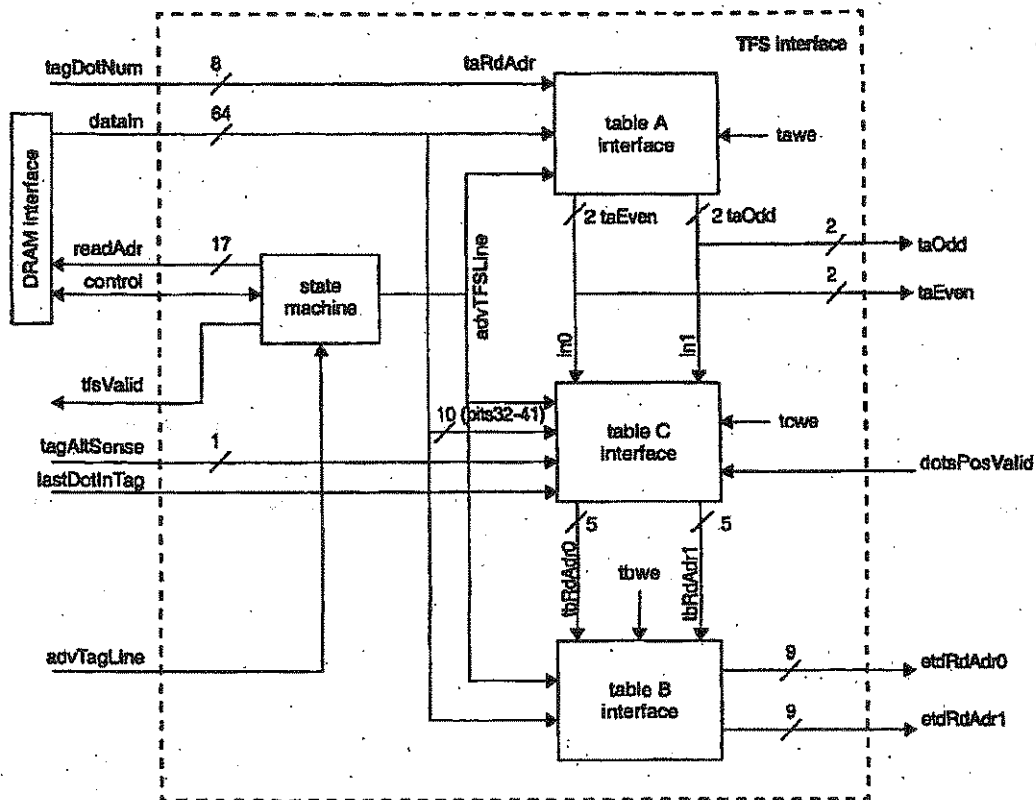


FIG. 231

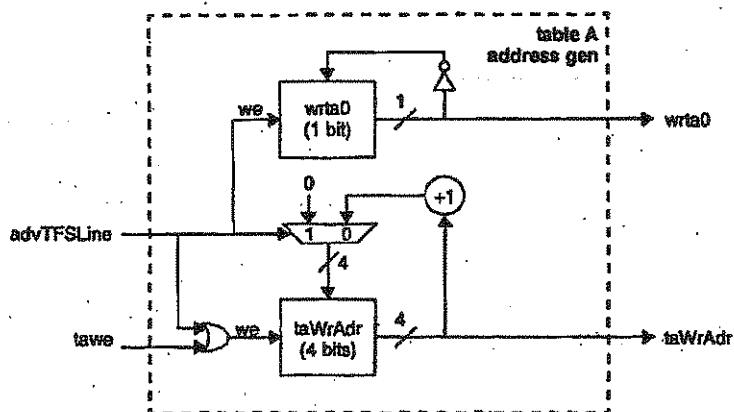


FIG. 232

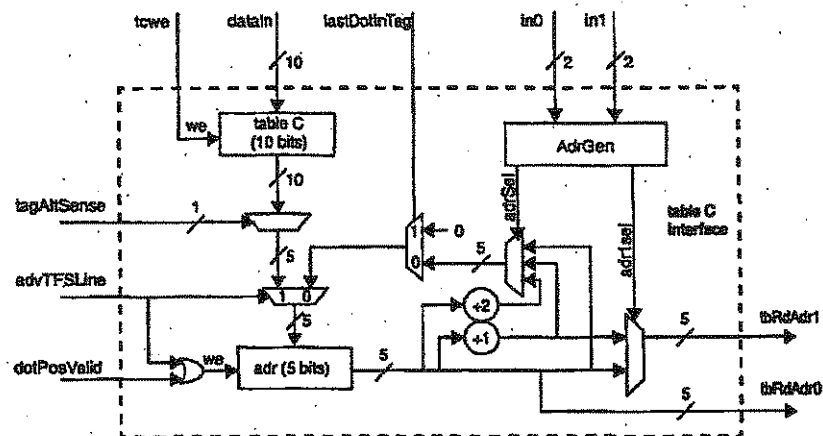


FIG. 233

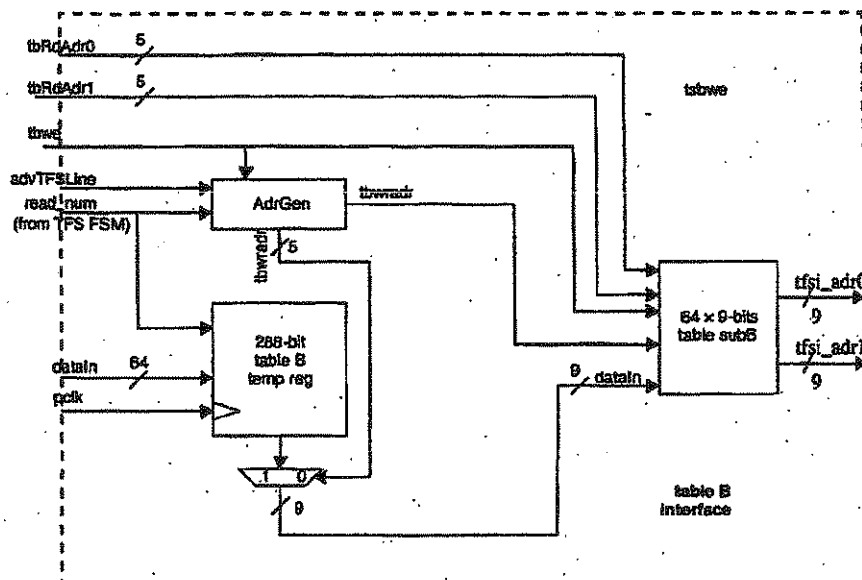


FIG. 234

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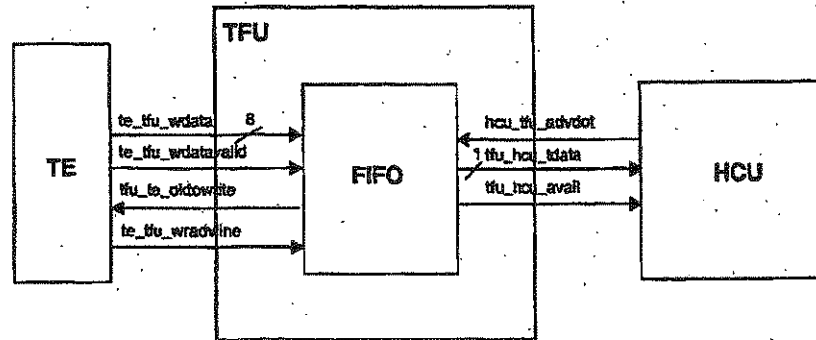


FIG. 235

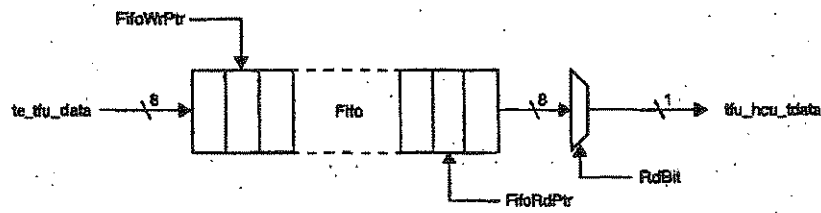


FIG. 236

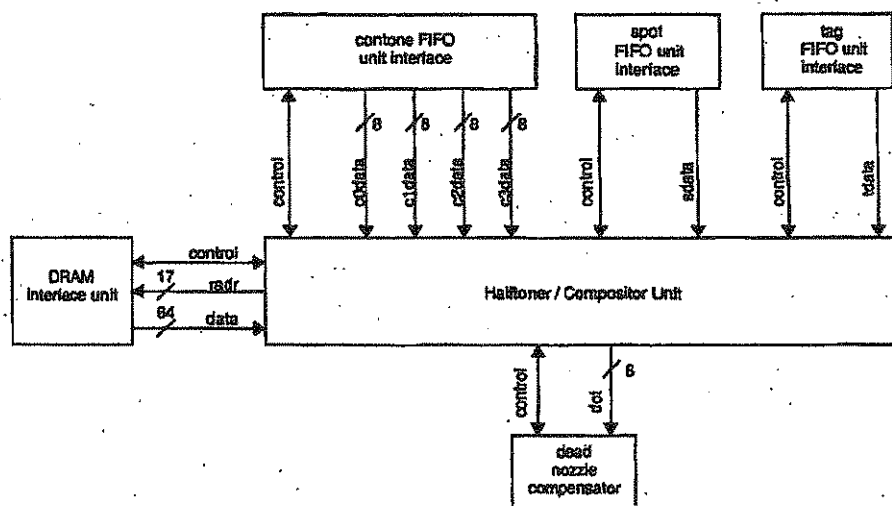


FIG. 237

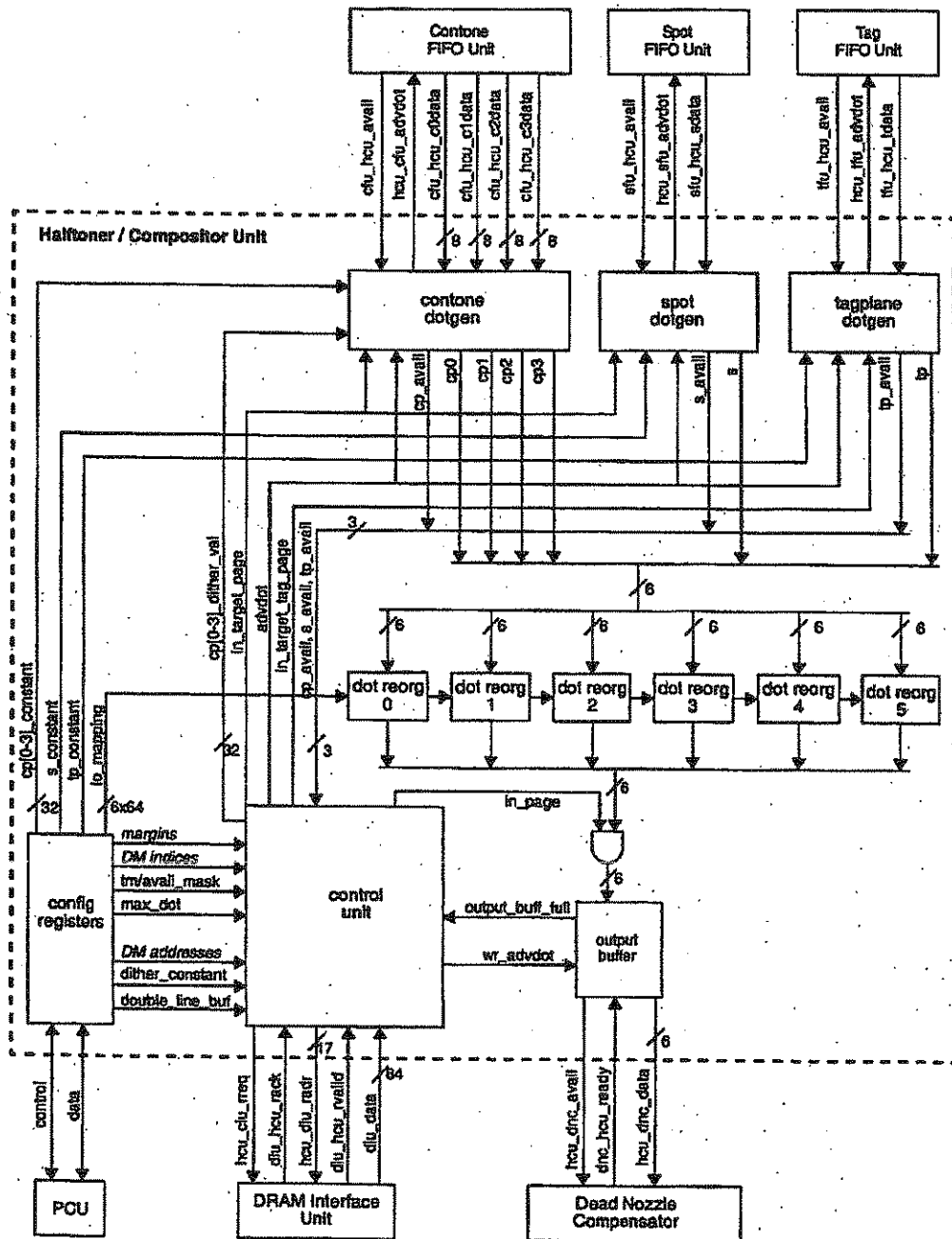


FIG. 238

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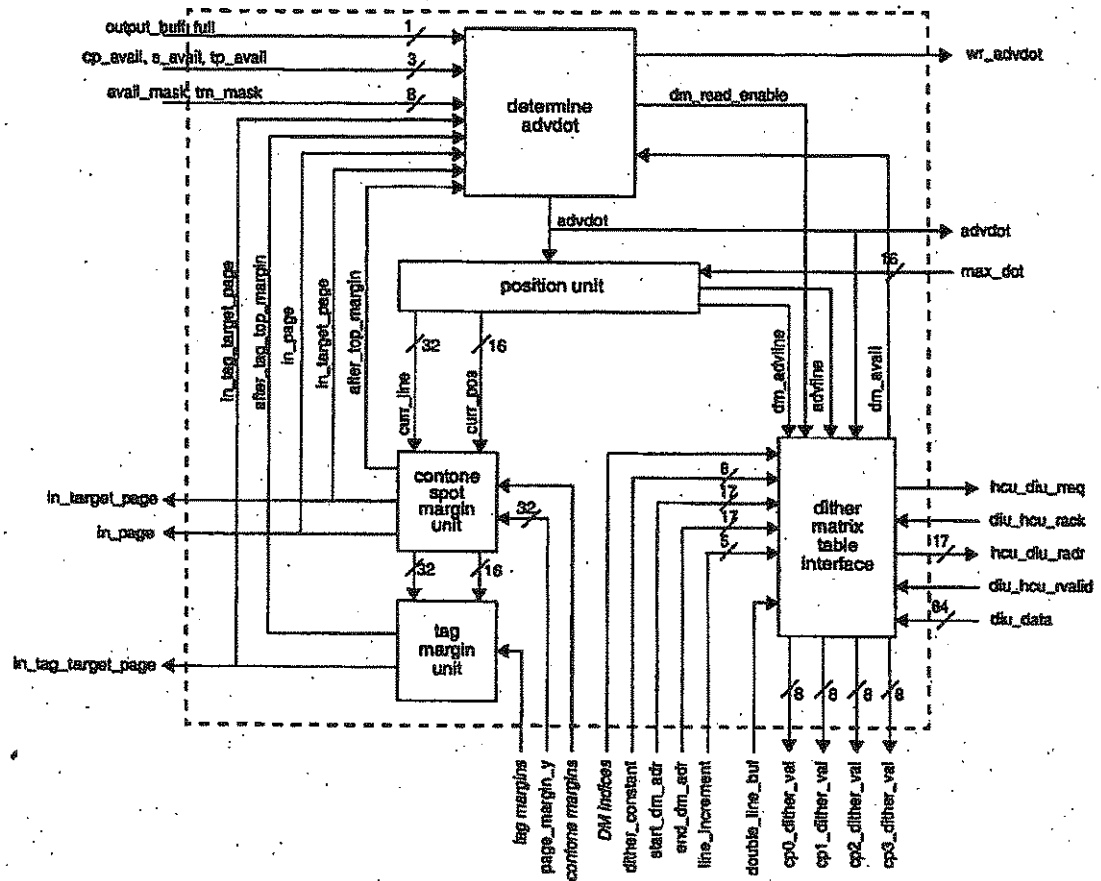


FIG. 239

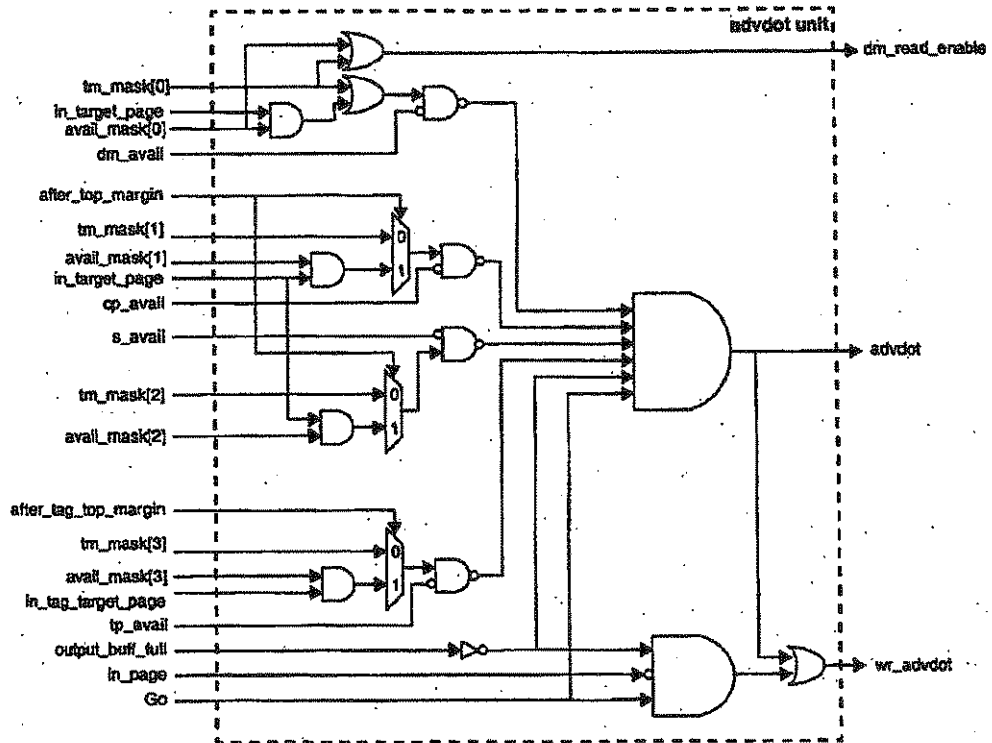


FIG. 240

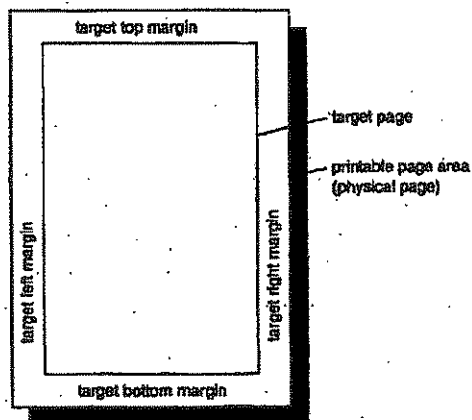


FIG. 241

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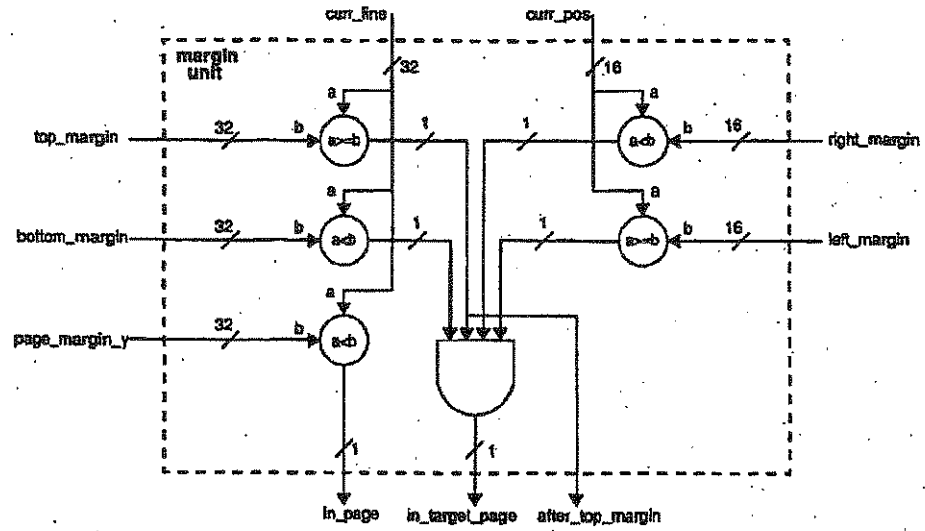


FIG. 242

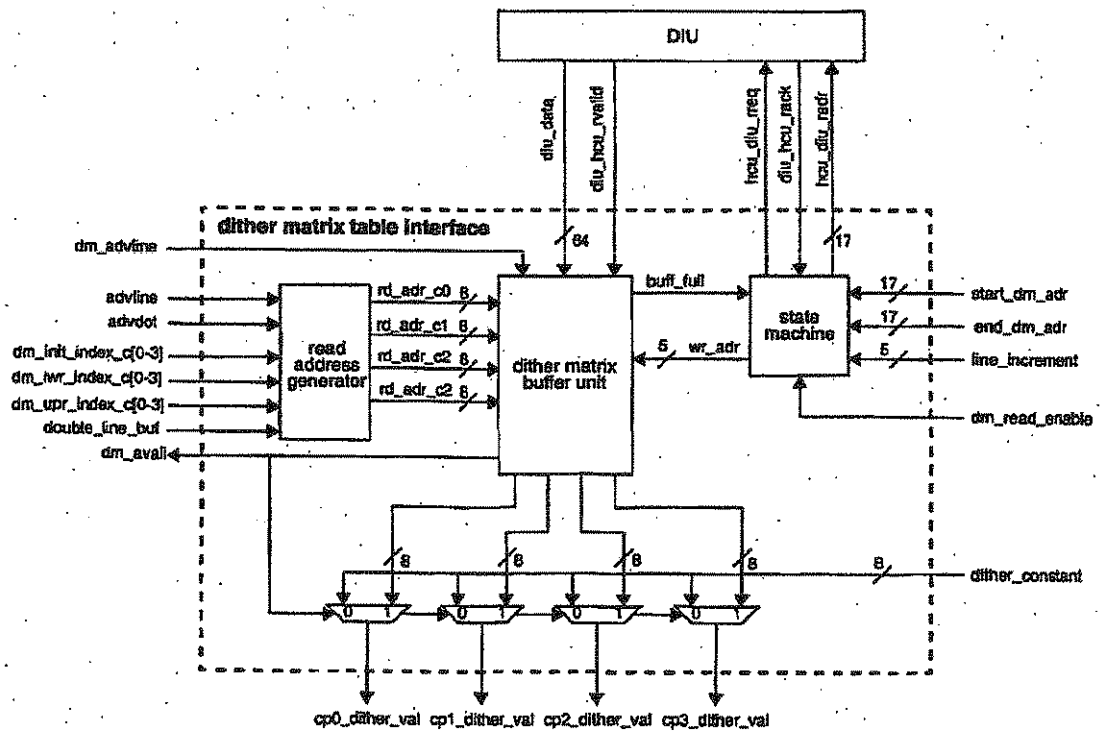


FIG. 243

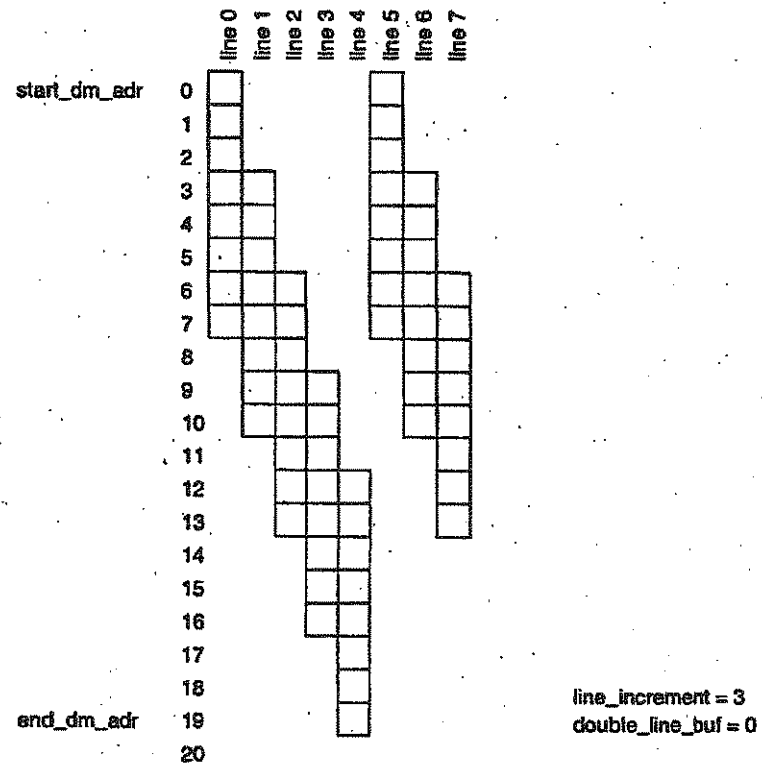


FIG. 244

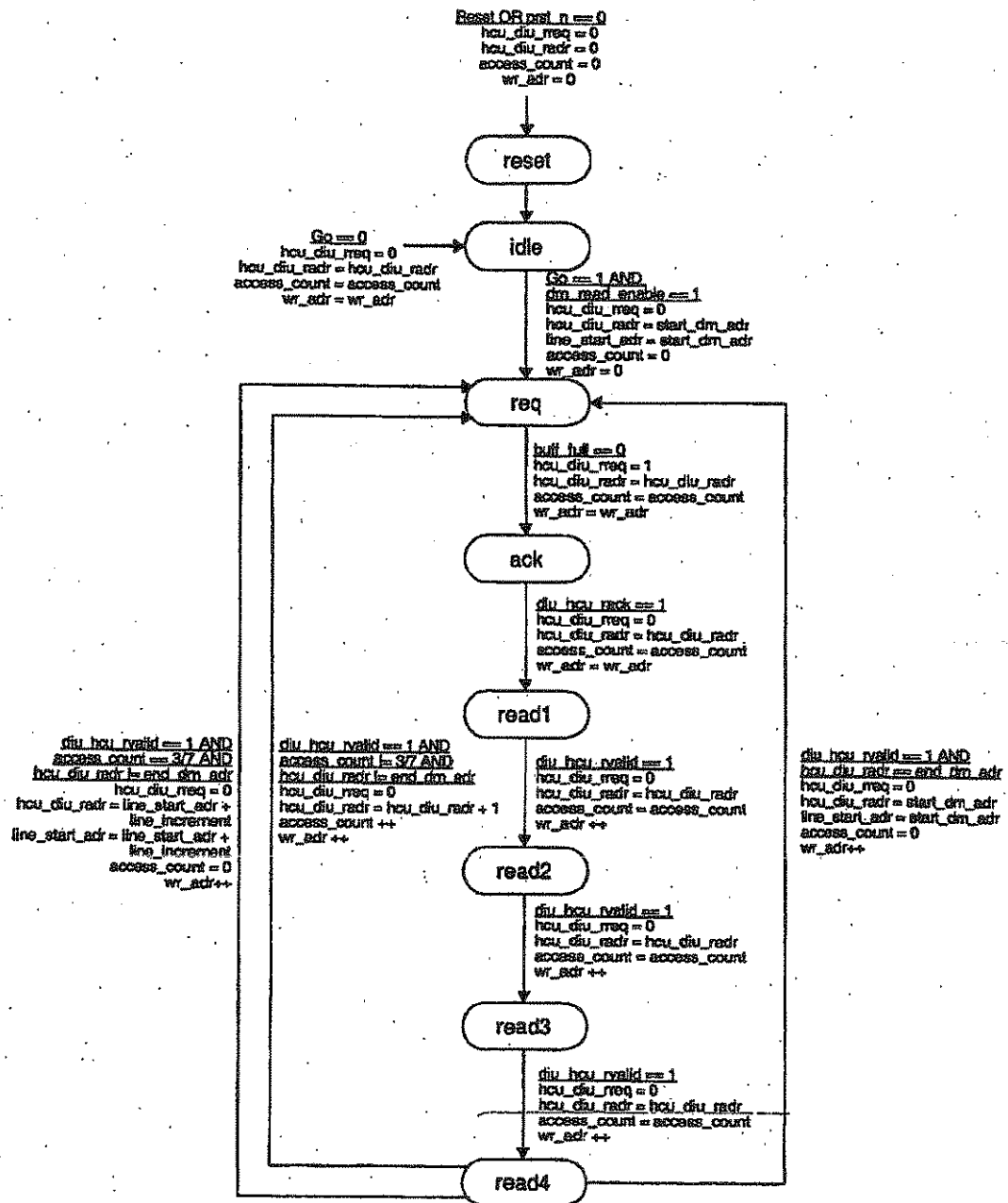


FIG. 245

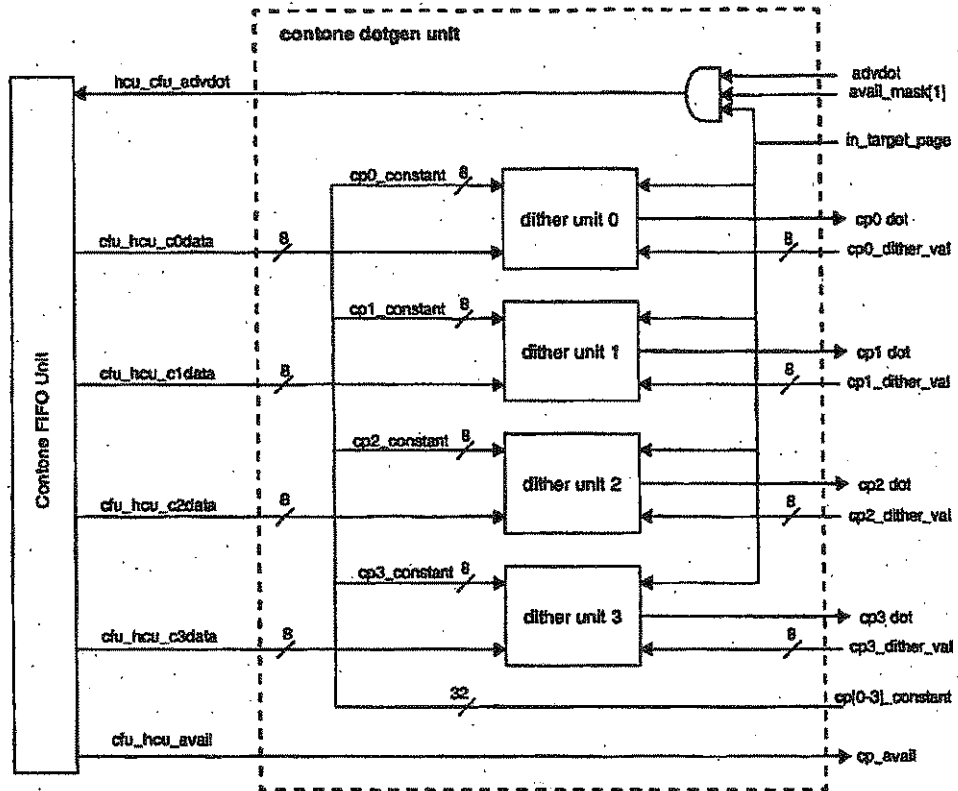


FIG. 246

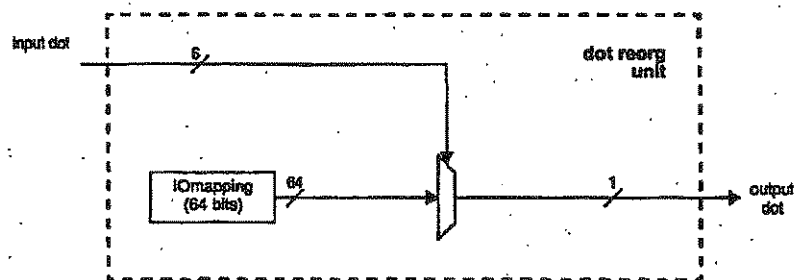


FIG. 247

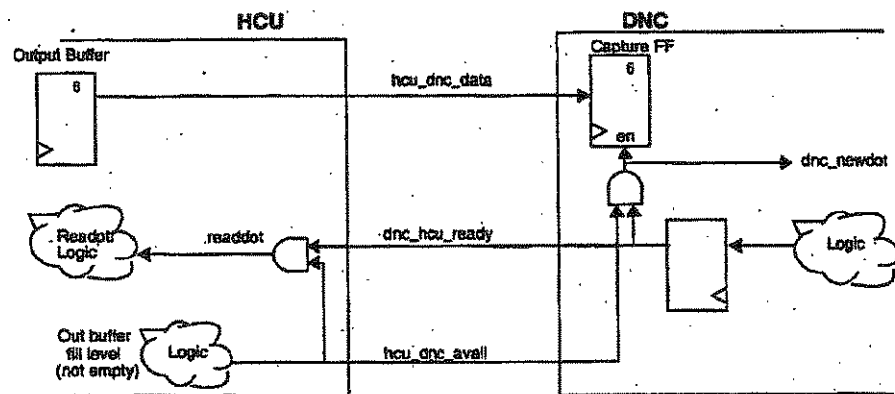
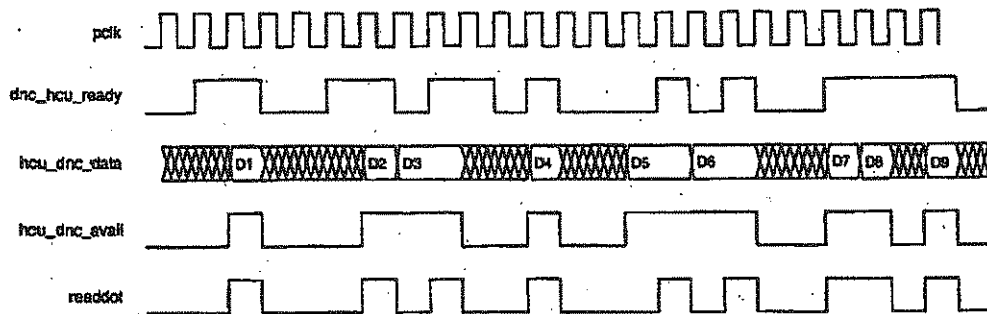


FIG. 248

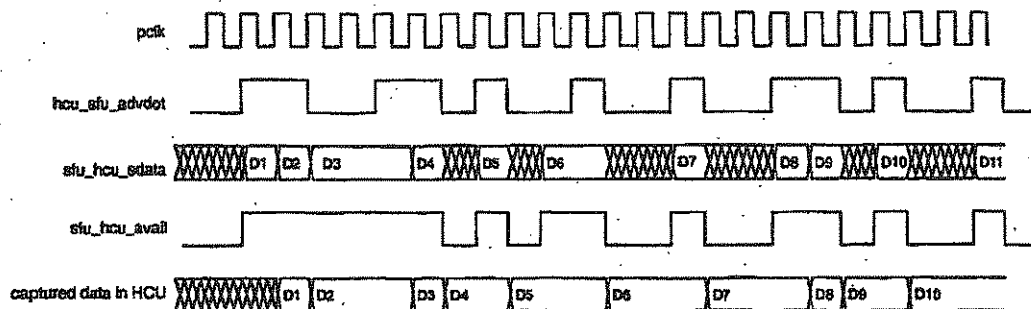


FIG. 249

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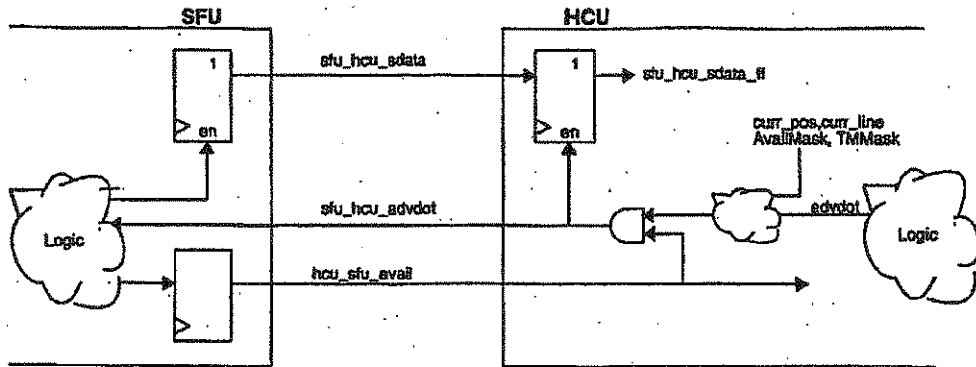


FIG. 250

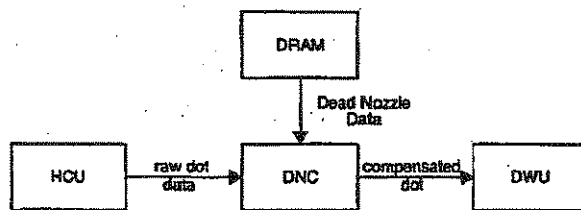


FIG. 251

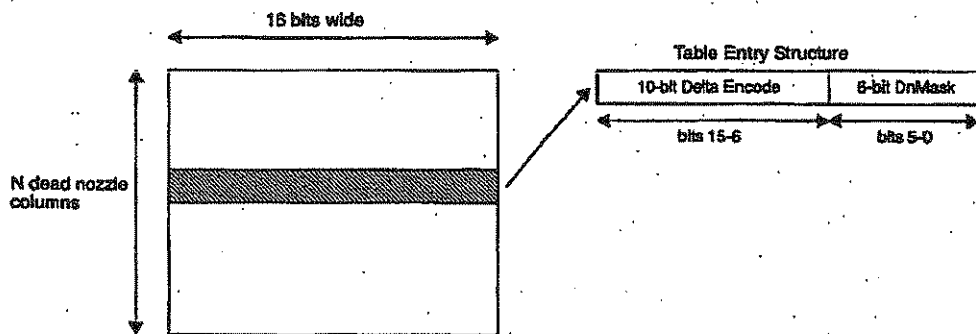


FIG. 252

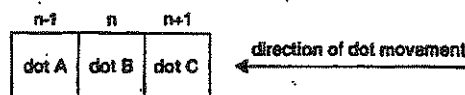


FIG. 253

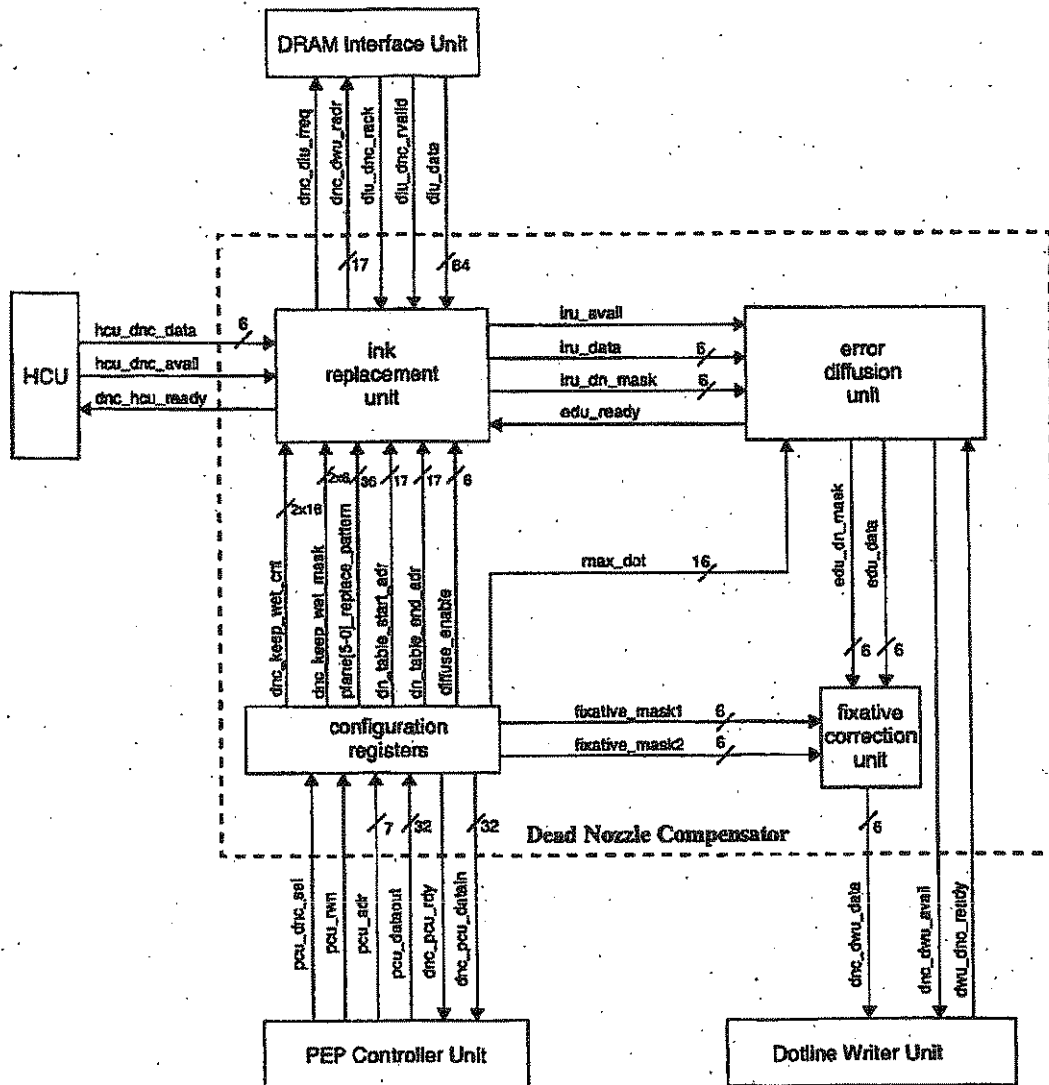


FIG. 254

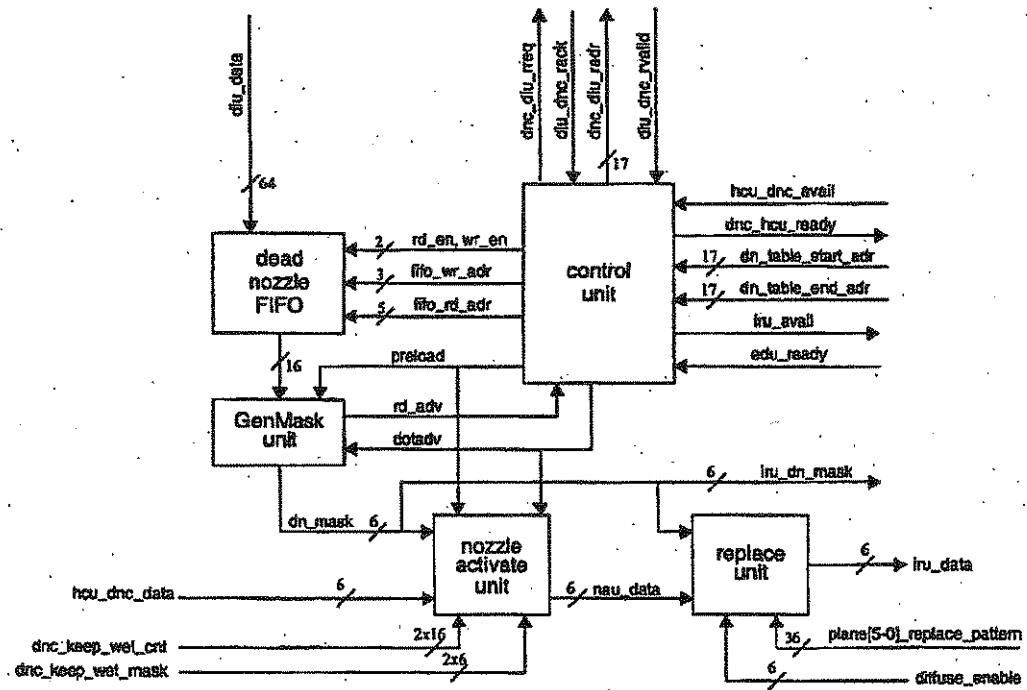


FIG. 255

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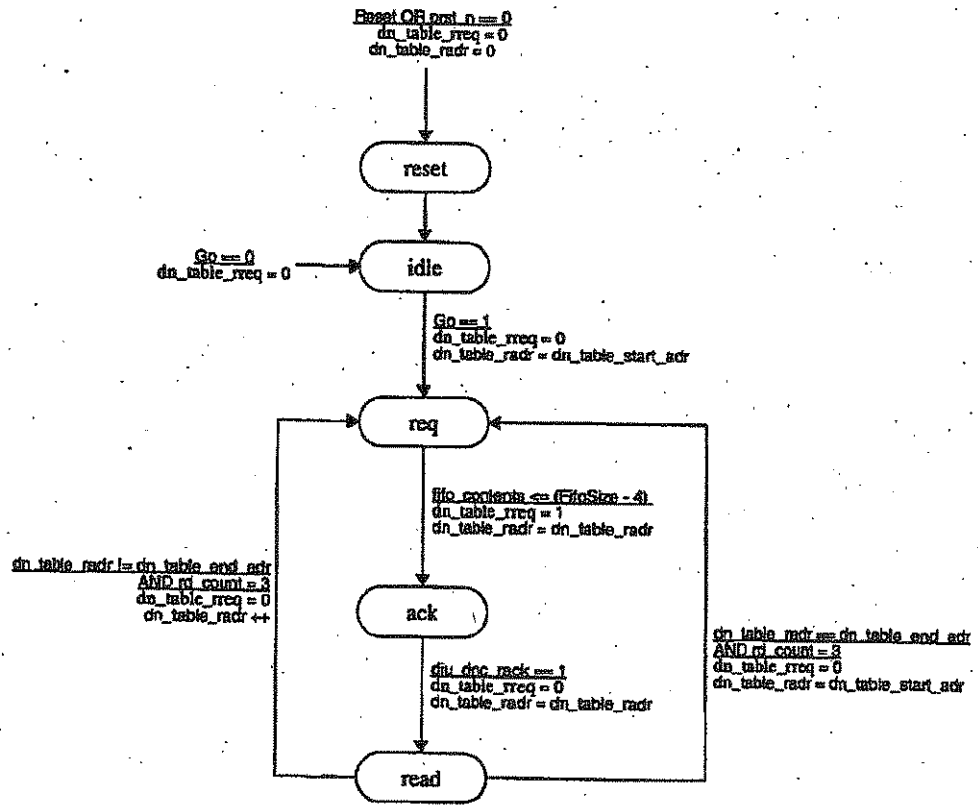


FIG. 256

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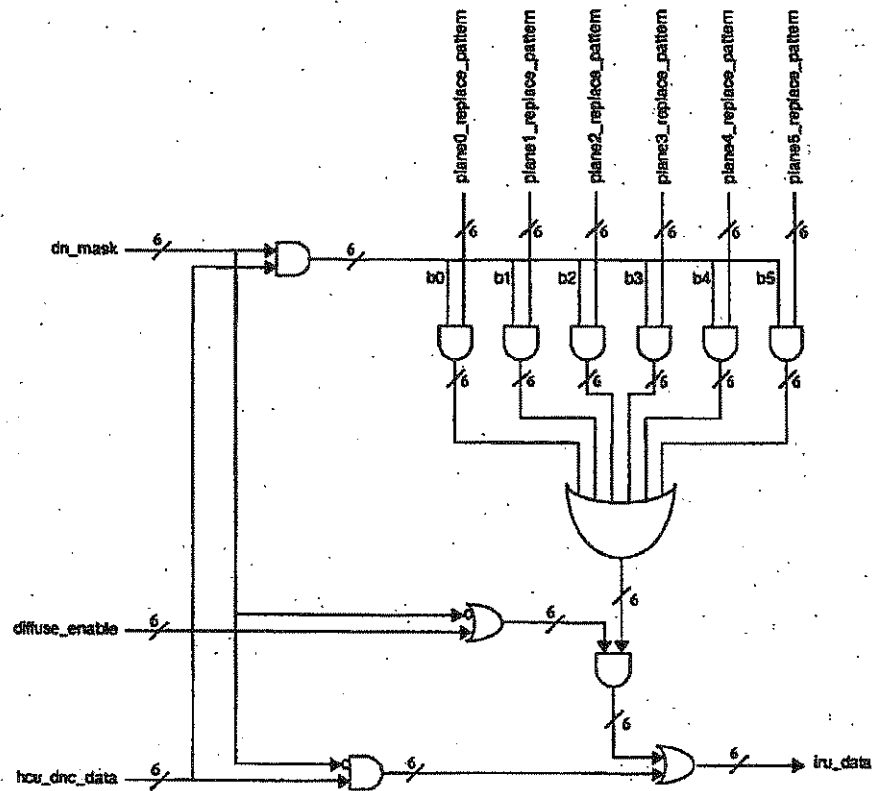


FIG. 257

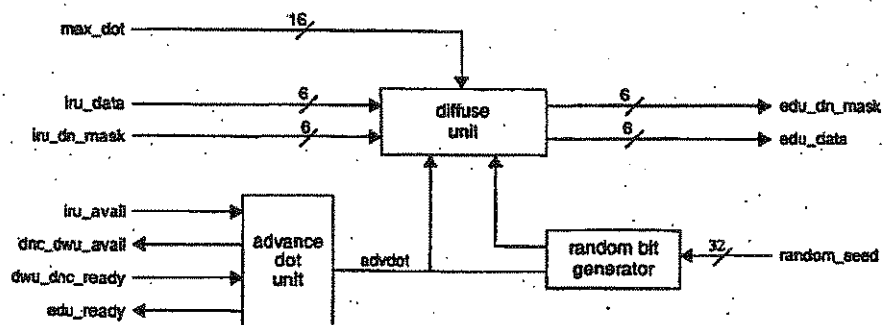


FIG. 258

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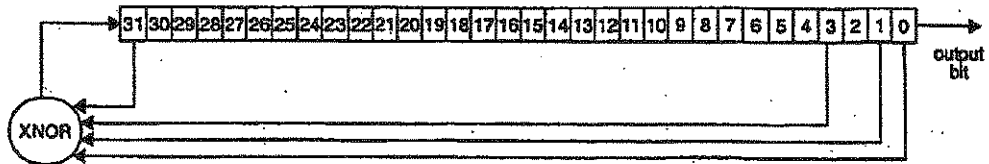


FIG. 259

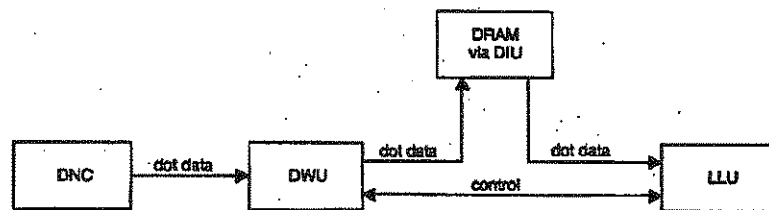
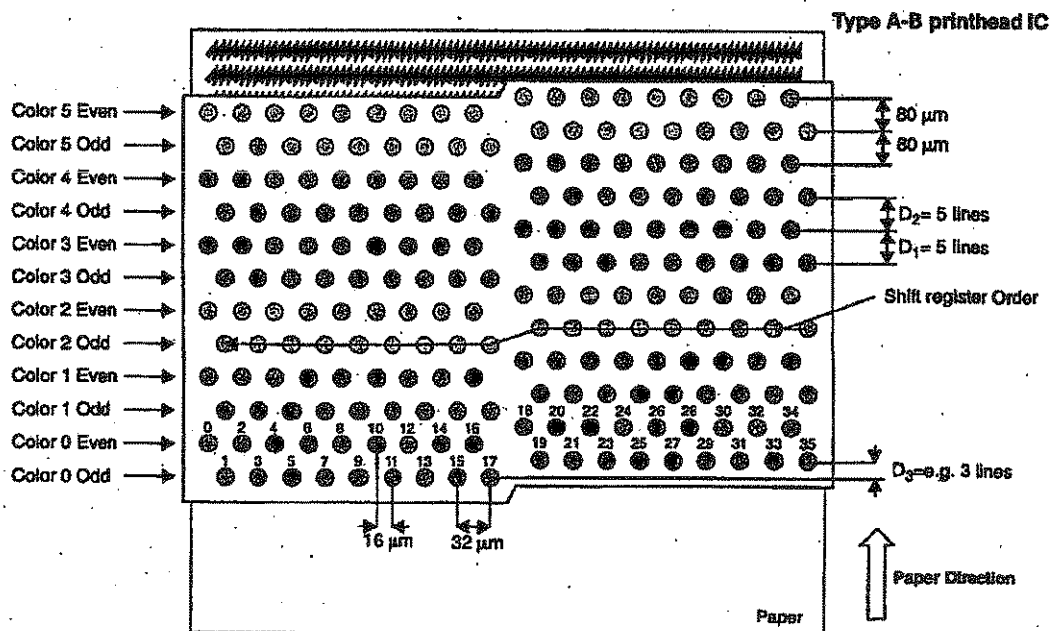


FIG. 260



Note: Paper passes under printhead

FIG. 261

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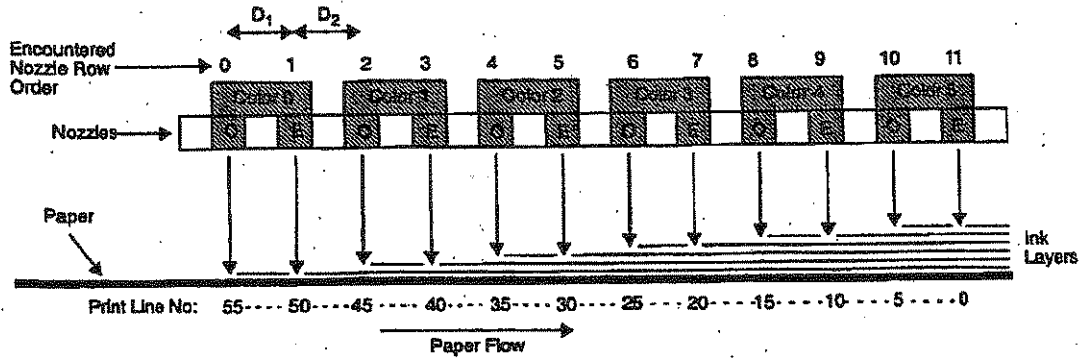


FIG. 262

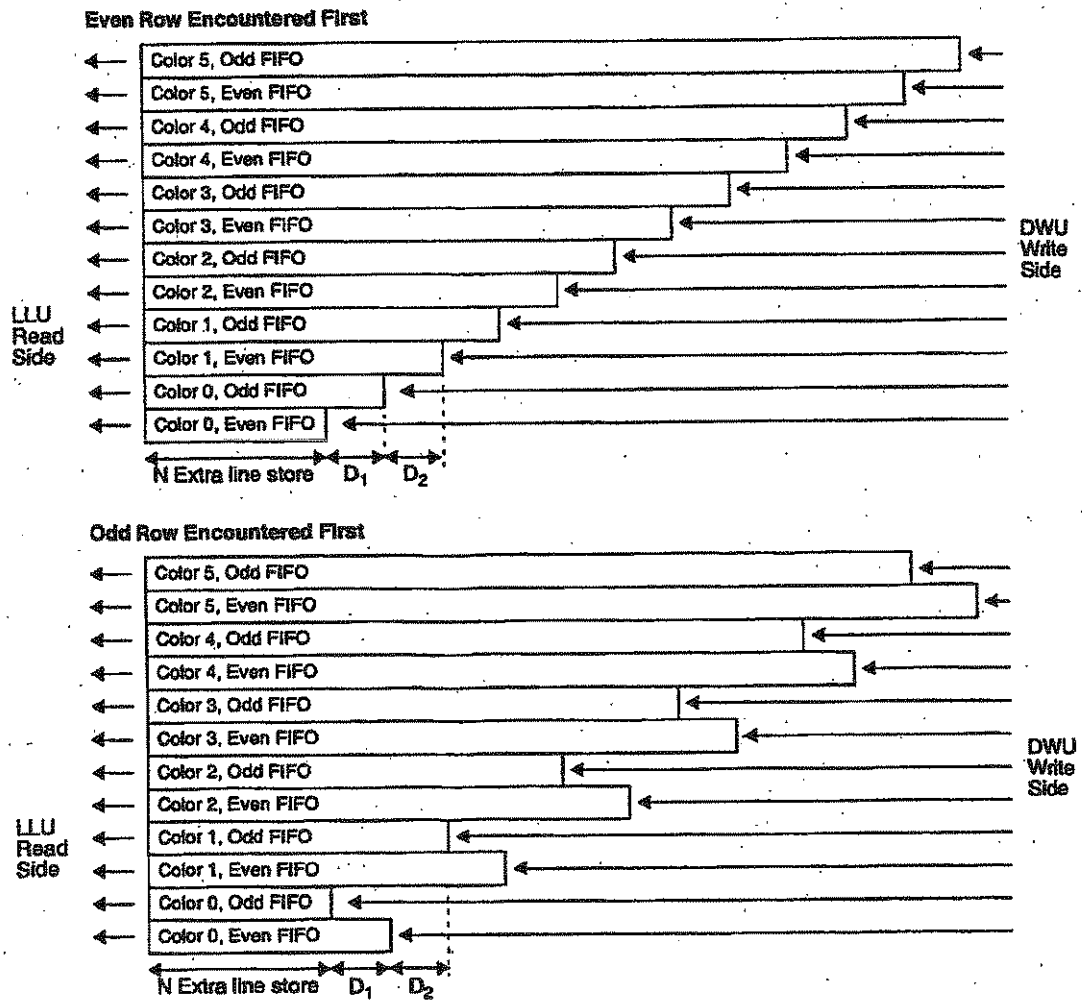


FIG. 263

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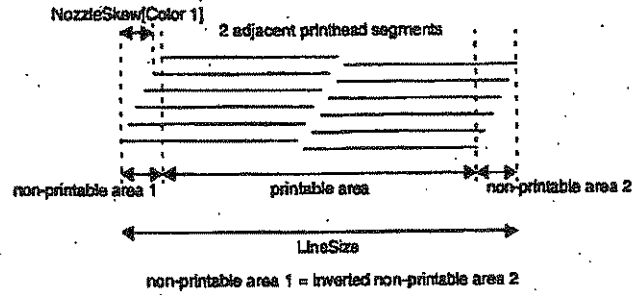


FIG. 264

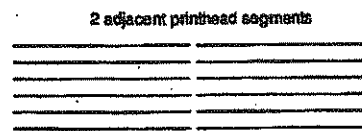


FIG. 265

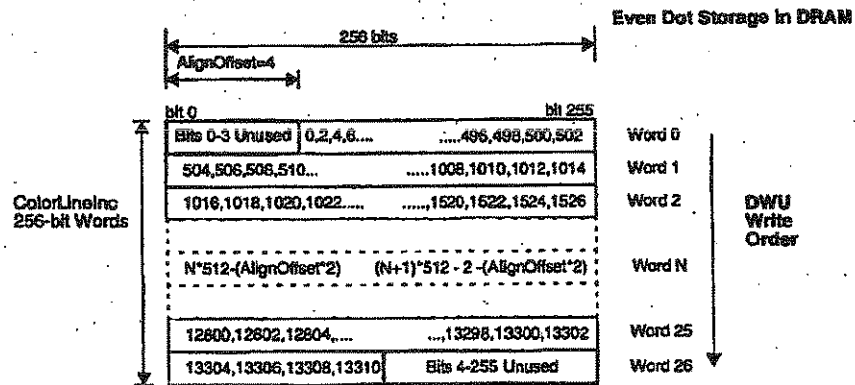


FIG. 266

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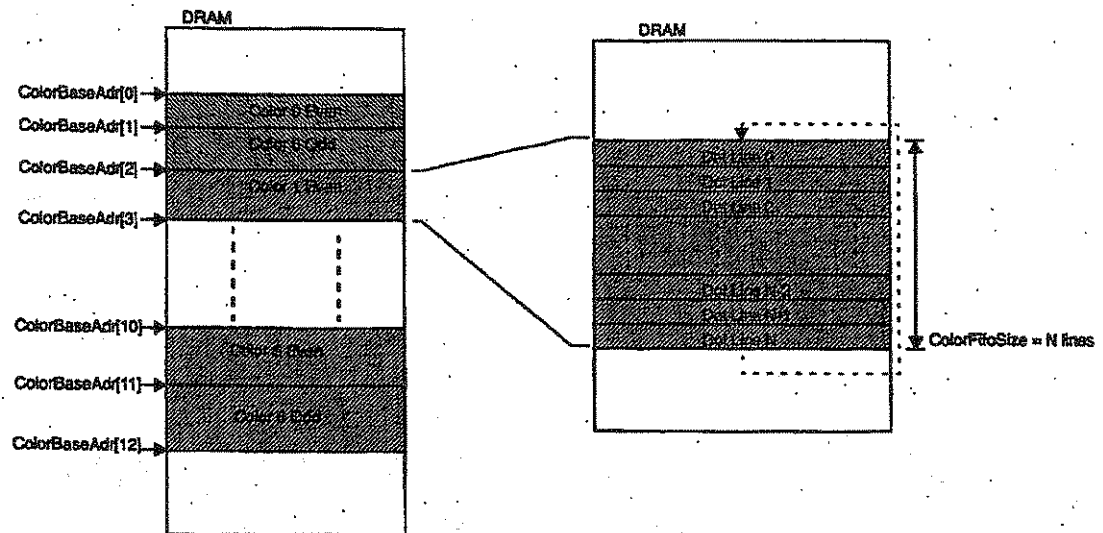


FIG. 267

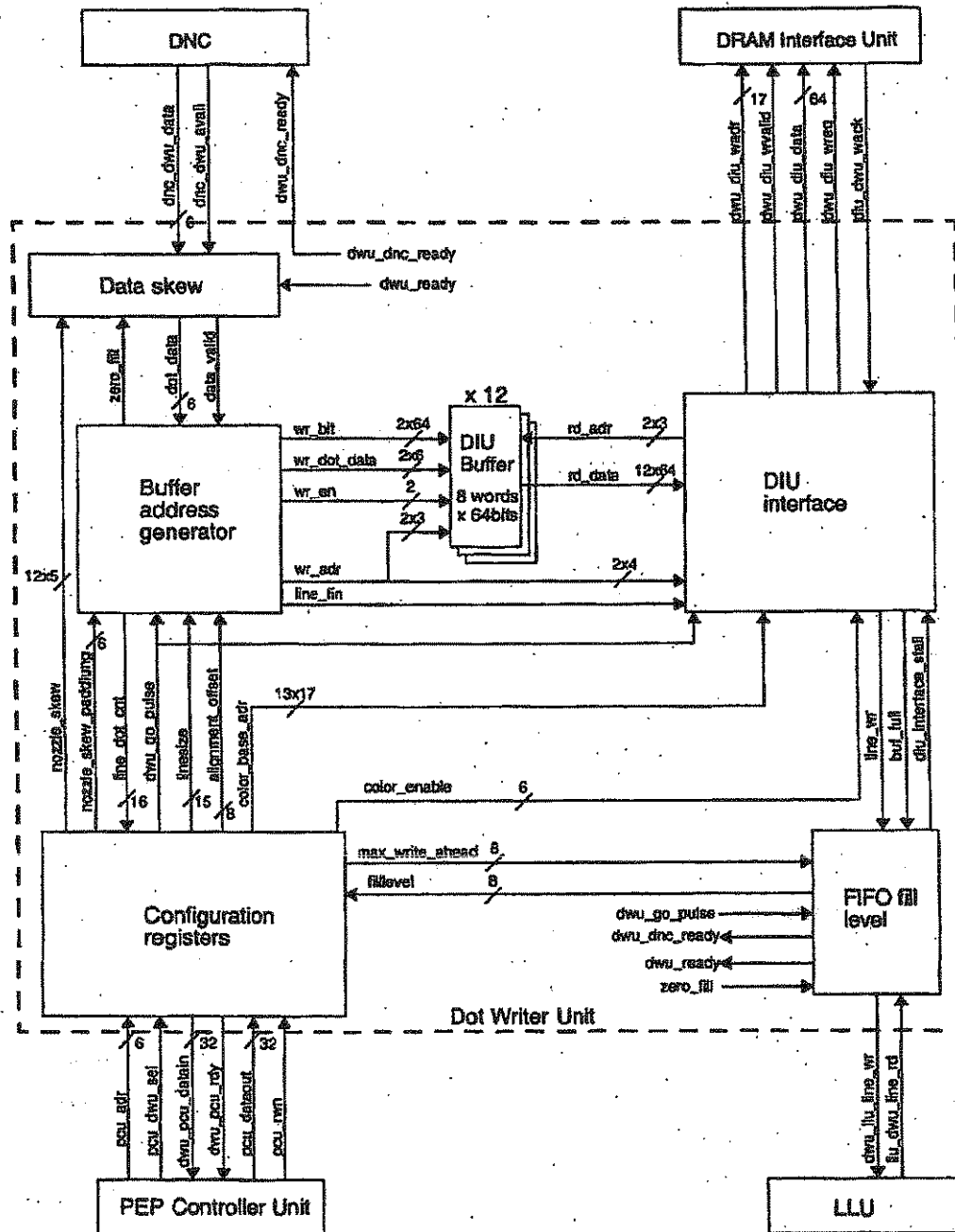


FIG. 268

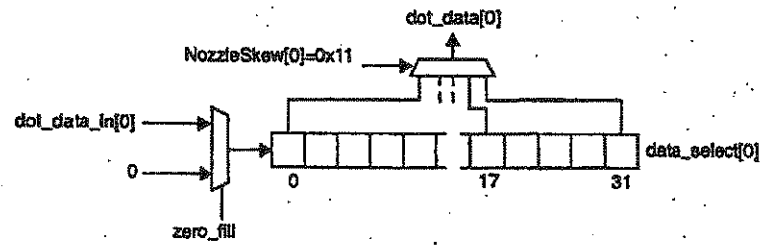


FIG. 269

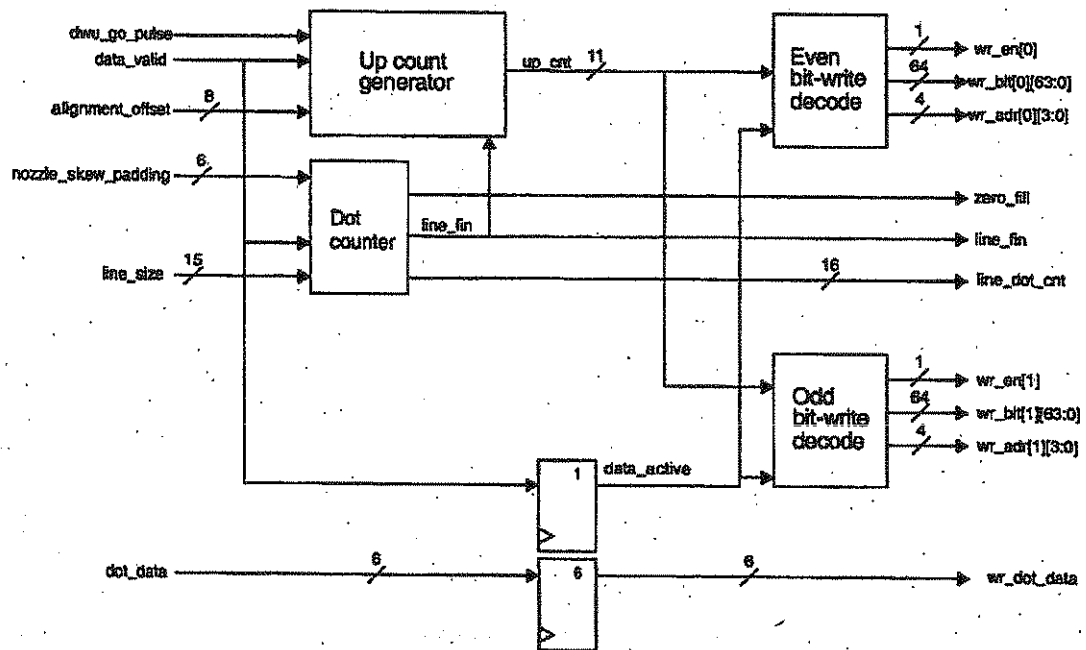


FIG. 270

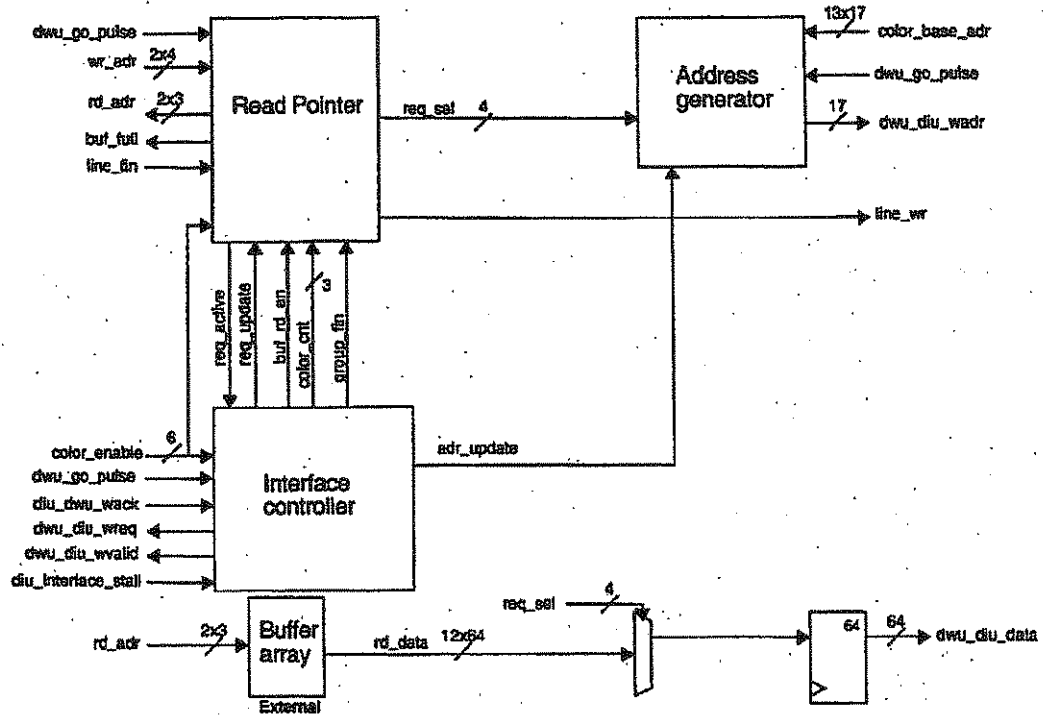


FIG. 271

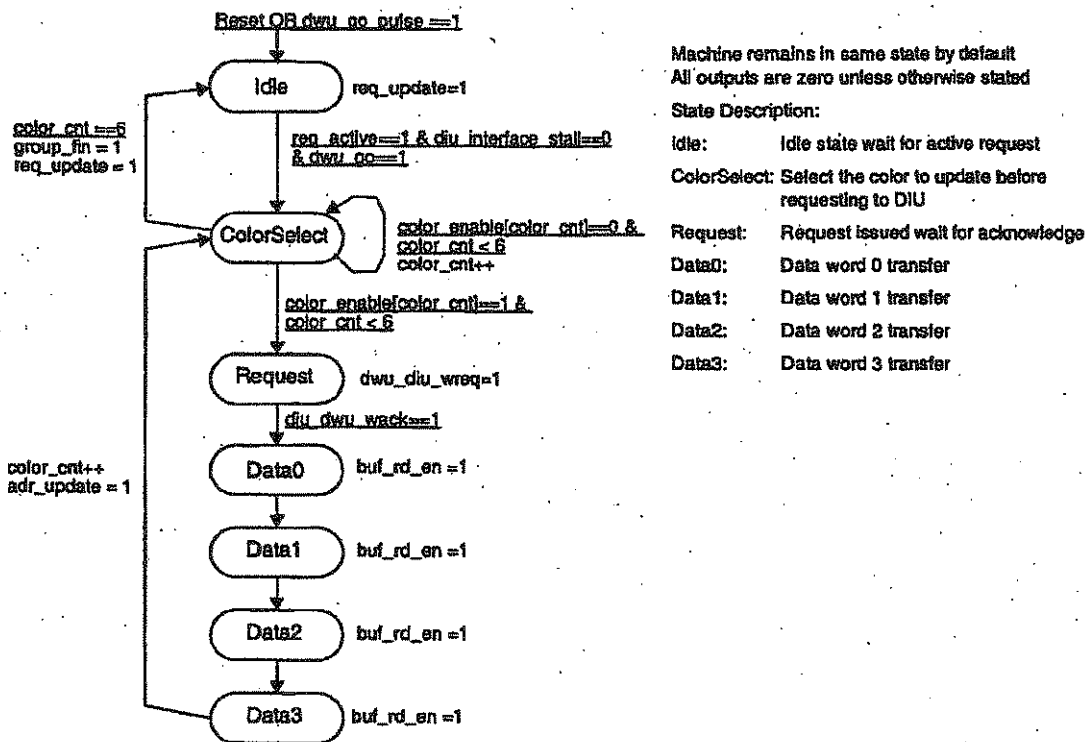


FIG. 272

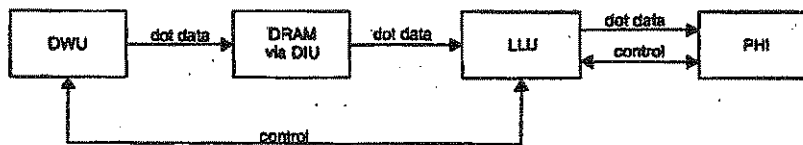


FIG. 273

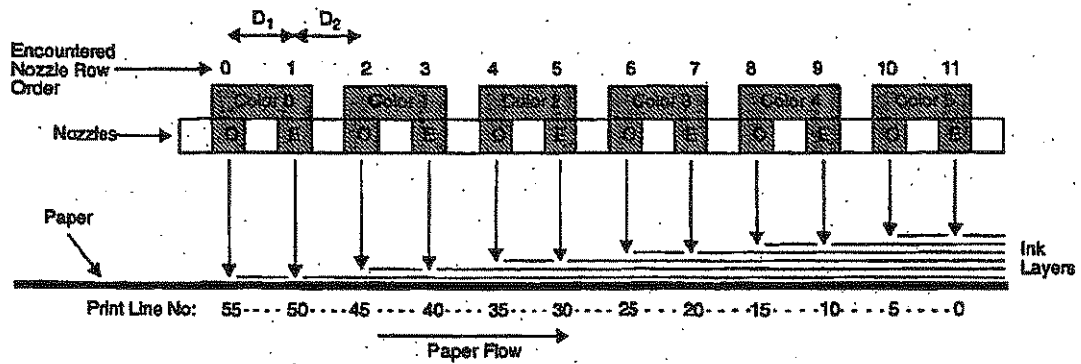


FIG. 274

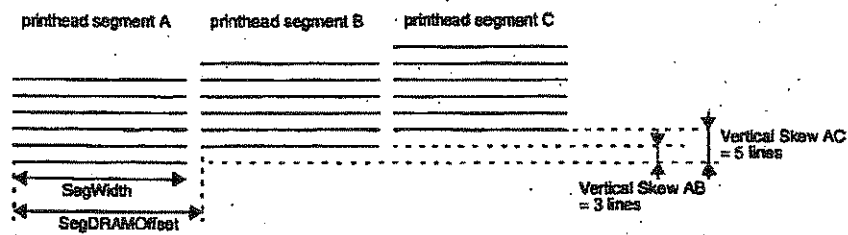


FIG. 275

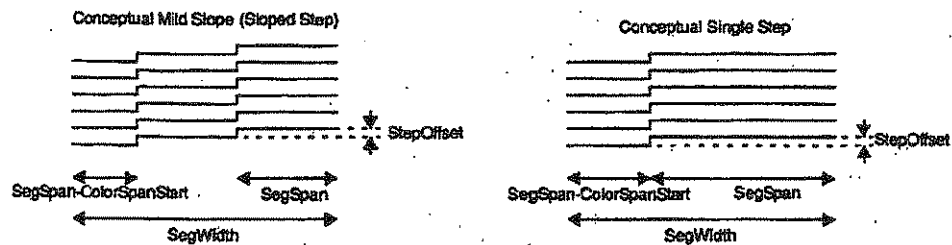


FIG. 276

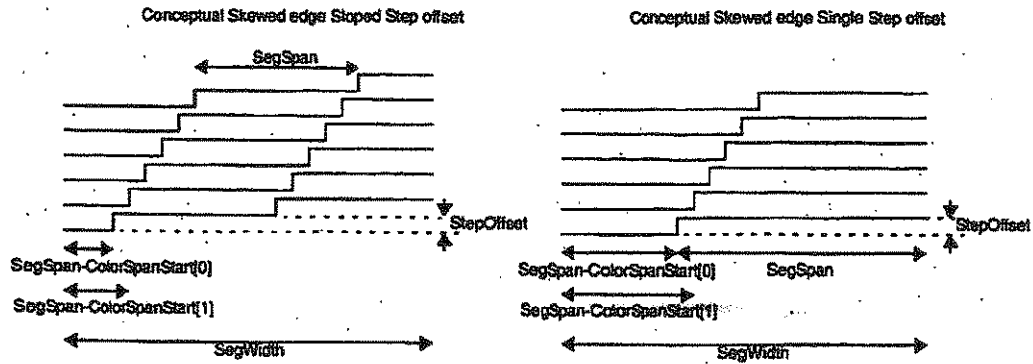


FIG. 277

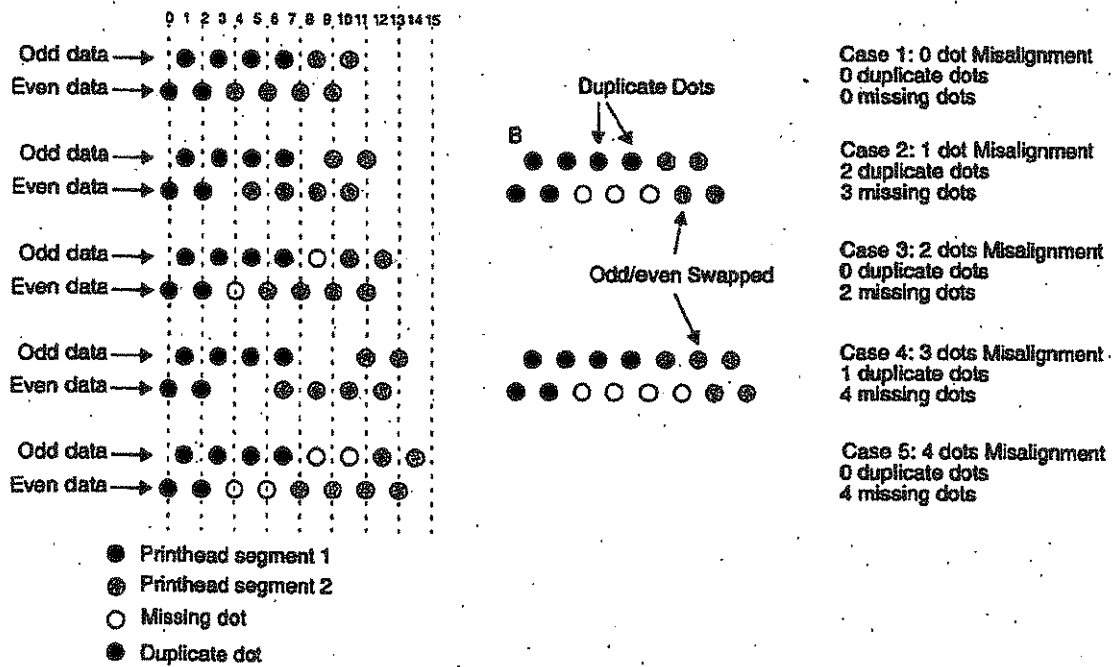


FIG. 278

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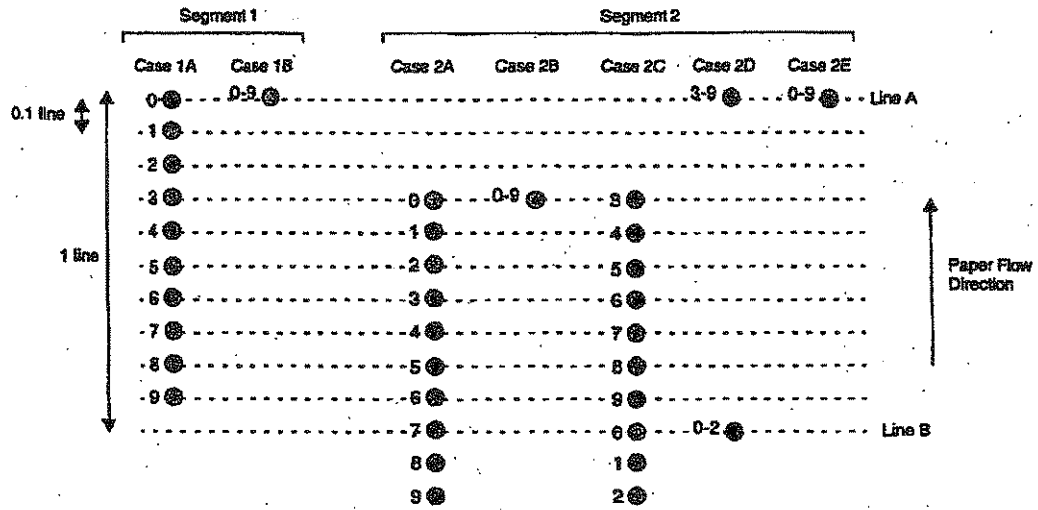


FIG. 279

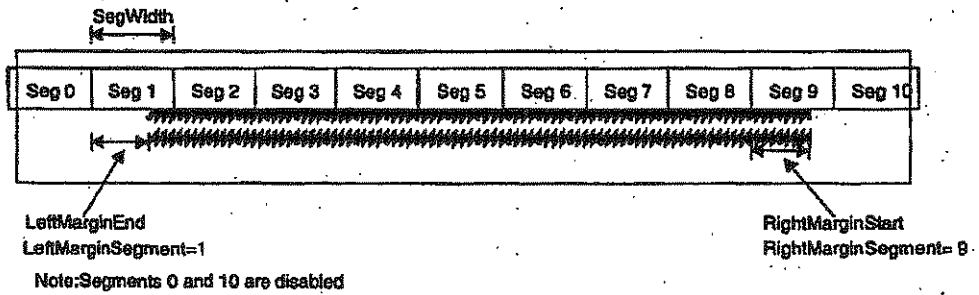


FIG. 280

Generate dot order (to the PHI)

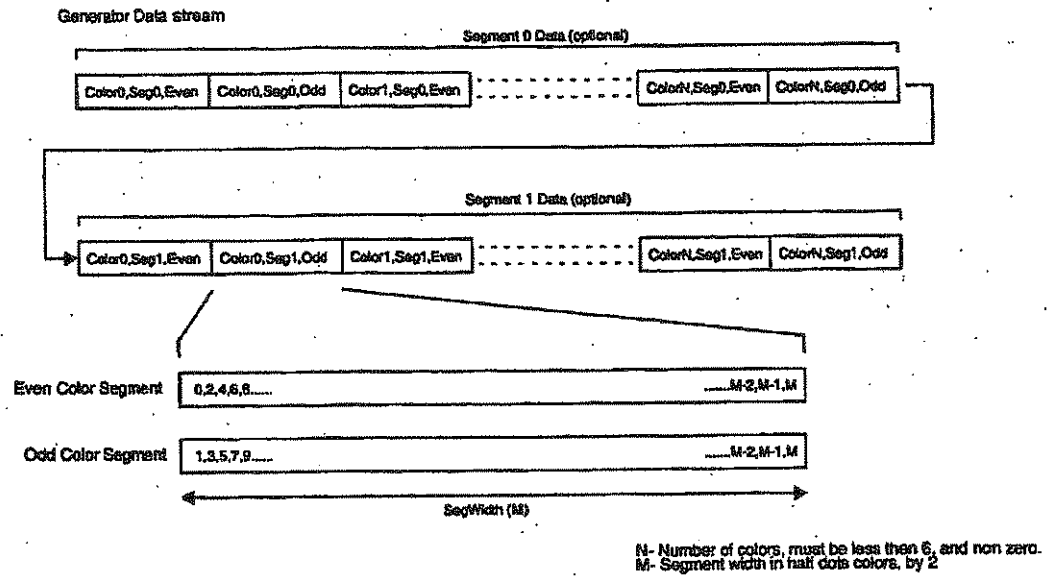


FIG. 281

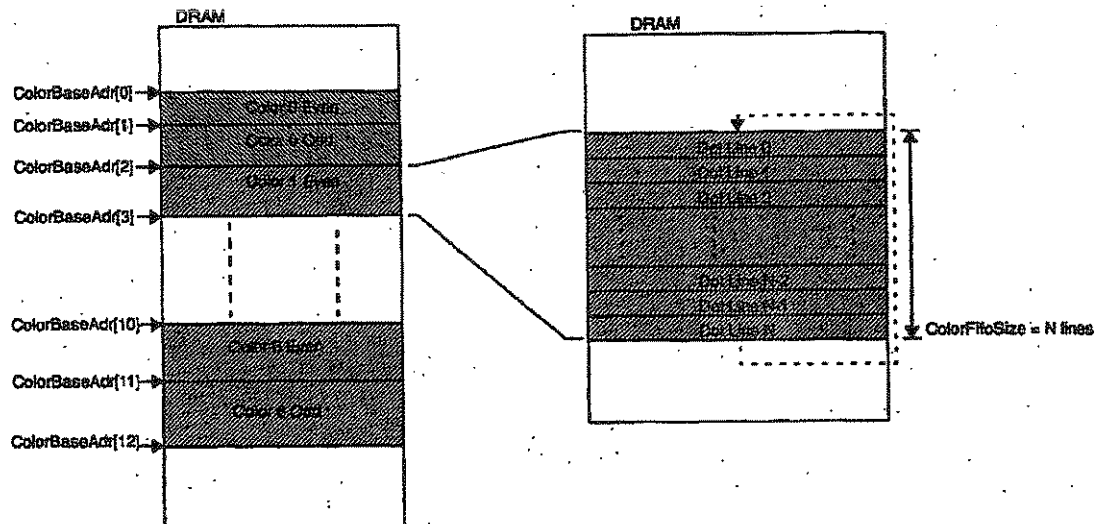


FIG. 282

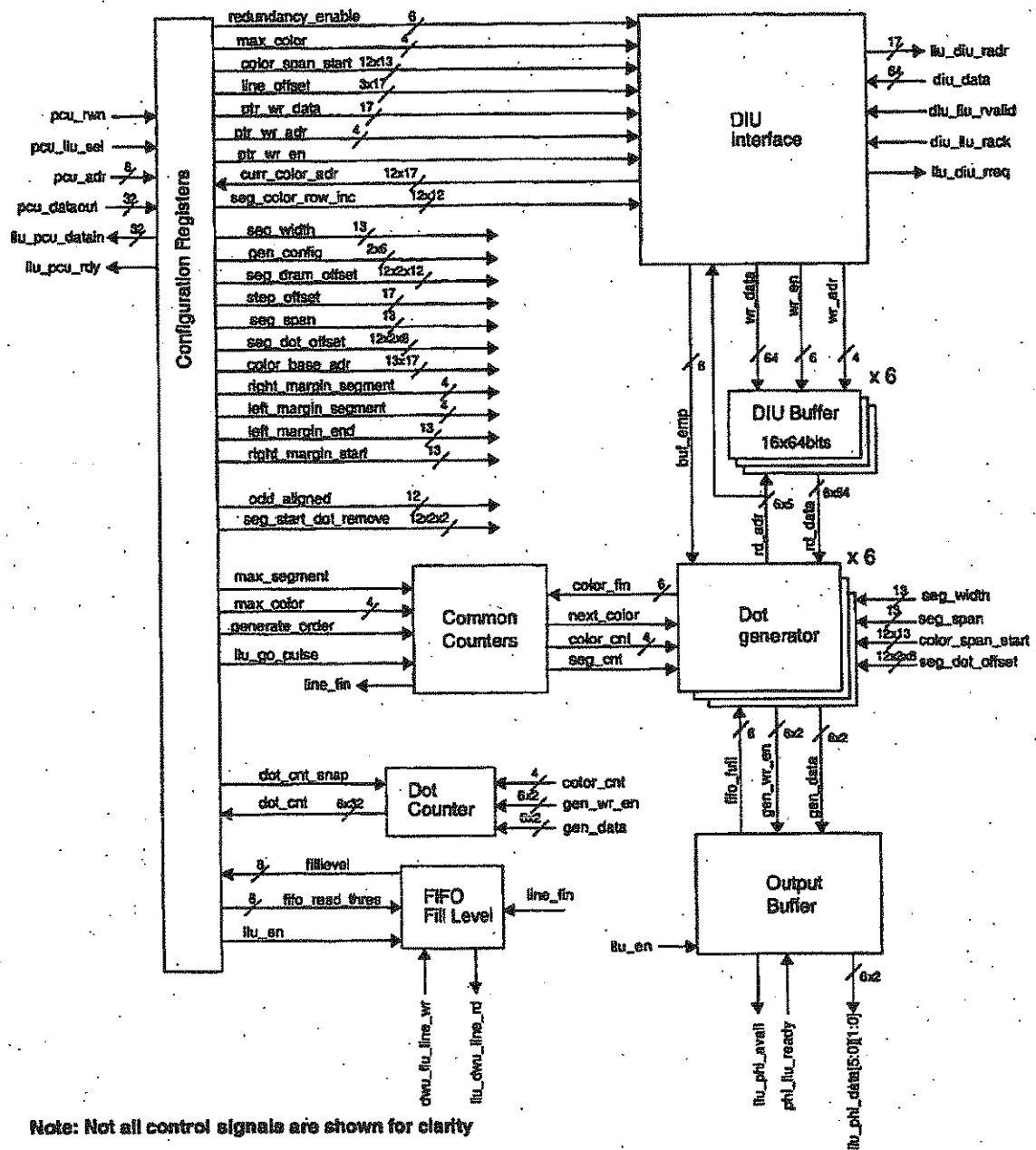


FIG. 283

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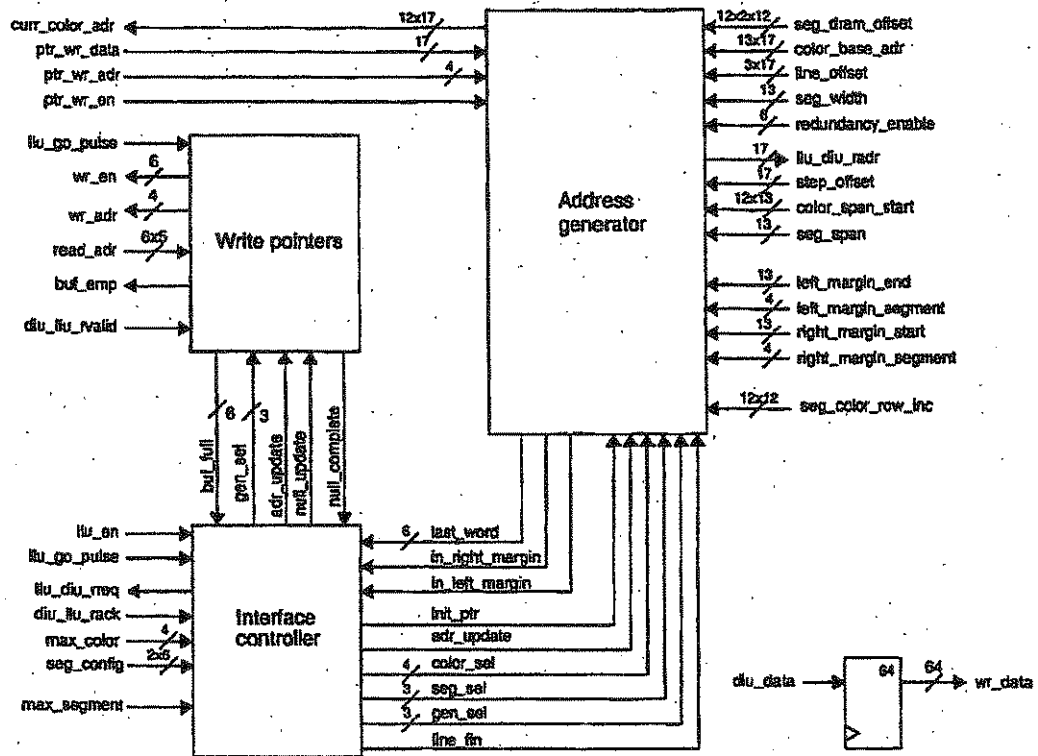
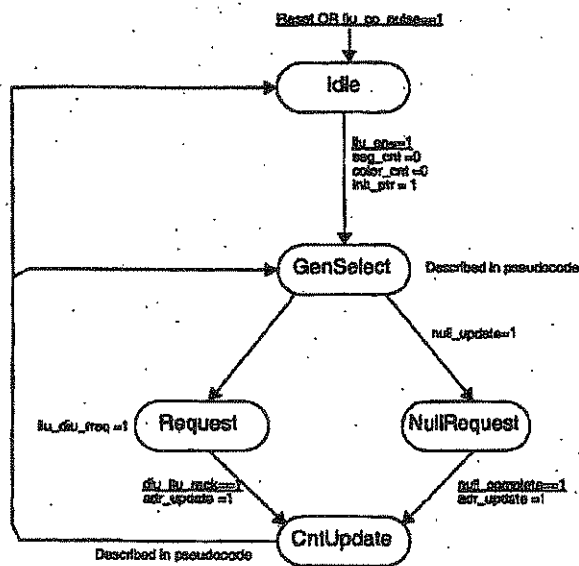


FIG. 284



Machine remains in same state by default
All outputs are zero unless otherwise stated

State Description:

- Idle:** Idle state wait for active request
- GenSelect:** Select the correct generator to update before requesting to DIU
- Request:** Request issued wait for acknowledge
- NullRequest:** Request that buffer be filled with null data, wait for completion
- CntUpdate:** Update the address pointers

FIG. 285

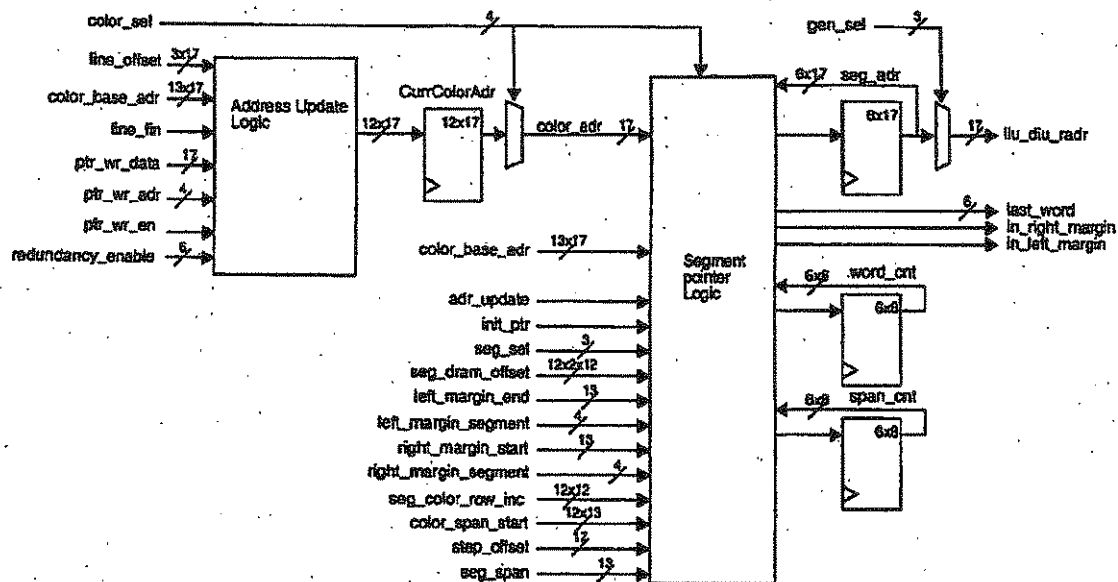


FIG. 286

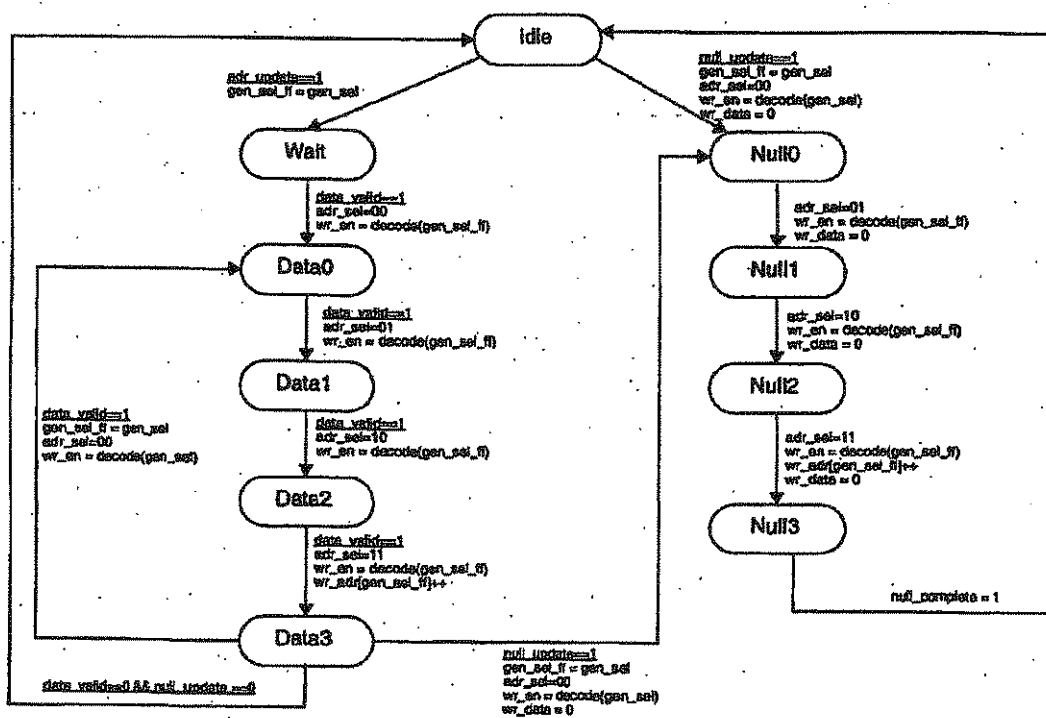


FIG. 287

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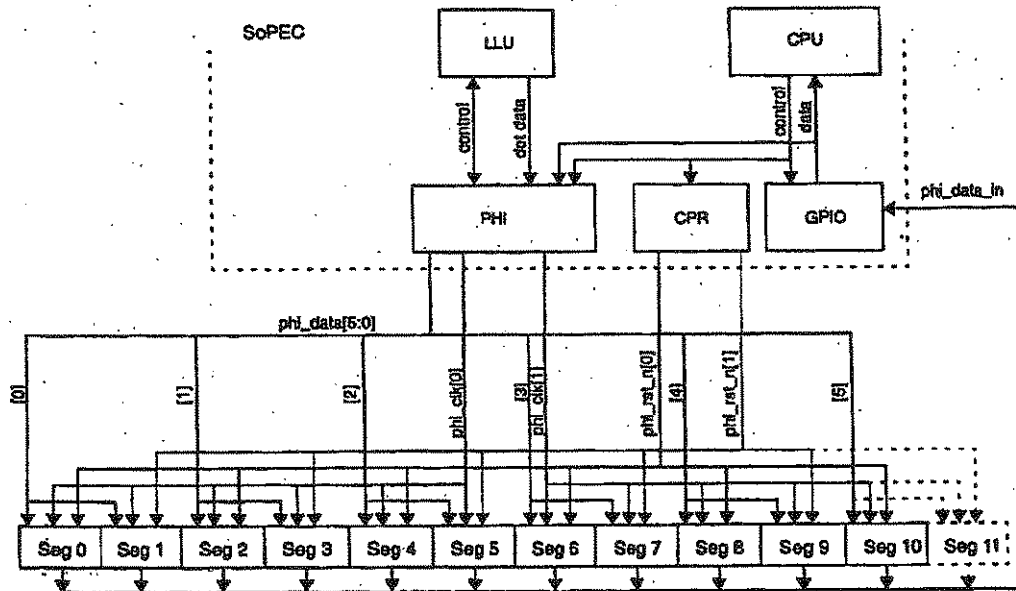


FIG. 288

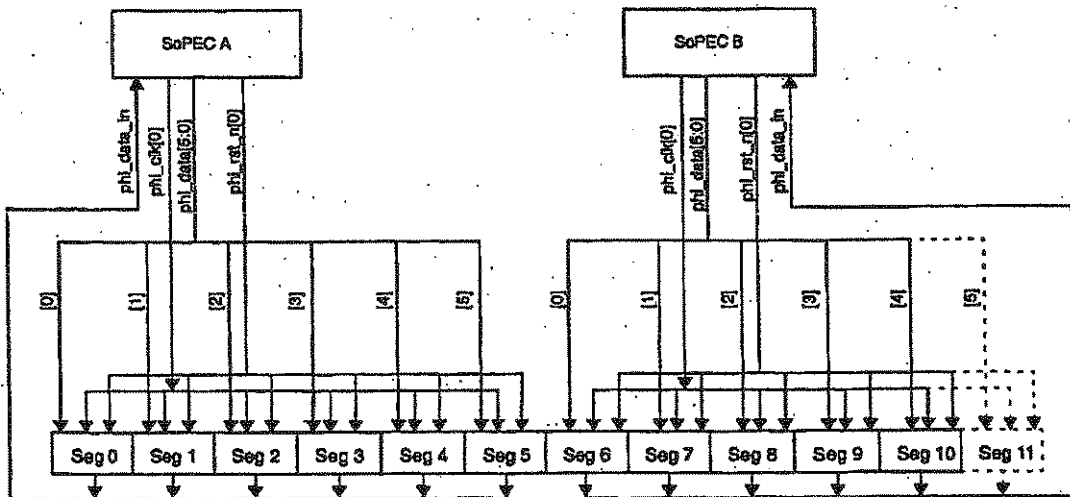


FIG. 289

15	14	13	12	9	8	0
Unused	EOC	Seg Address			Control or Data Symbol	

FIG. 290

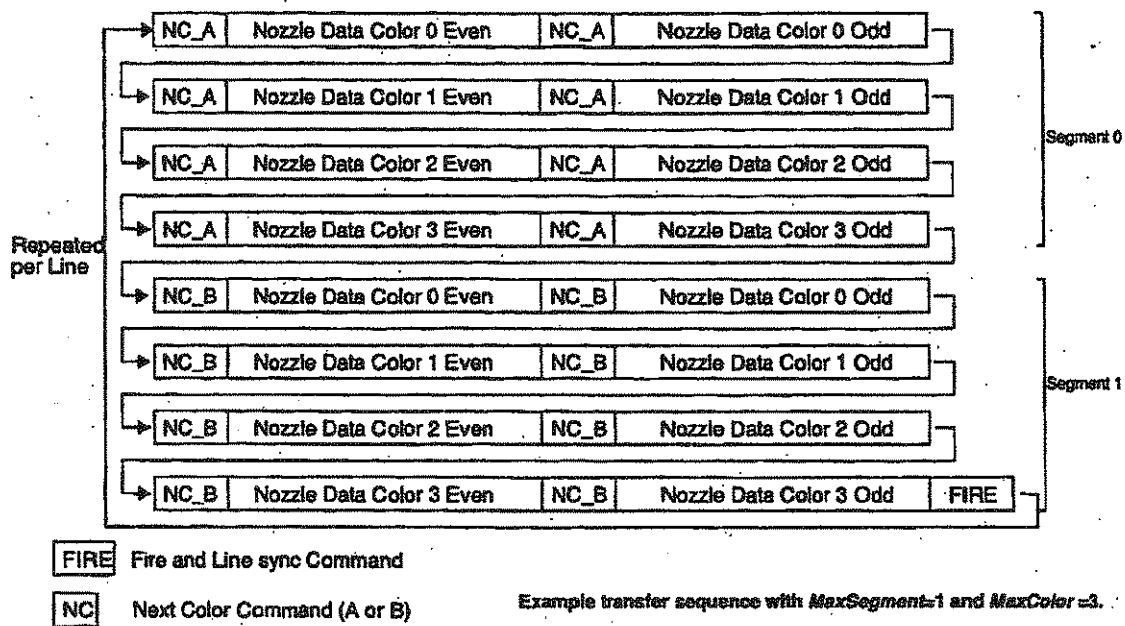


FIG. 291

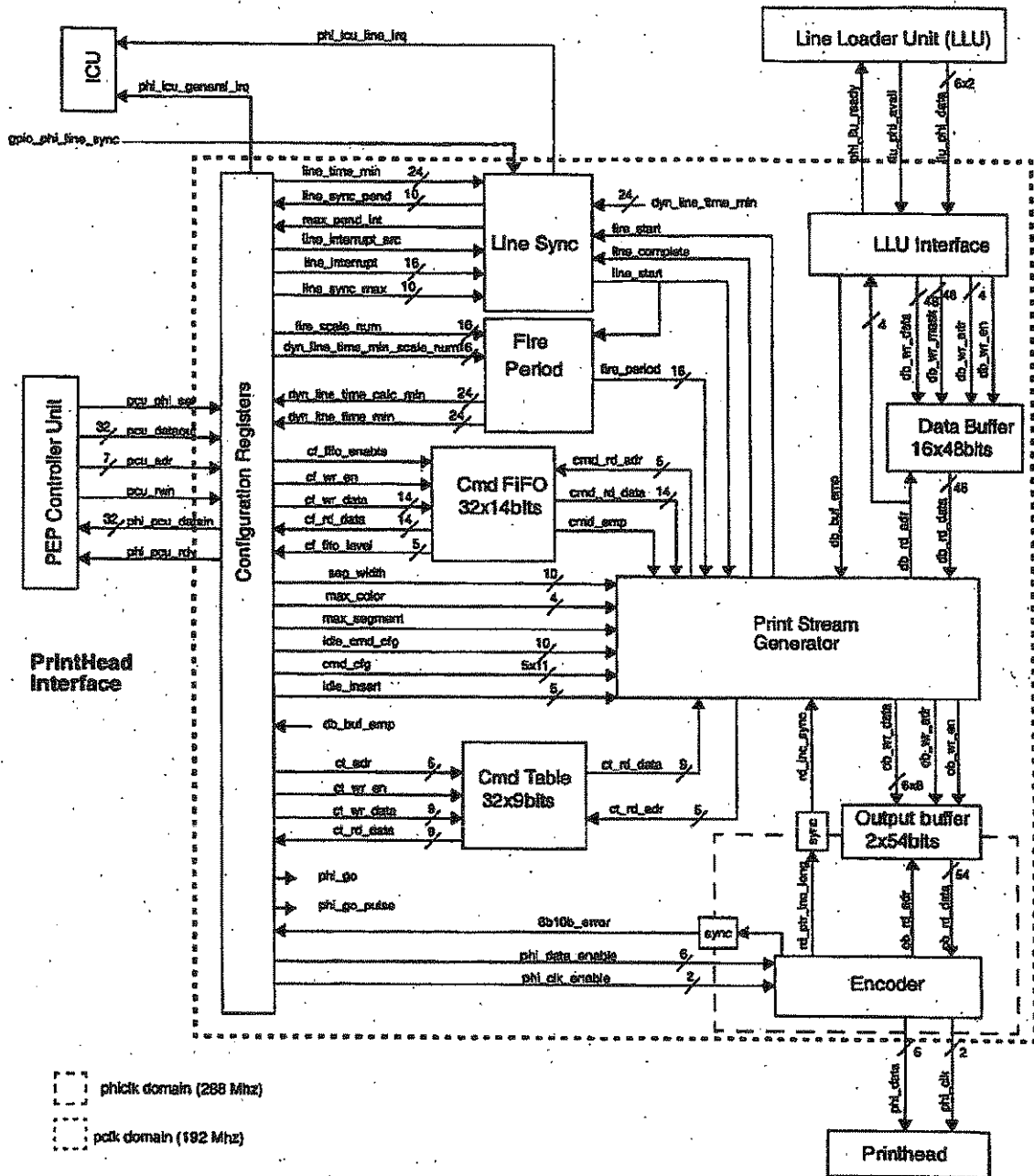


FIG. 292

Machine remains in same state by default
All outputs are zero unless otherwise stated

State Description:

Wait: Wait for line start

NCCmd: Generate NC_A/B (next color) command

NozzleData: Transmit Nozzle Data

Fire: Generate Fire command

IdleInsert: Insert idle characters

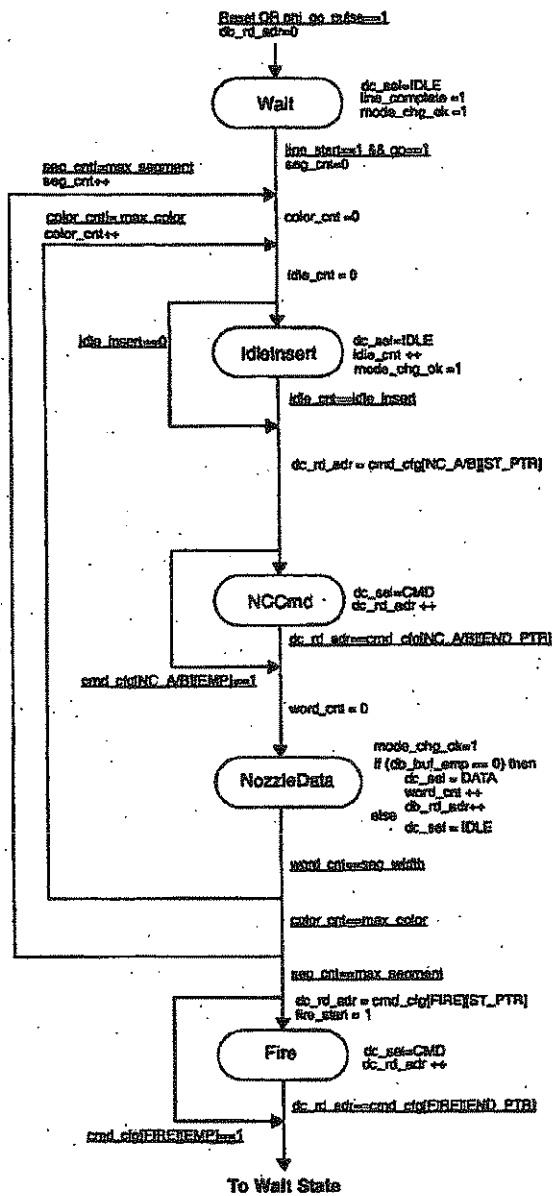


FIG. 293

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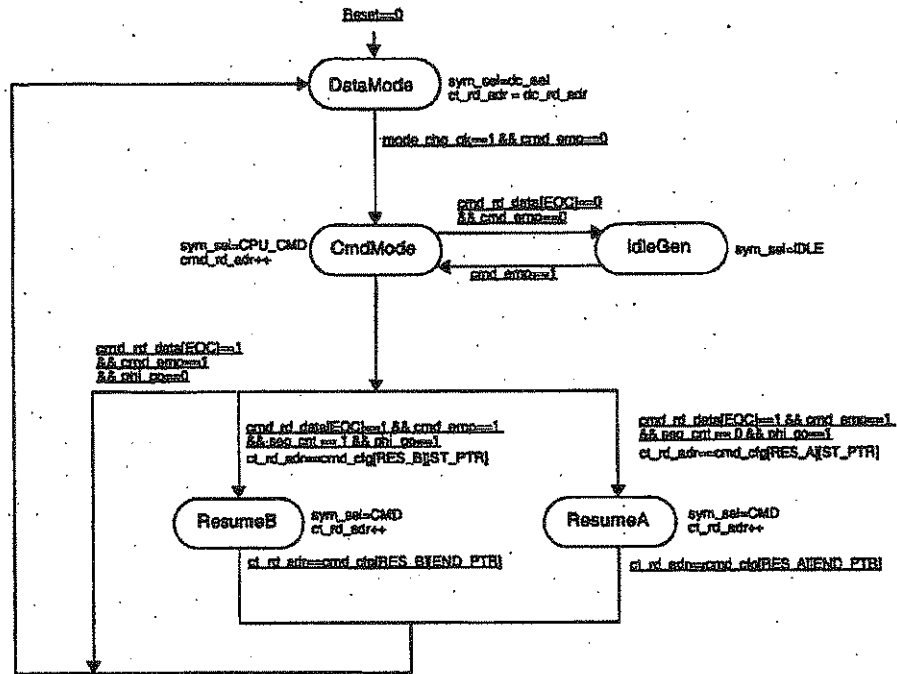
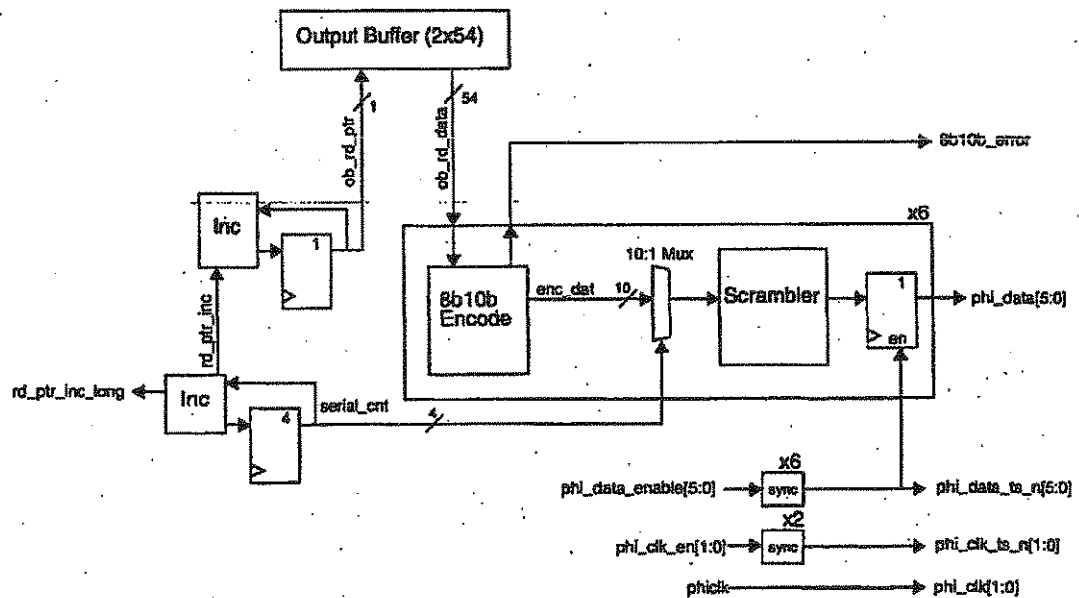


FIG. 294



Note: All logic clocked on phiclk

FIG. 295

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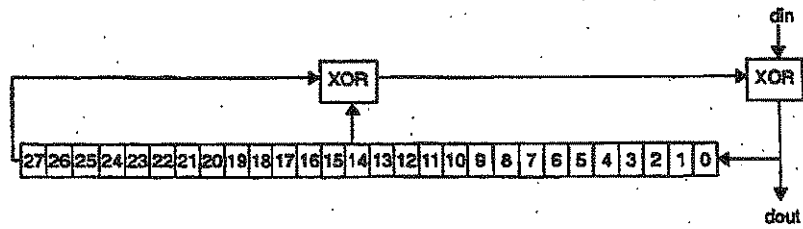


FIG. 296

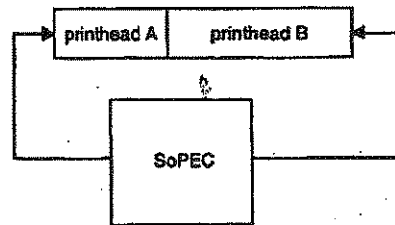


FIG. 297

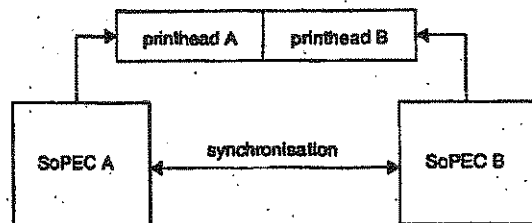


FIG. 298

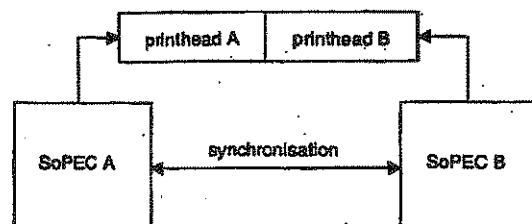


FIG. 299

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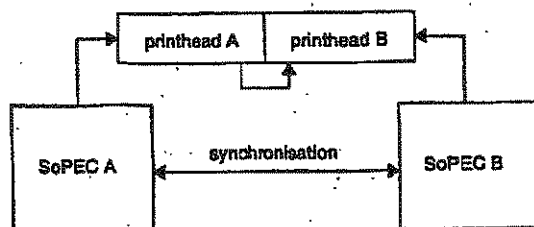


FIG. 300

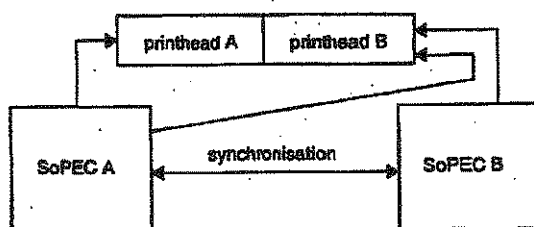


FIG. 301

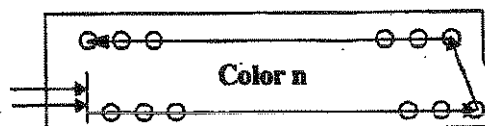


FIG. 302

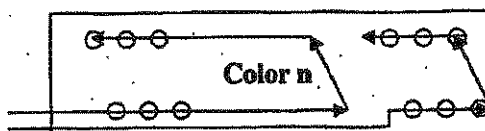


FIG. 303

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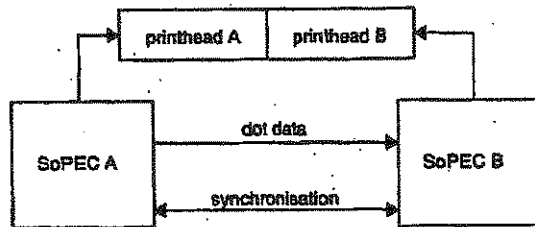


FIG. 304

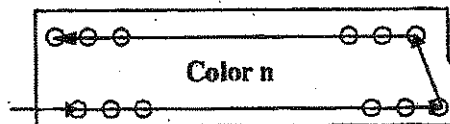


FIG. 305

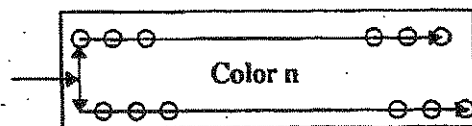


FIG. 306

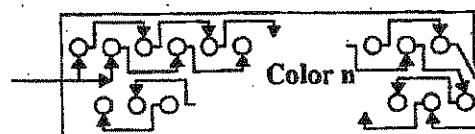


FIG. 307



FIG. 308

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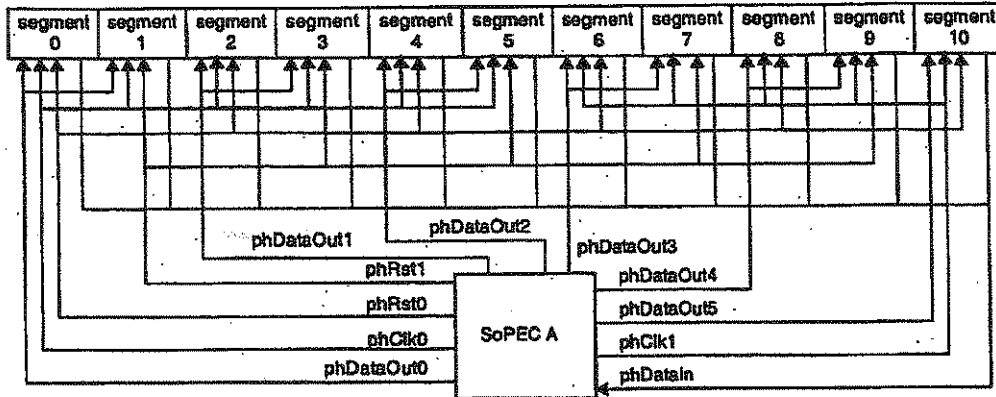


FIG. 309

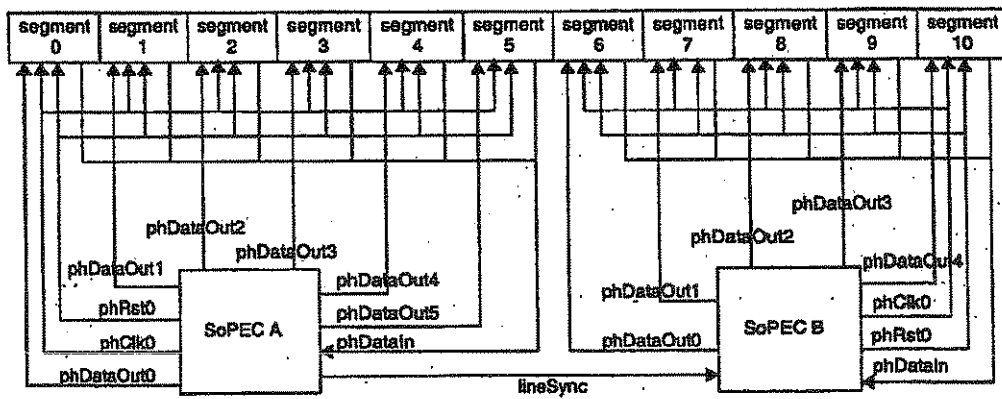


FIG. 310

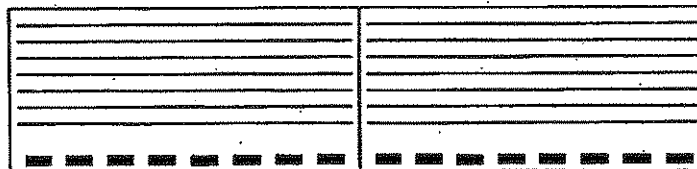


FIG. 311

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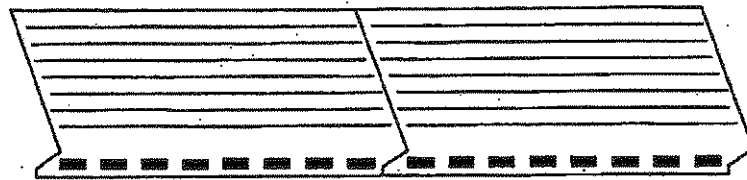


FIG. 312

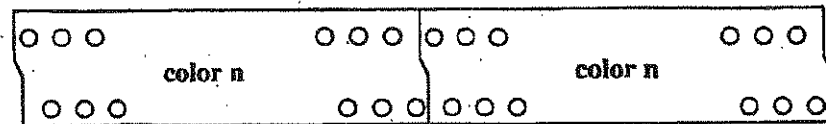


FIG. 313

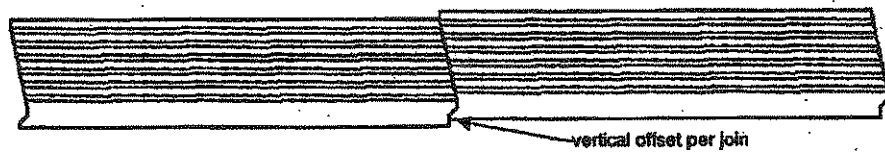


FIG. 314

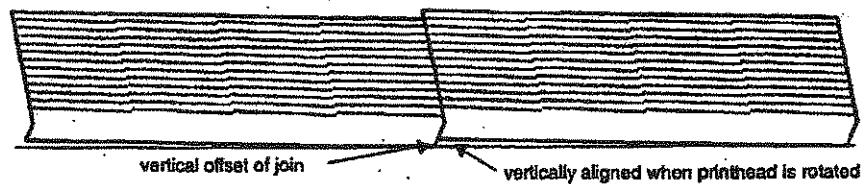


FIG. 315

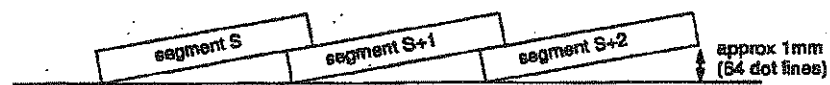


FIG. 316

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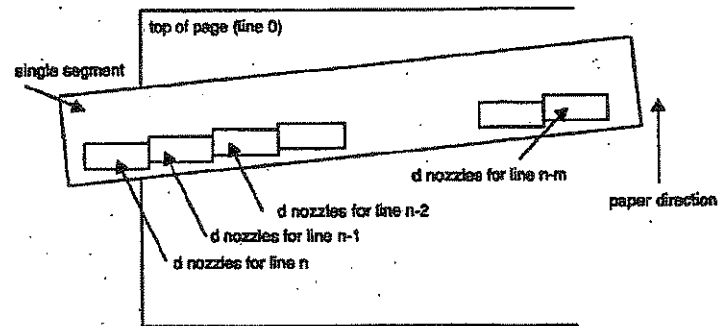


FIG. 317



FIG. 318

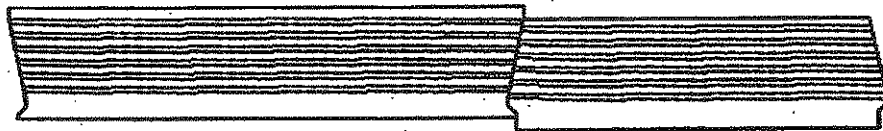


FIG. 319



FIG. 320



FIG. 321

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FIG. 322

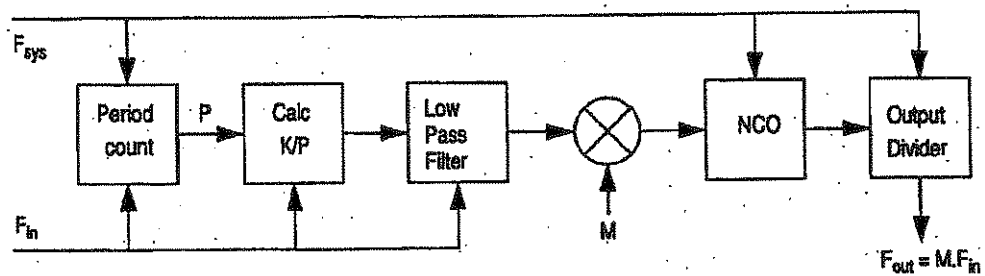


FIG. 323

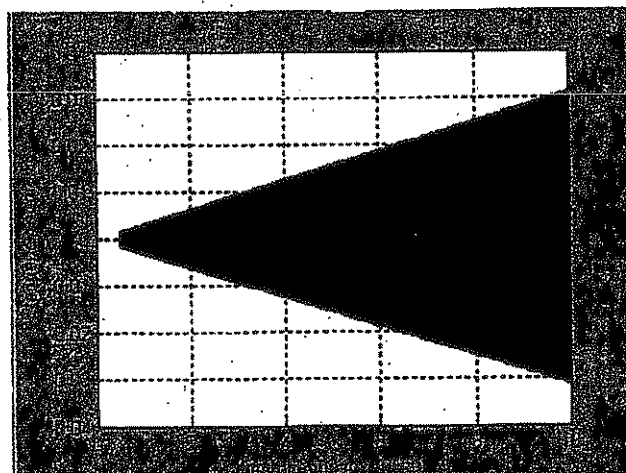


FIG. 324

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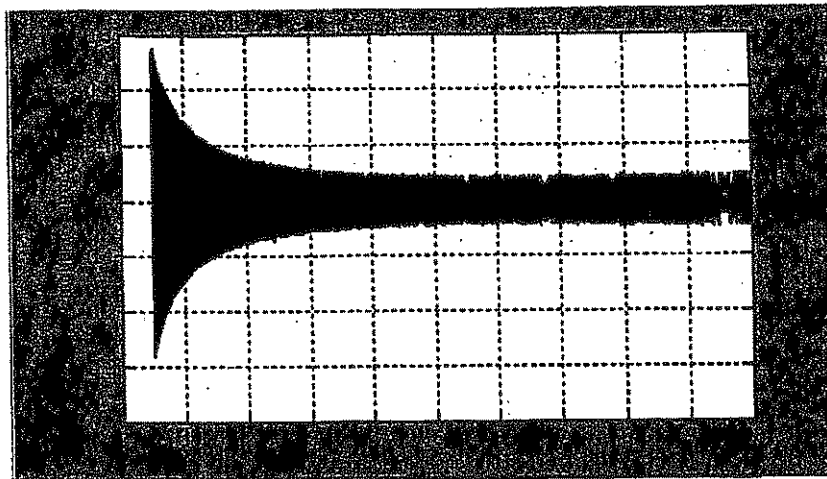


FIG. 325

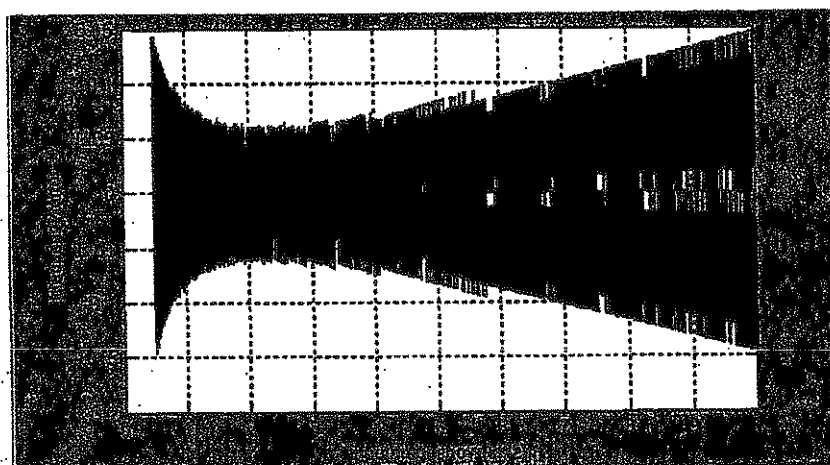


FIG. 326

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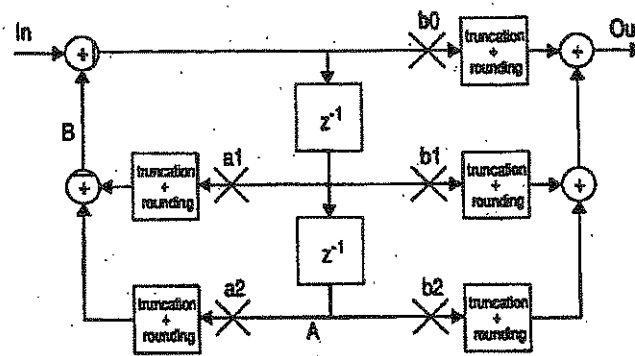


FIG. 327

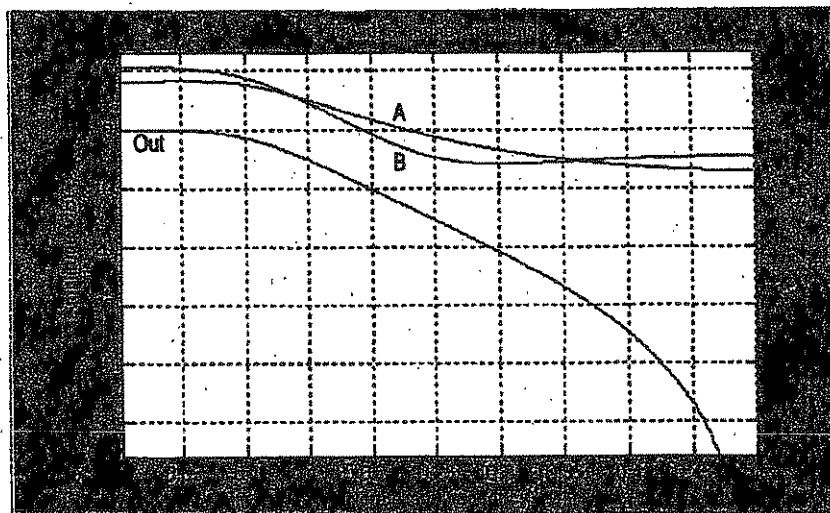


FIG. 328

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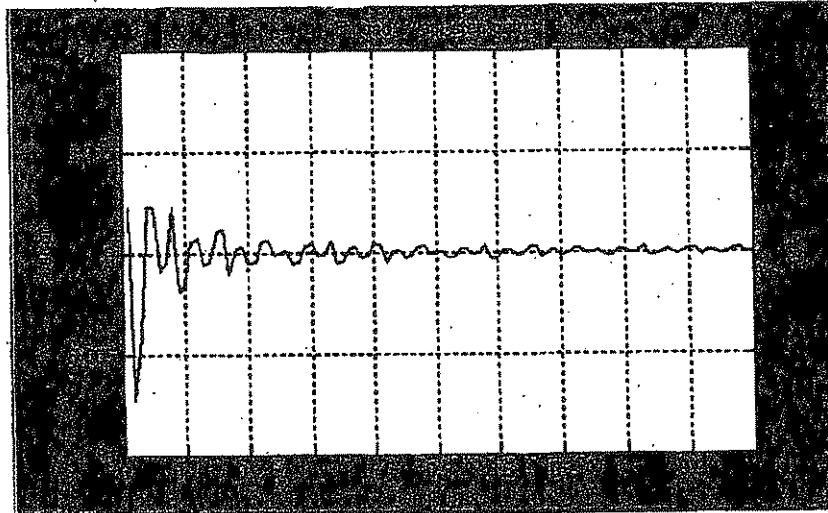


FIG. 329

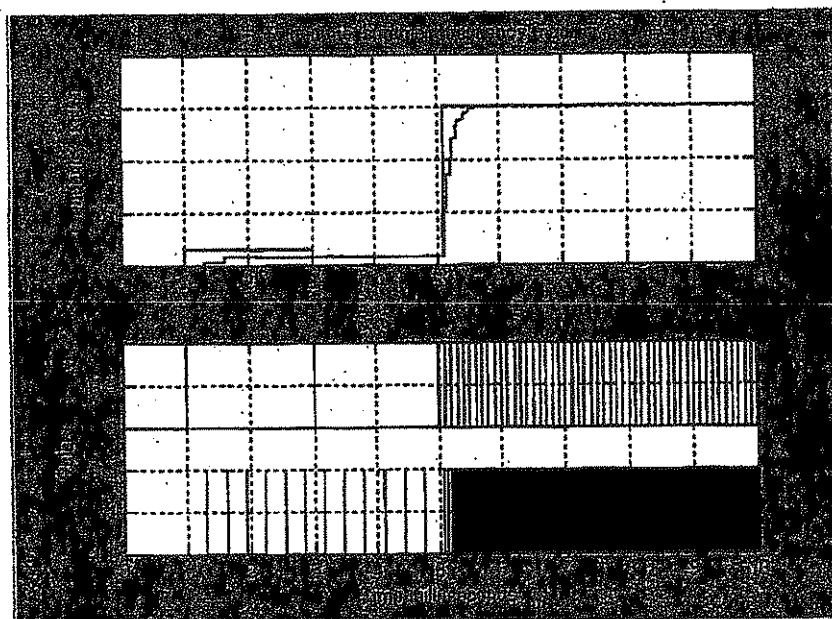


FIG. 330

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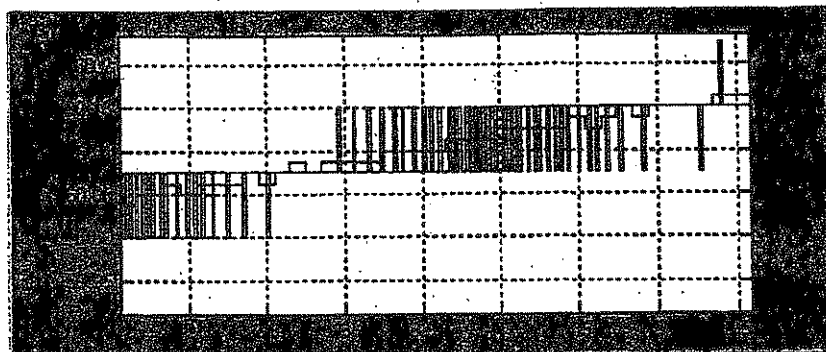


FIG. 331

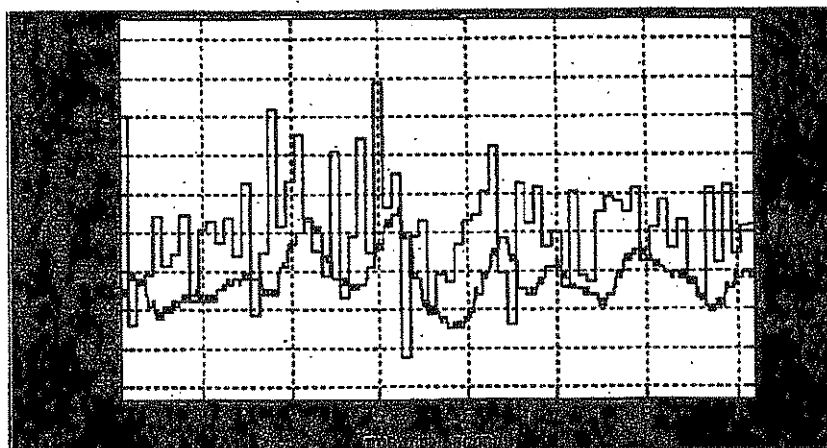


FIG. 332

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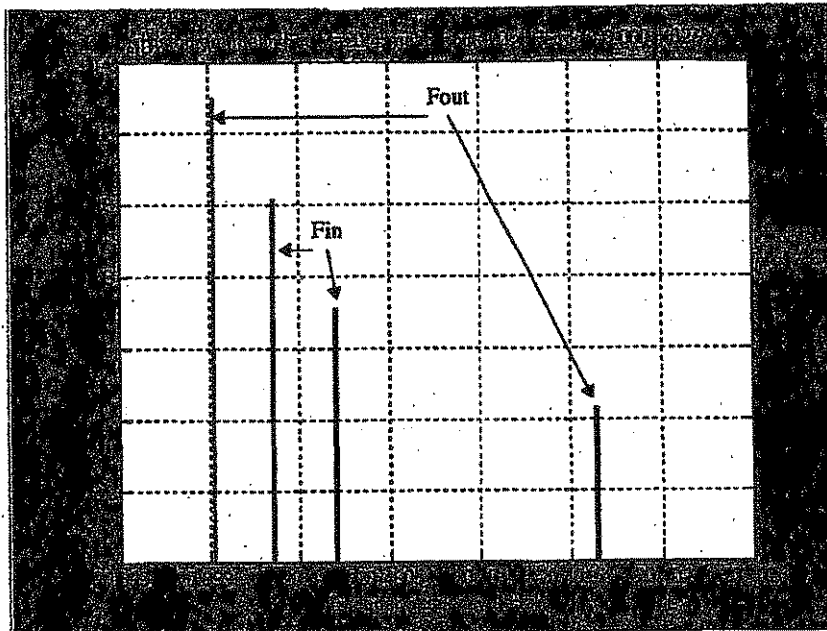


FIG. 333

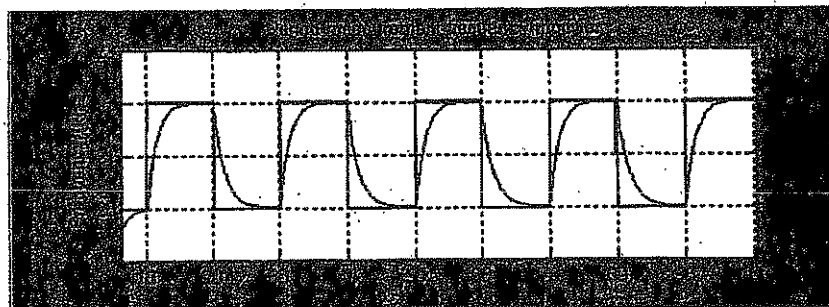


FIG. 334

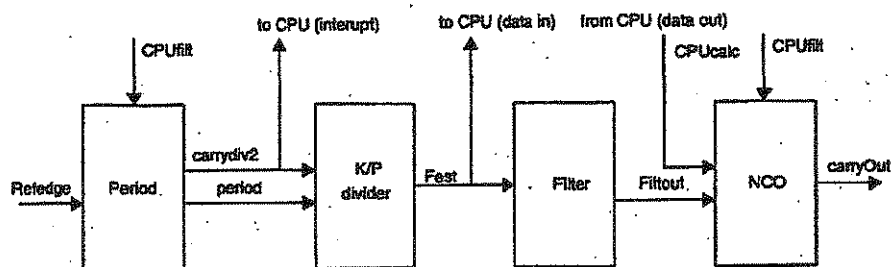


FIG. 335

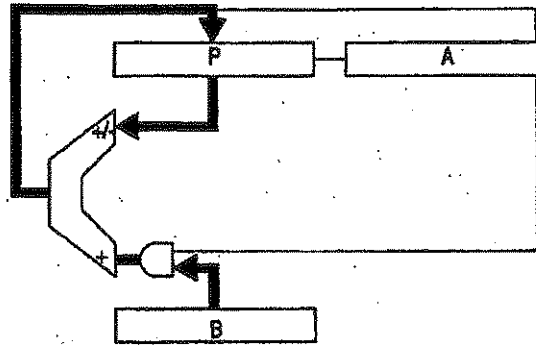


FIG. 336

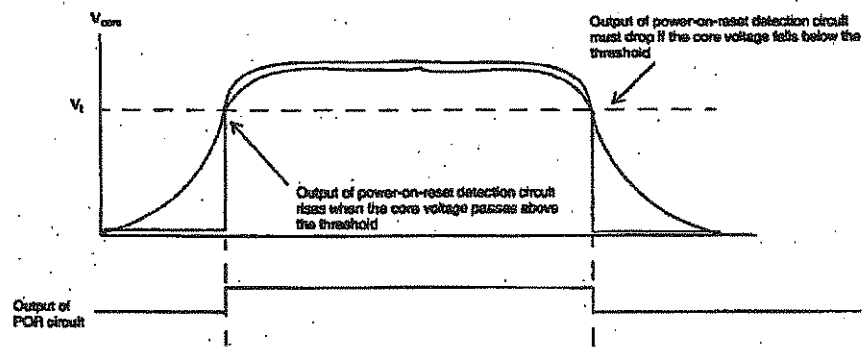


FIG. 337

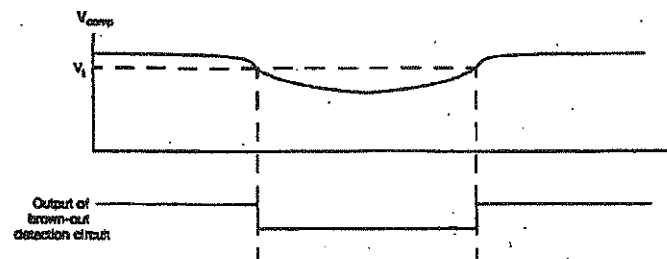


FIG. 338

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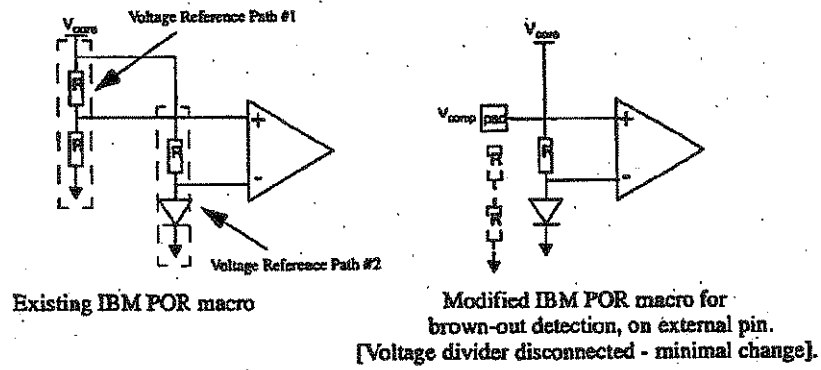


FIG. 339

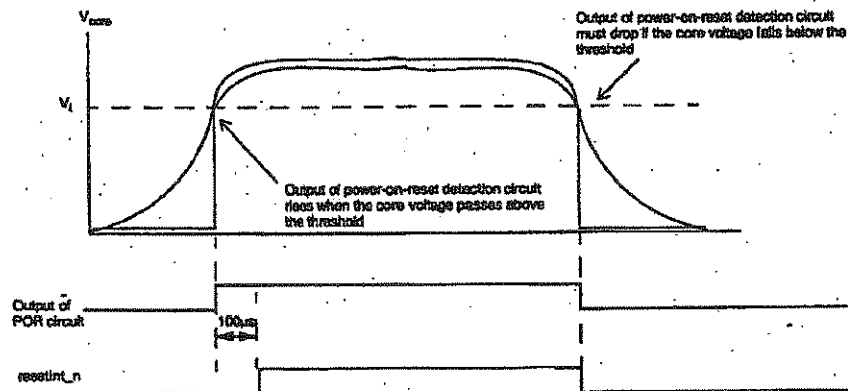


FIG. 340

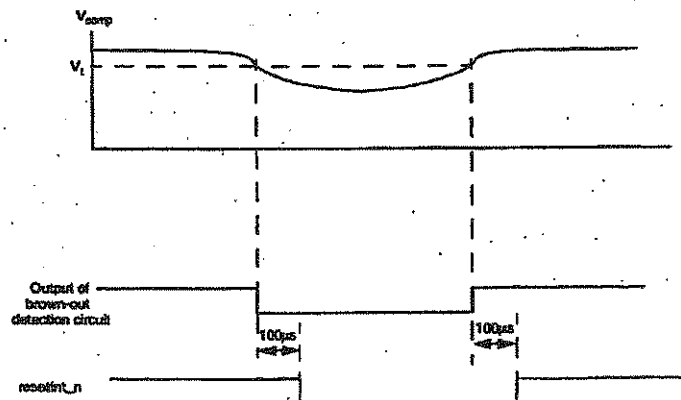


FIG. 341

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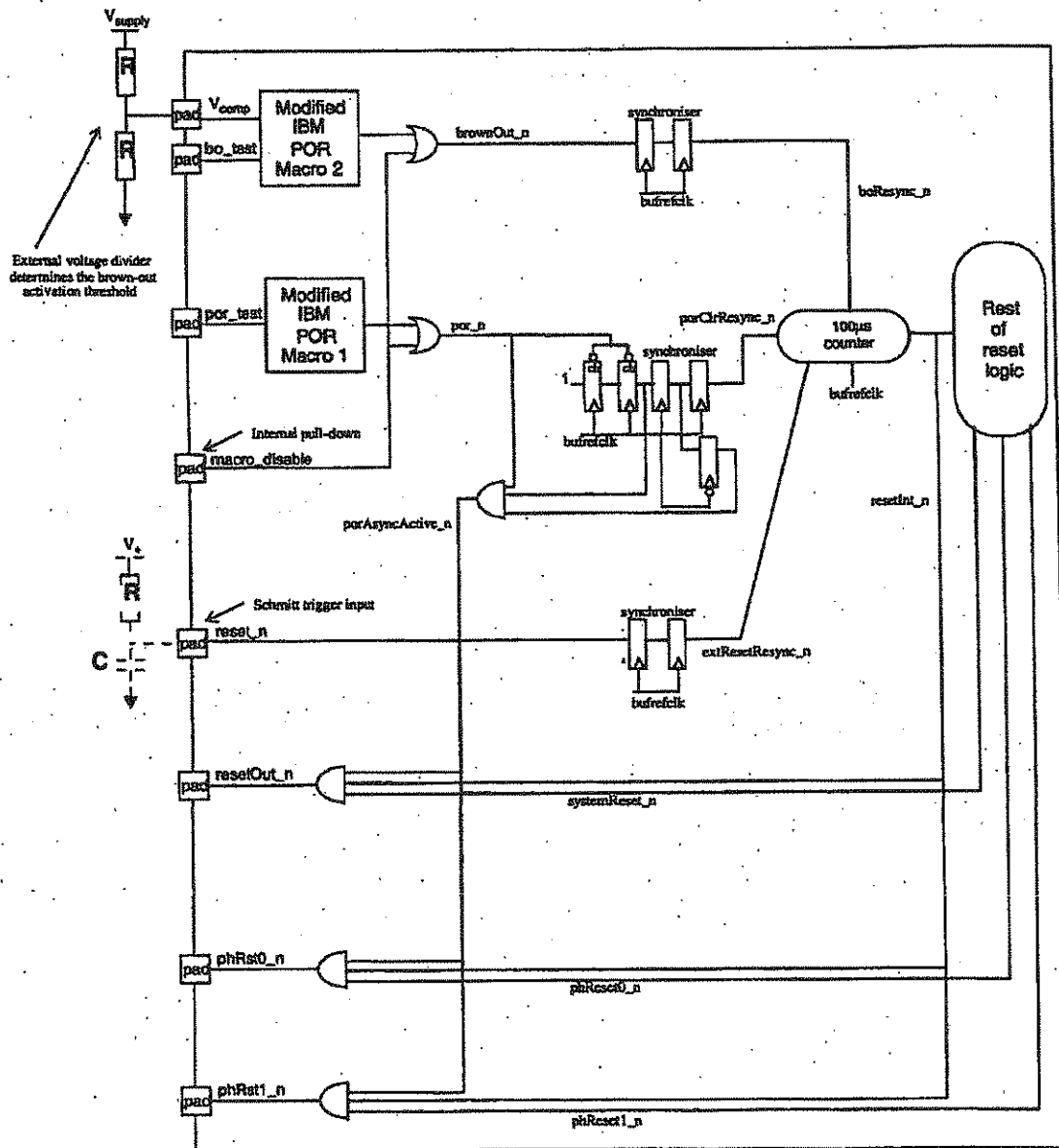


FIG. 342

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Length
Load Address
Run Address
Data (Second Stage Loader)

FIG. 343

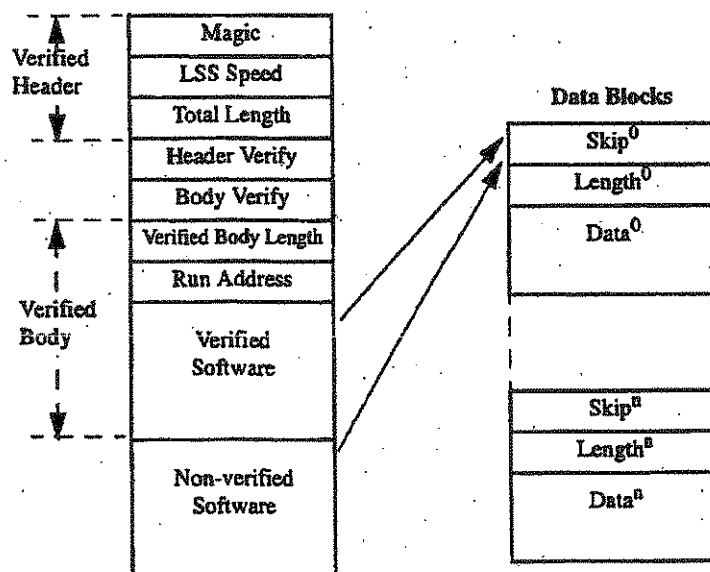


FIG. 344

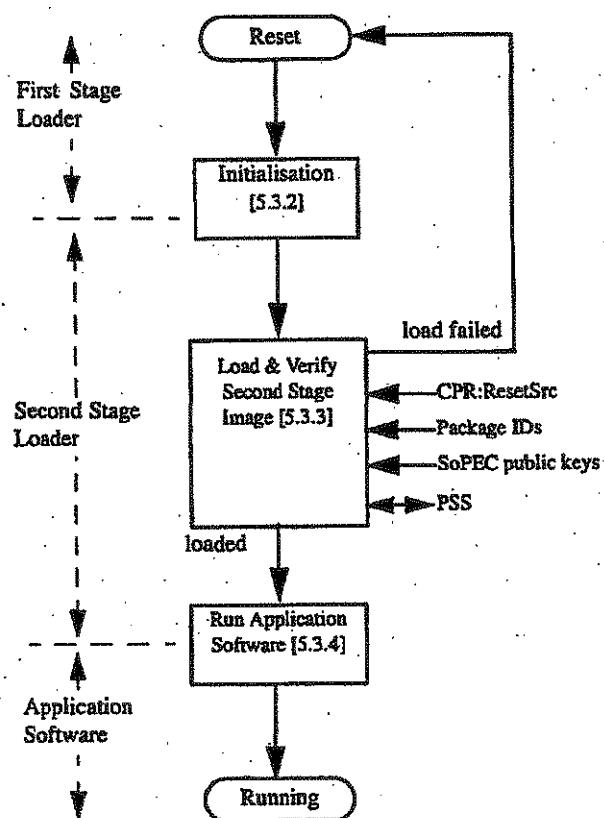


FIG. 345

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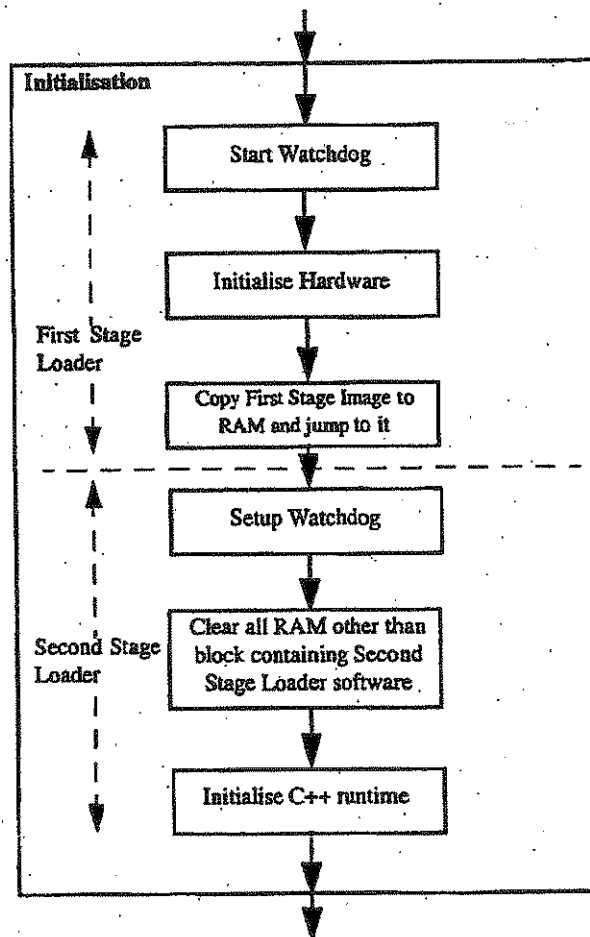


FIG. 346

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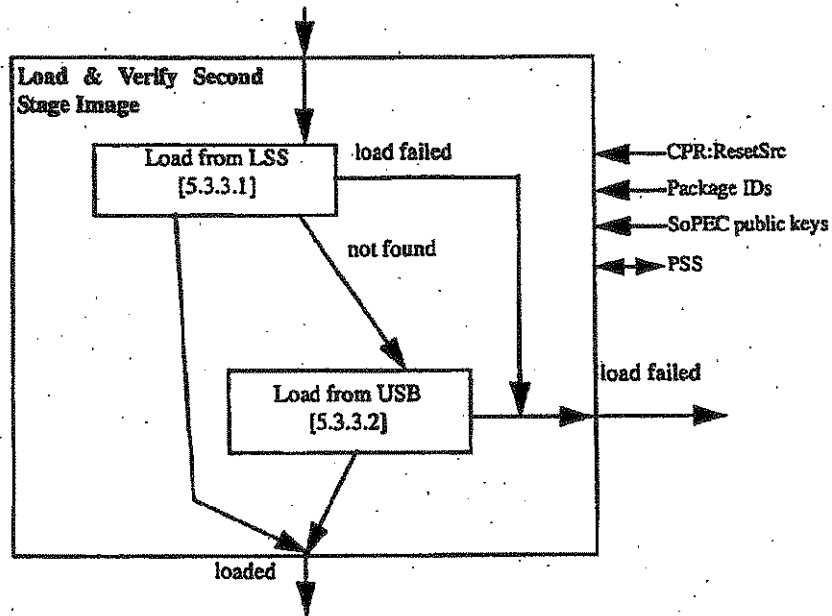


FIG. 347

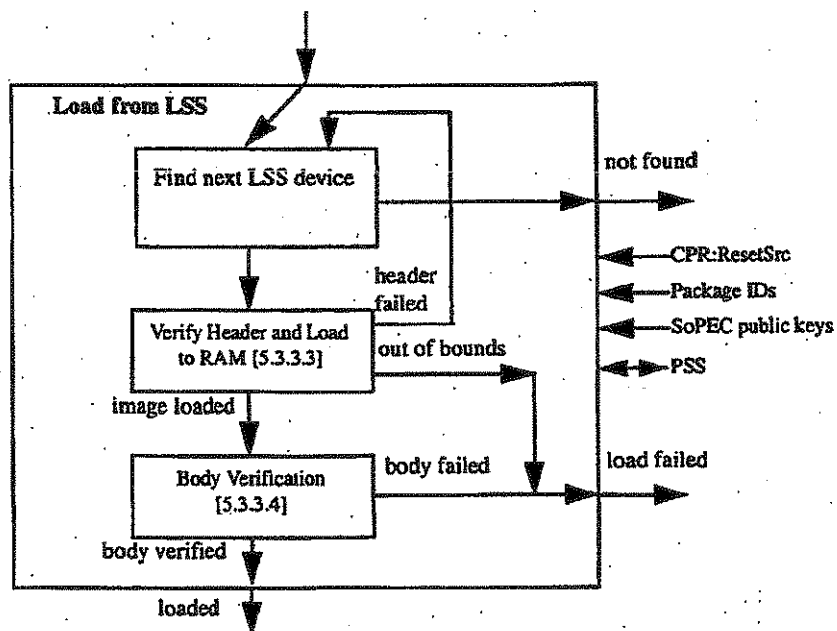


FIG. 348

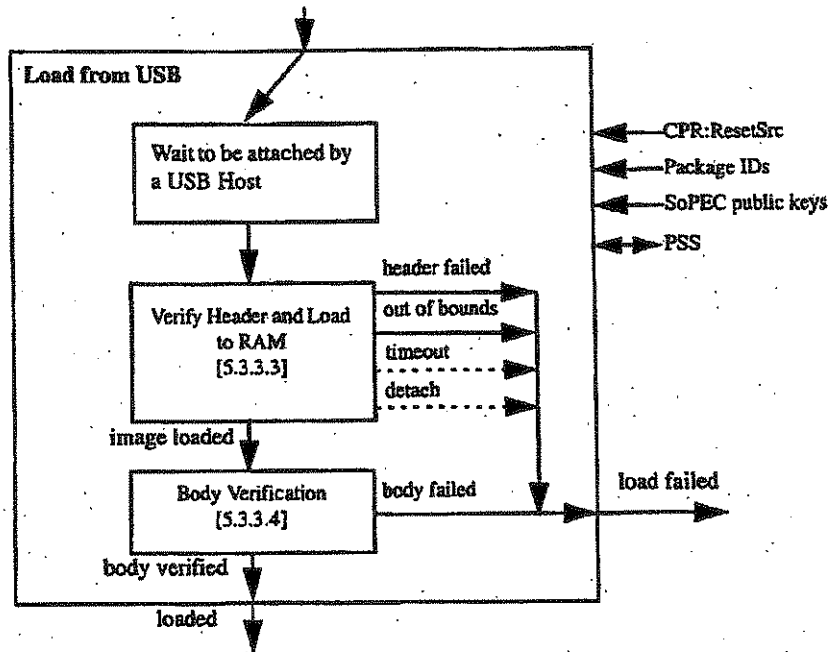


FIG. 349

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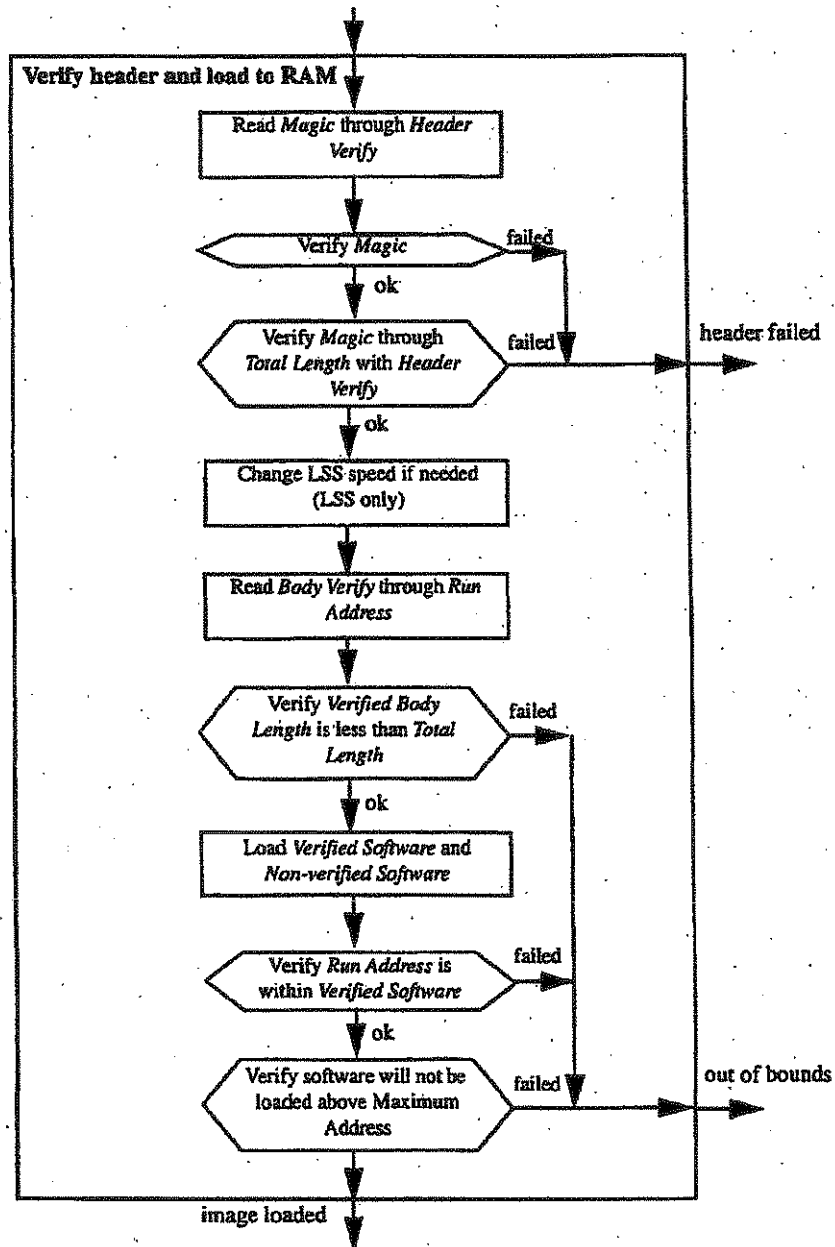


FIG. 350

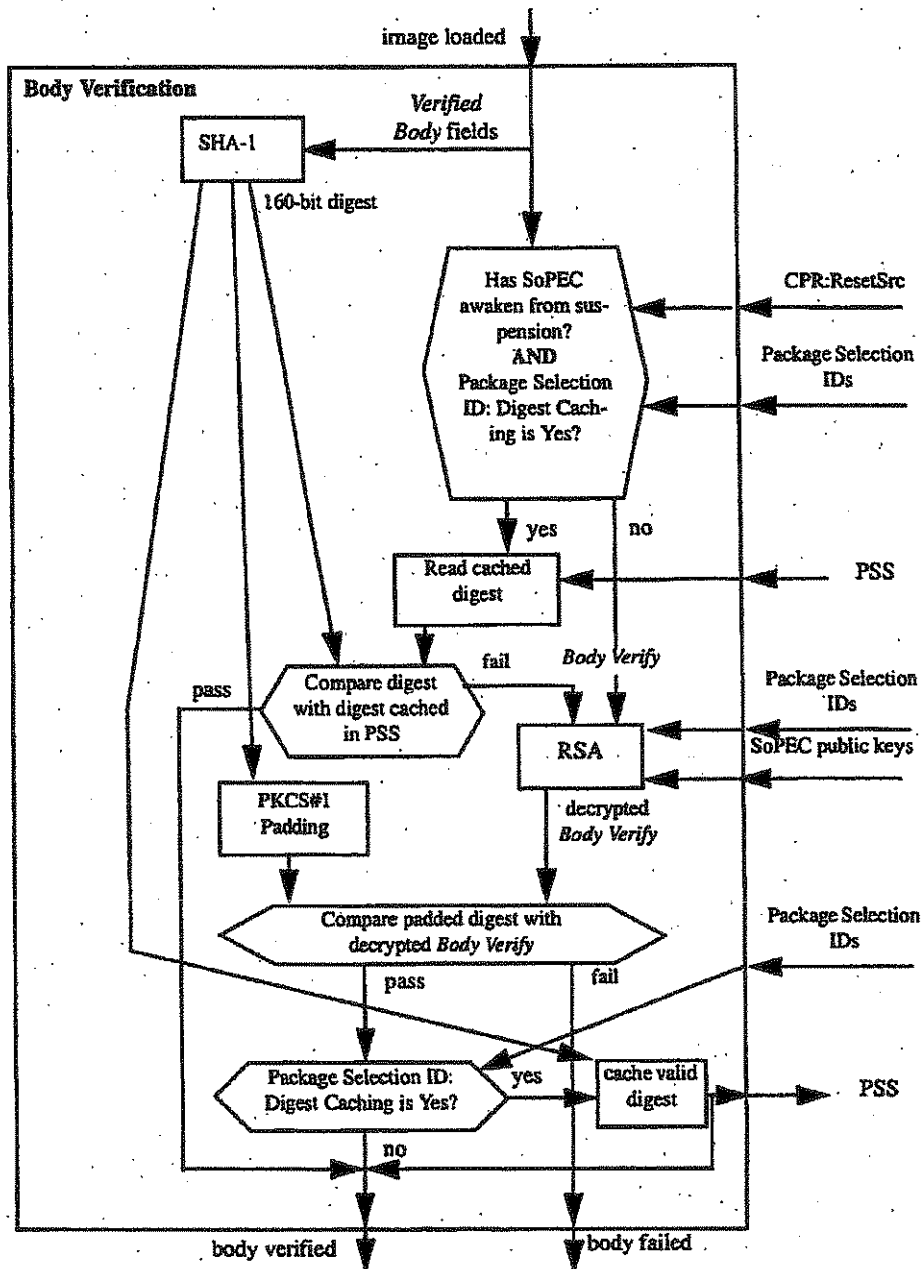


FIG. 351

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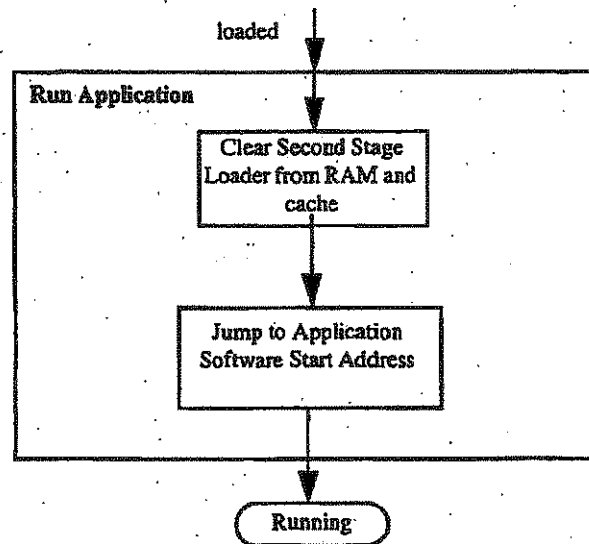


FIG. 352

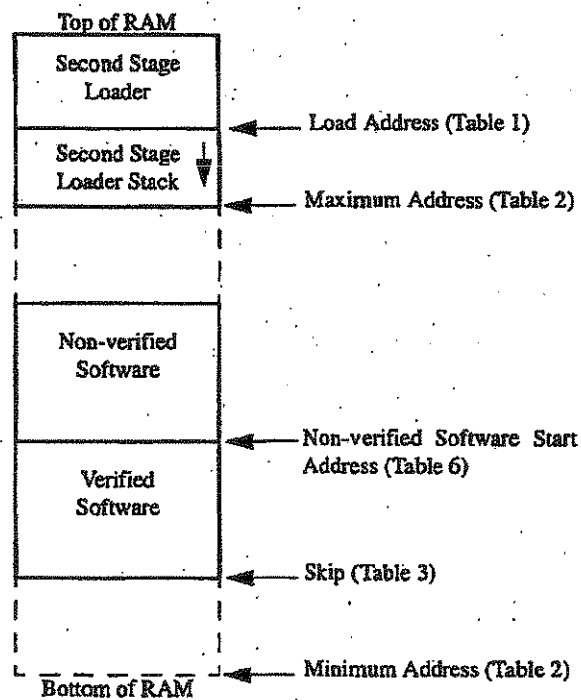


FIG. 353

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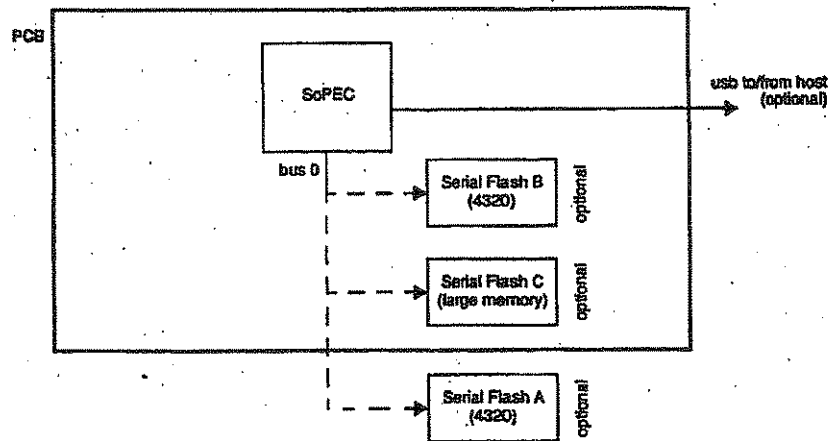


FIG. 354

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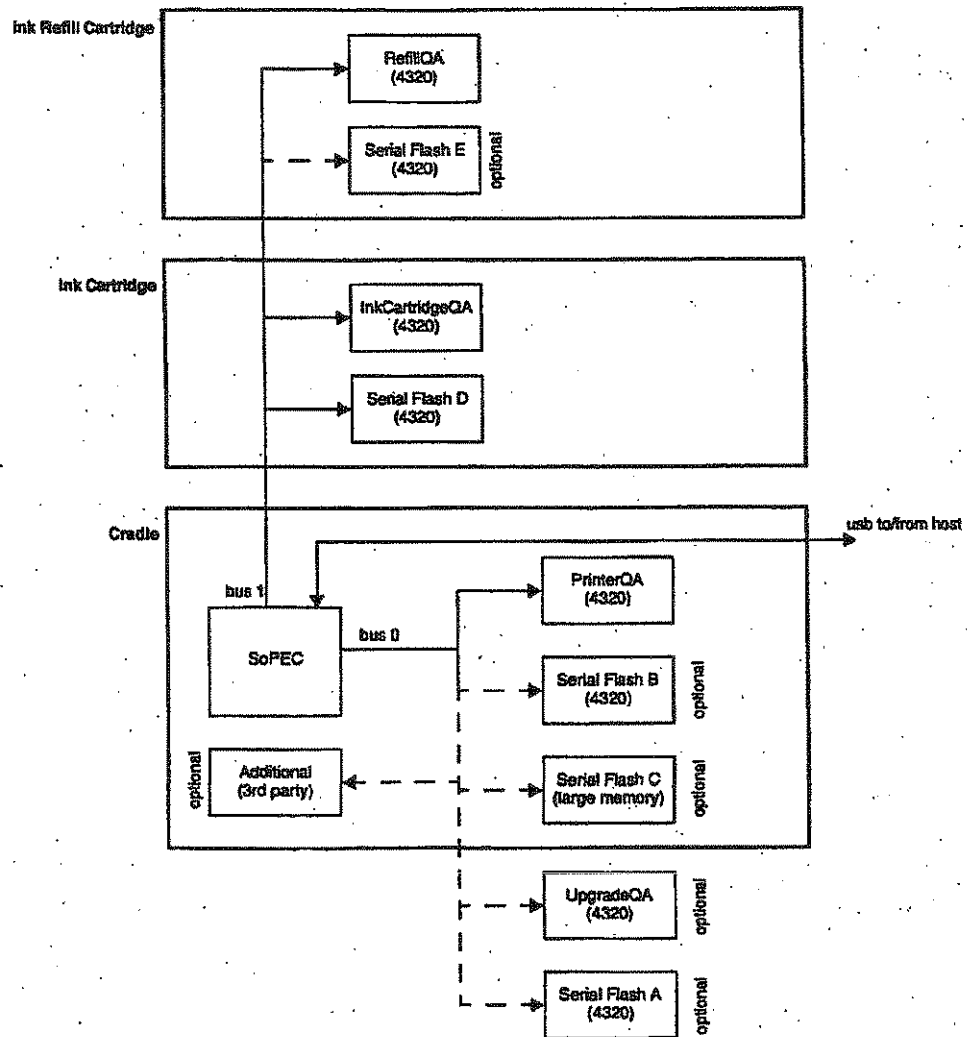


FIG. 355

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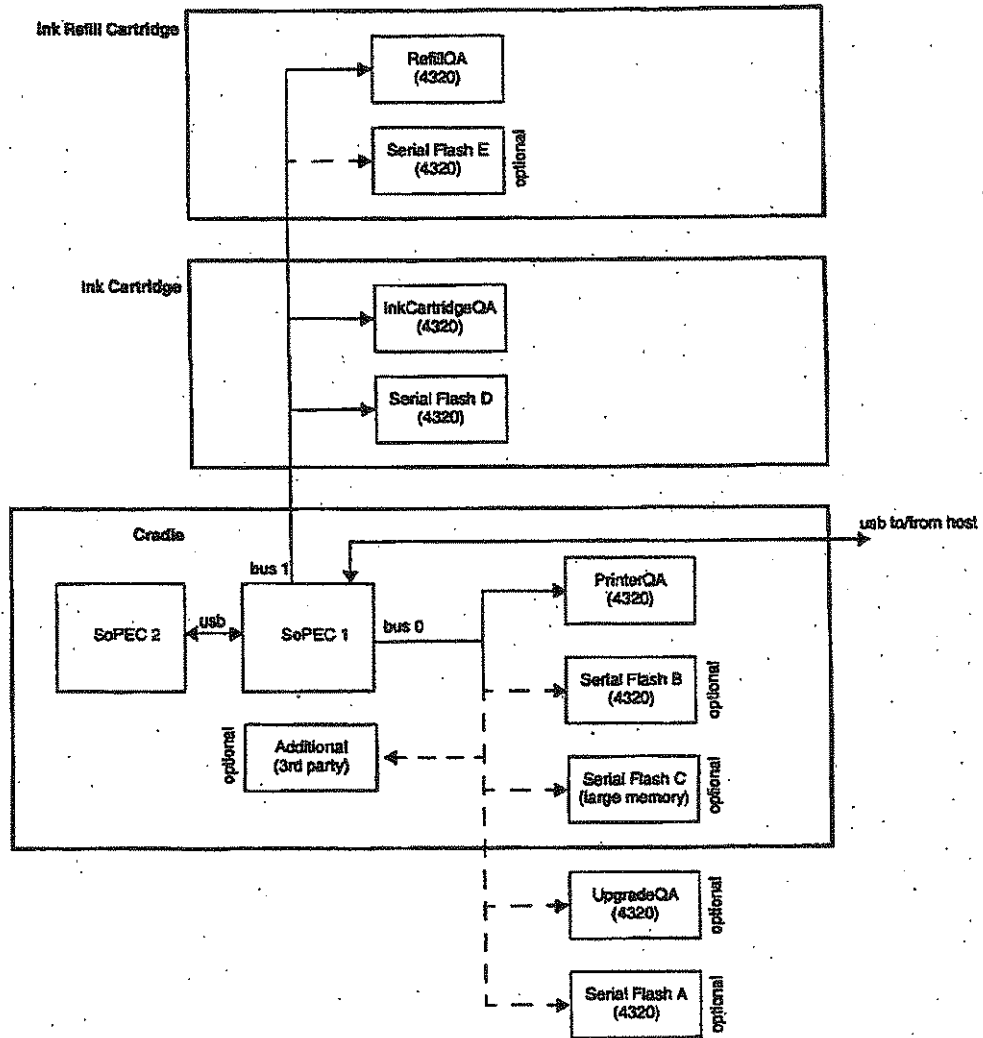


FIG. 356

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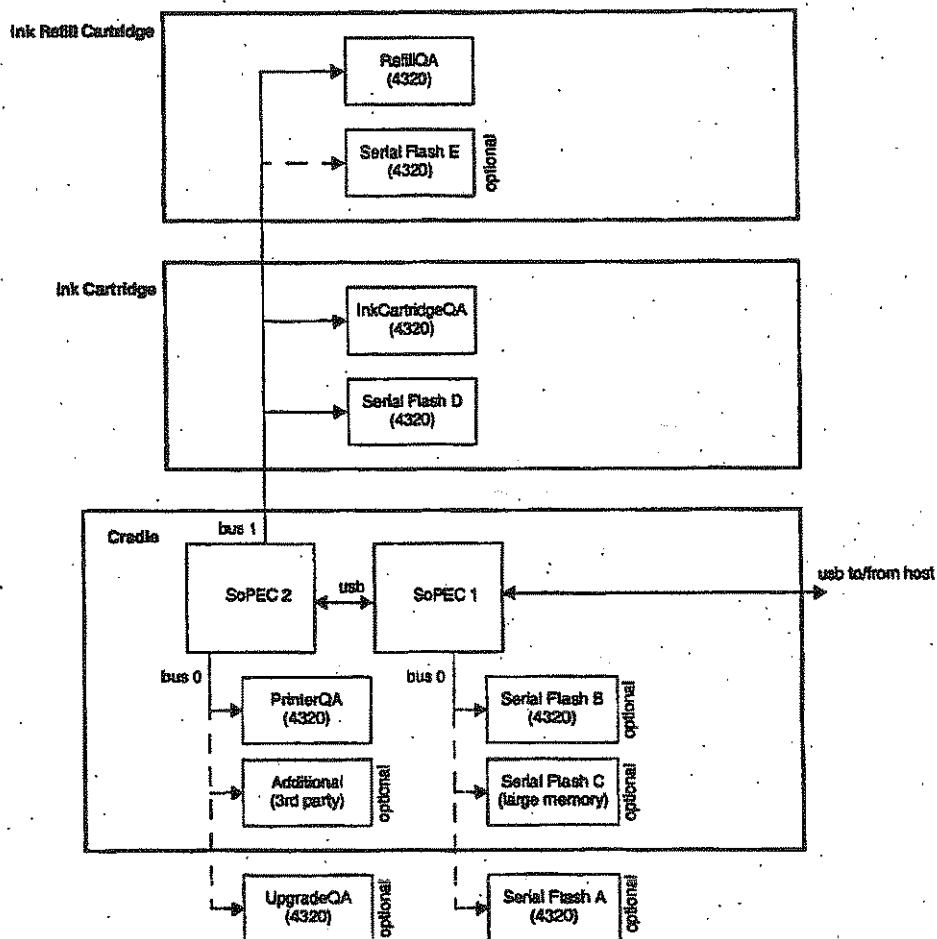


FIG. 357

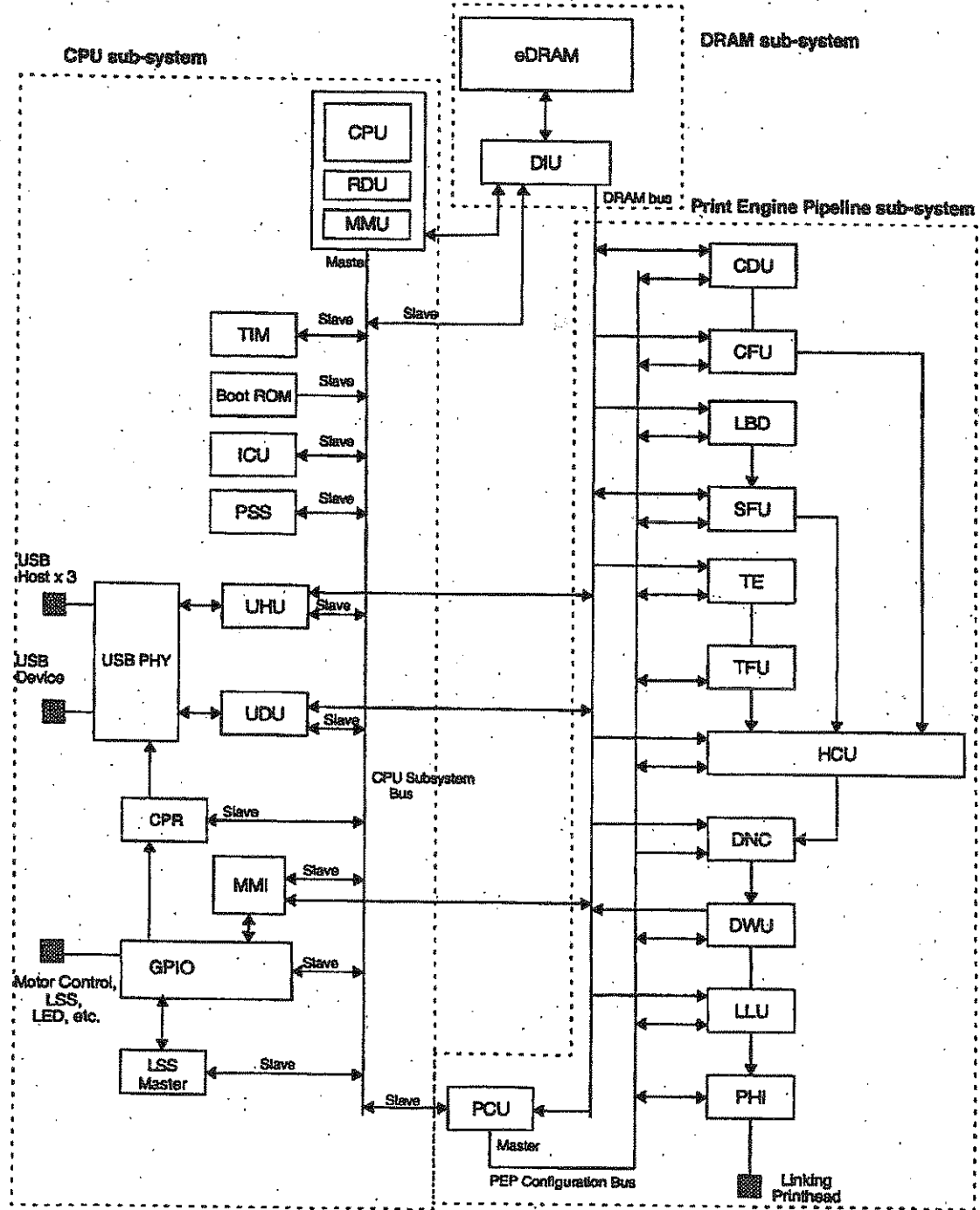


FIG. 358

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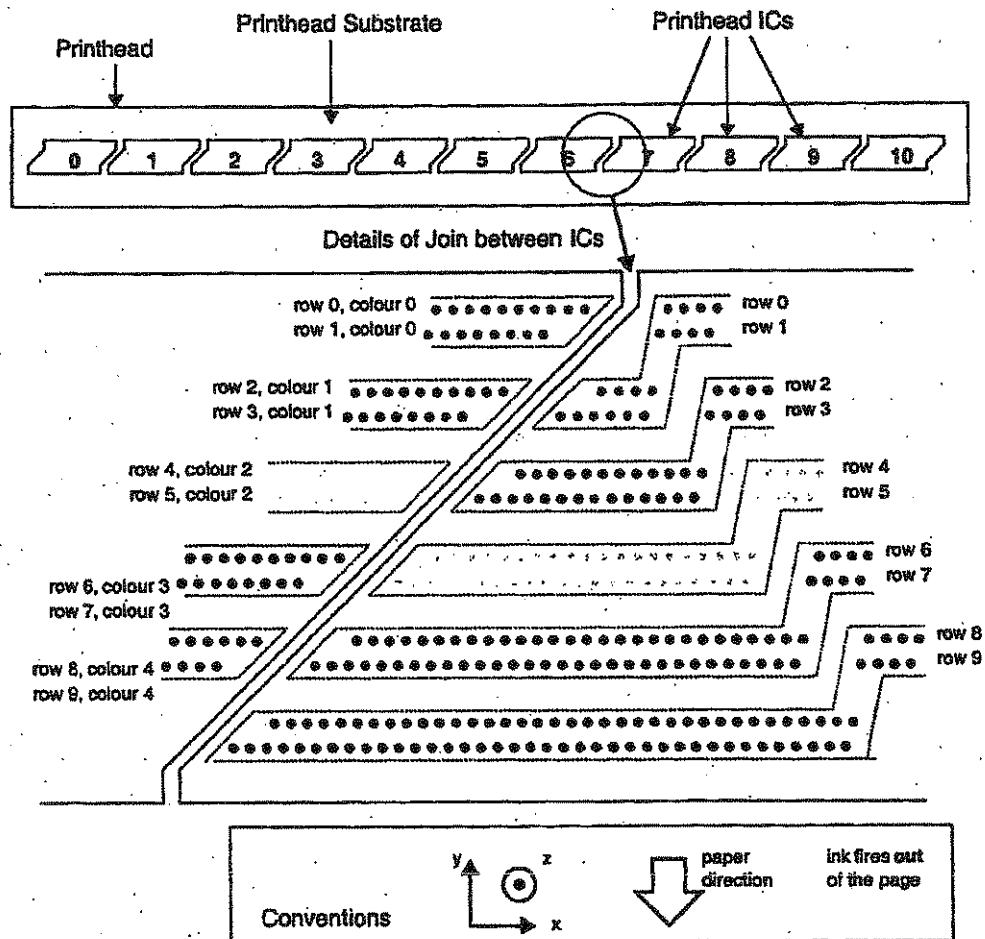


FIG. 359

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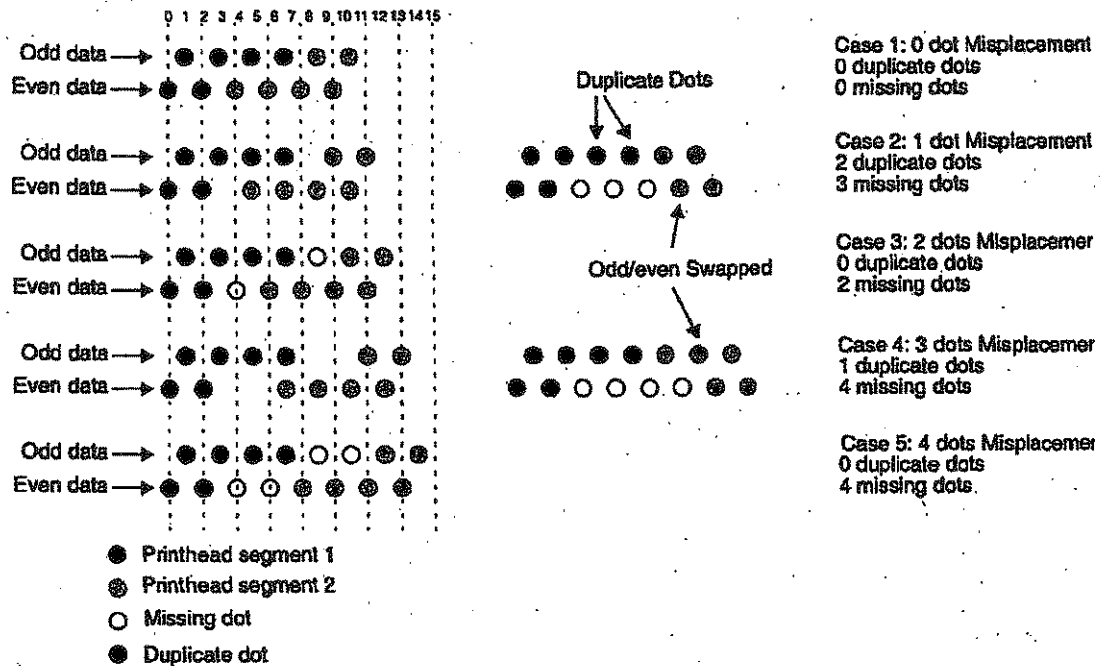


FIG. 360

Row Number	Default Firing Order	Relative Row position in line-pitches
0	1	0
1	6	3.5
2	2	10.1
3	7	13.6
4	3	20.2
5	8	23.7
6	4	30.3
7	9	33.8
8	5	40.4
9	10	43.9

FIG. 361

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Firing Order	Row position	Adjusted Firing Order	Row position relative to ideal segment row 0
1	0	4	0.3
6	3.5	9	3.8
2	10.1	5	10.4
7	13.6	10	13.9
3	20.2	6	20.5
8	23.7	1	24.0
4	30.3	7	30.6
9	33.8	2	34.1
5	40.4	8	40.7
10	43.9	3	44.2

Ideal segment

Segment misplaced by 0.3 line-pitches

FIG. 362

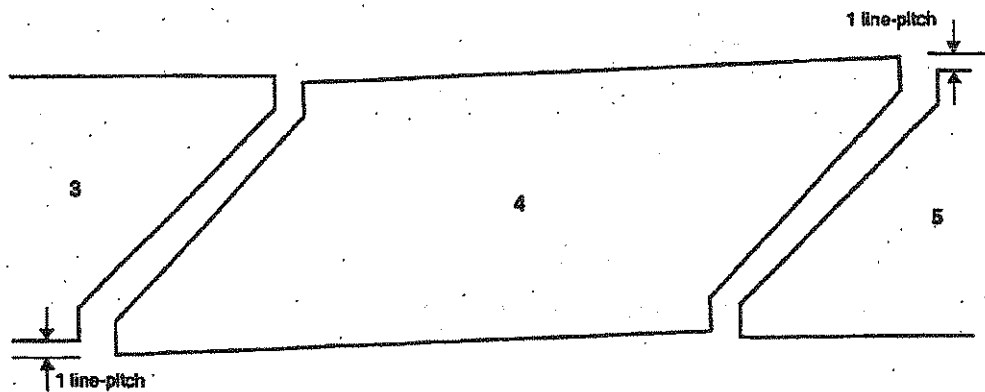


FIG. 363

Default Firing Order

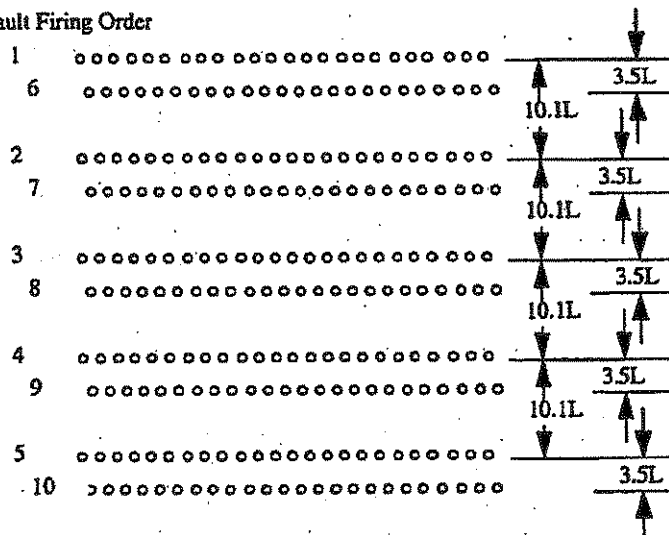


FIG. 364

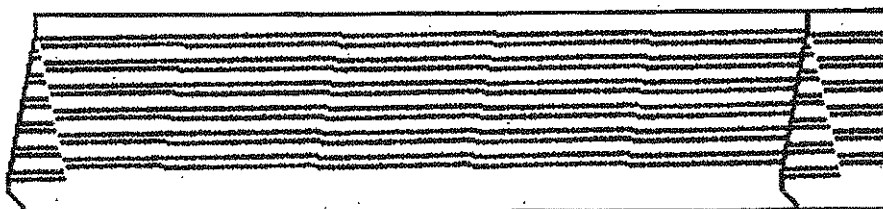


FIG. 365

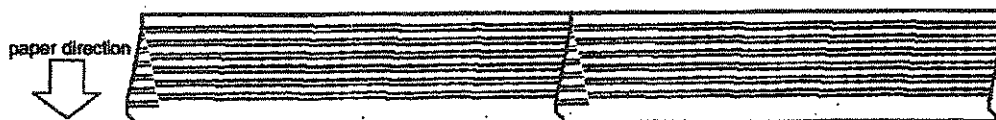


FIG. 366

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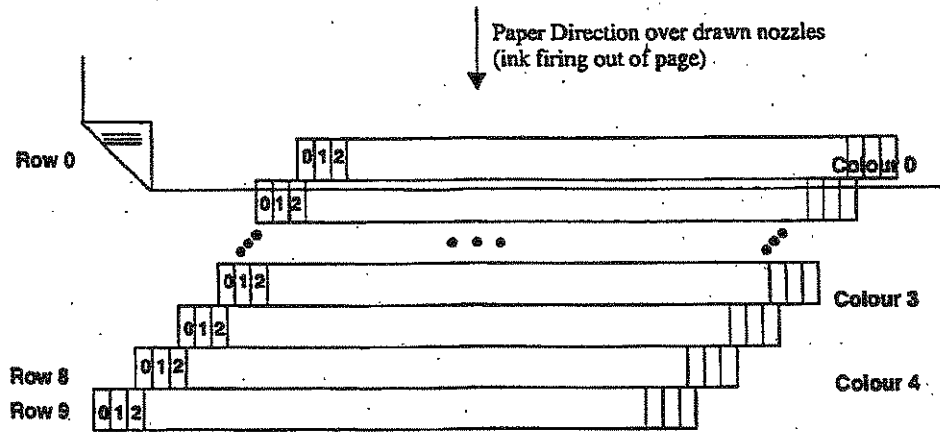


FIG. 367

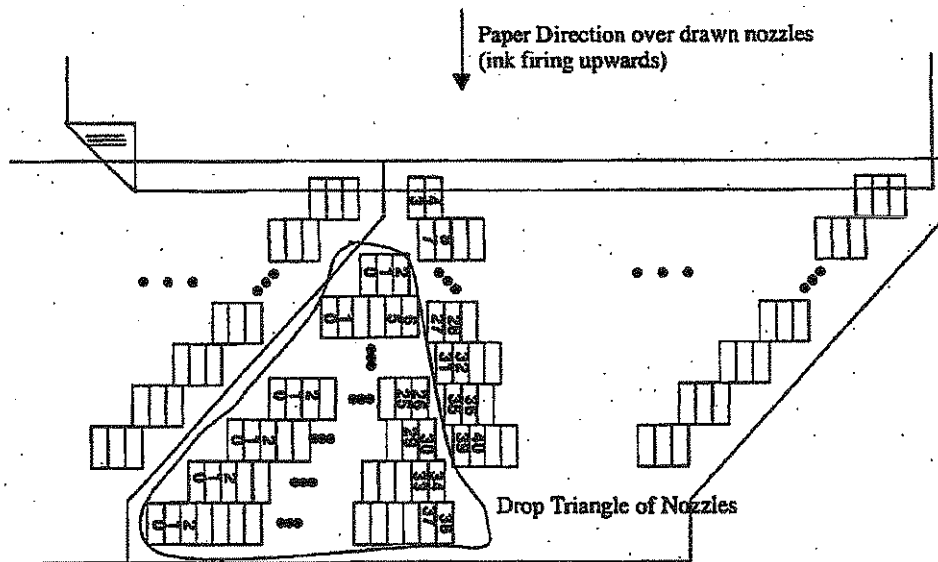


FIG. 368

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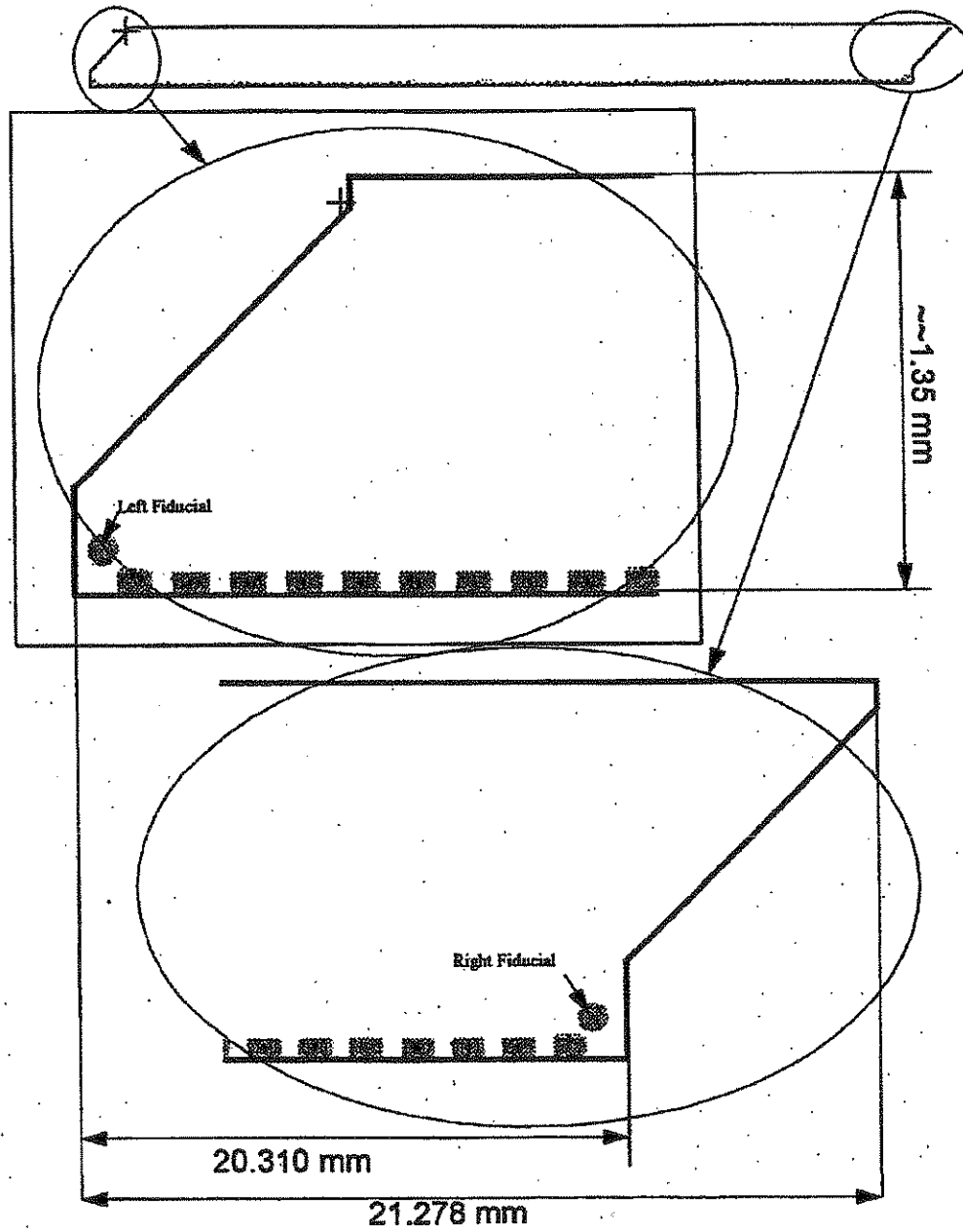


FIG. 369

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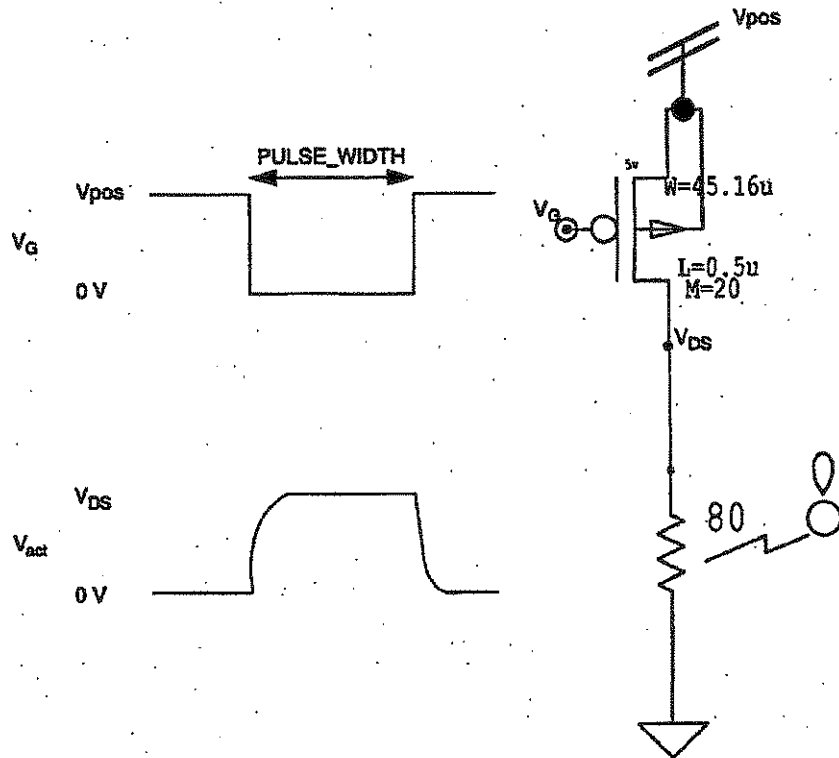


FIG. 370

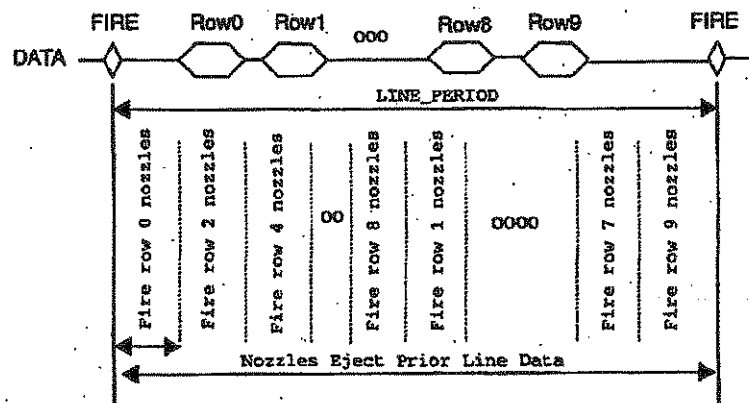


FIG. 371

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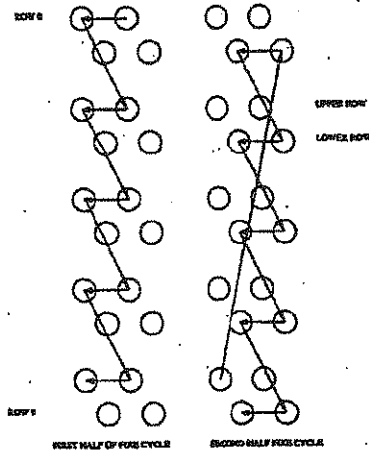


FIG. 372

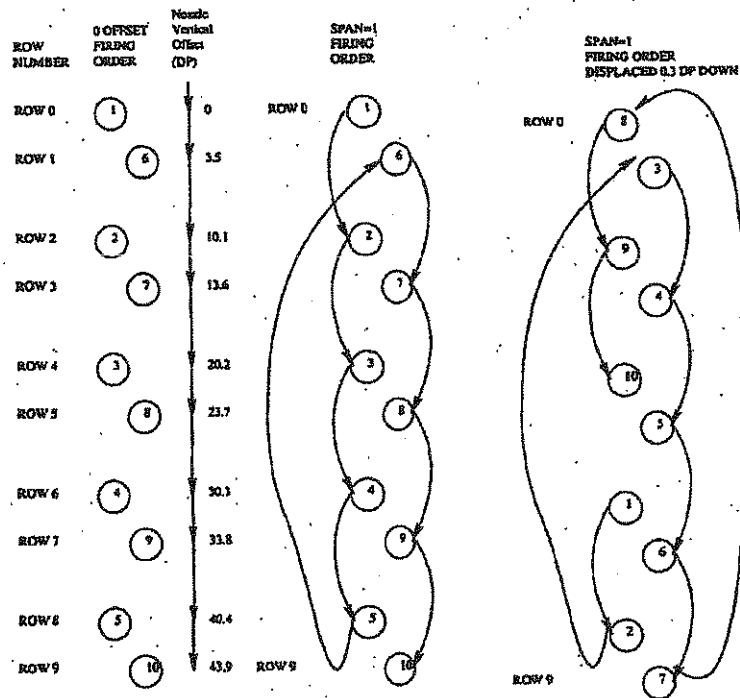


FIG. 373

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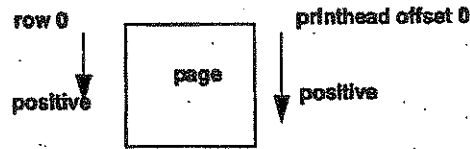


FIG. 374

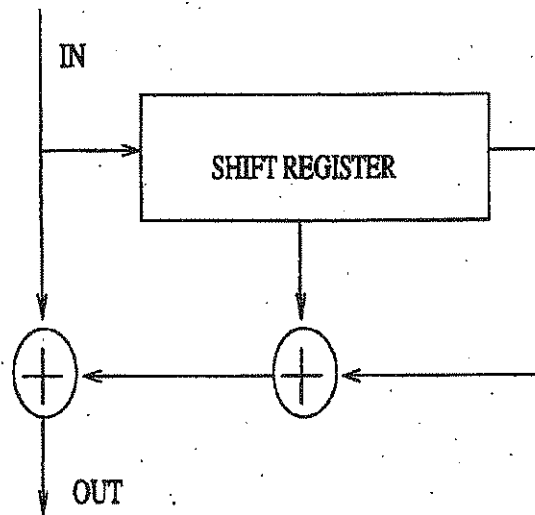


FIG. 375

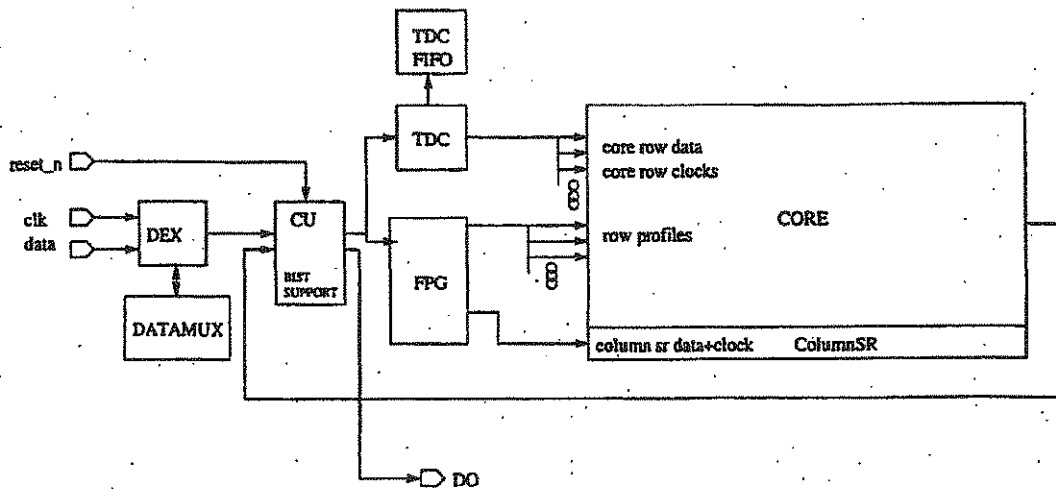


FIG. 376

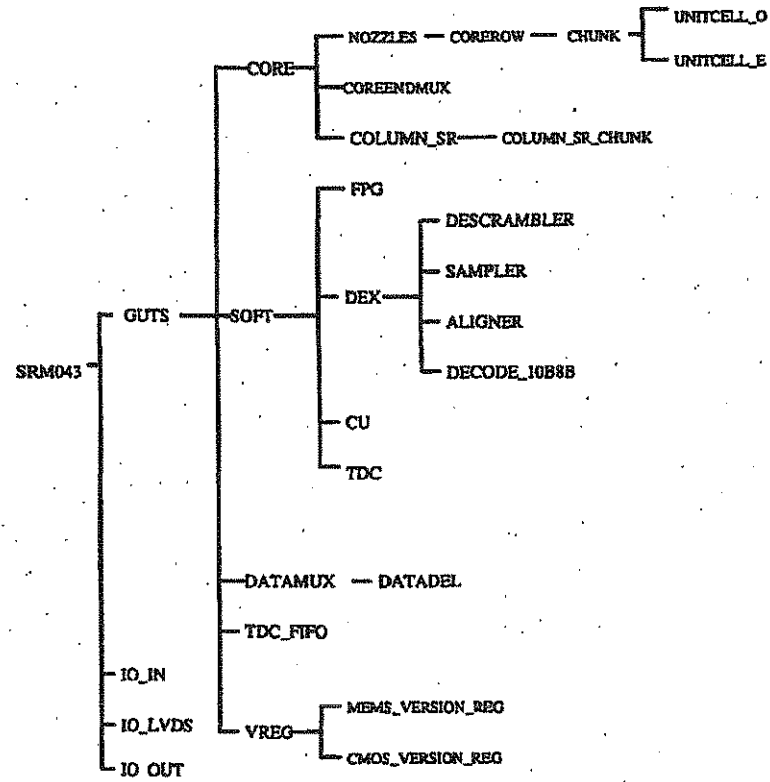


FIG. 377

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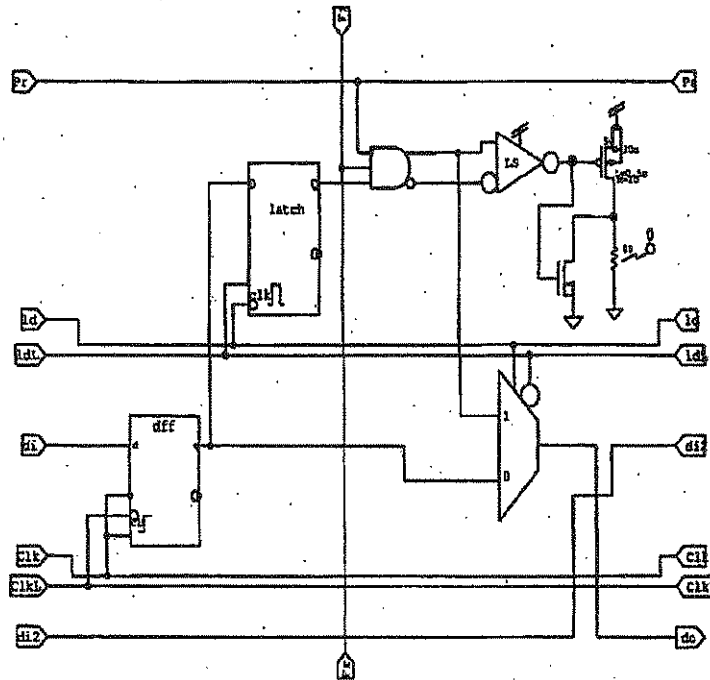


FIG. 378

	uu7		uu6		uu5		uu4		uu3		uu2	Pr	uu1	Ck	uu0	La
ul7		ul6		ul5		ul4		ul3		ul2		ul1	Pr	ul0	Ck	

FIG. 379

FIRE	
D0	D1
D1	D2
LD	LD
PR	PR
CK	CK
FIRE	

FIG. 380

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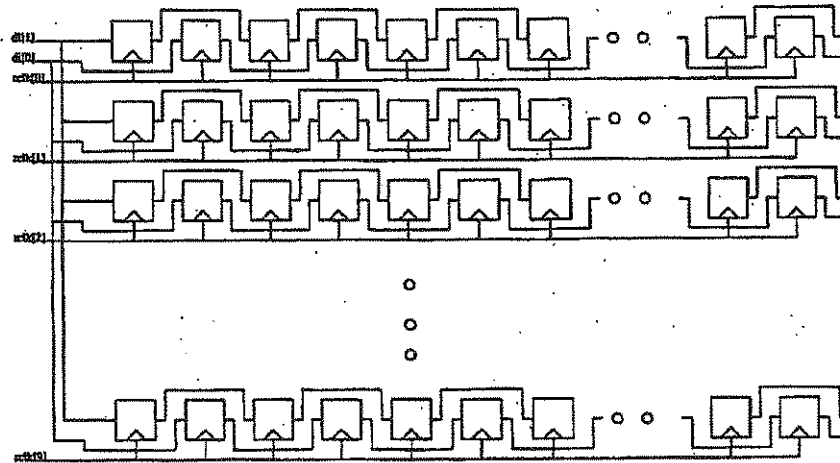


FIG. 381

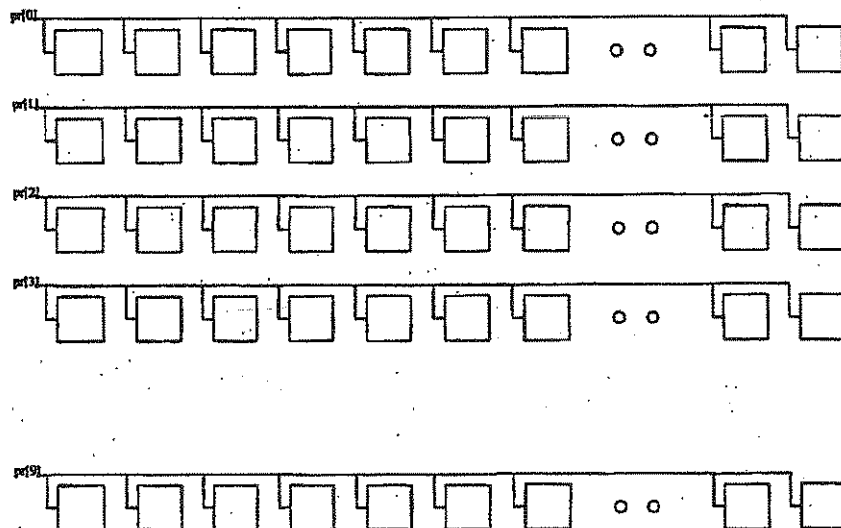


FIG. 382

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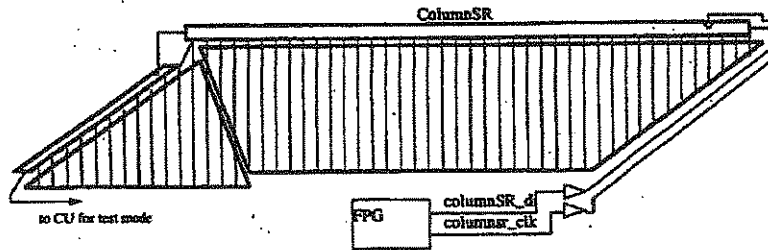


FIG. 383

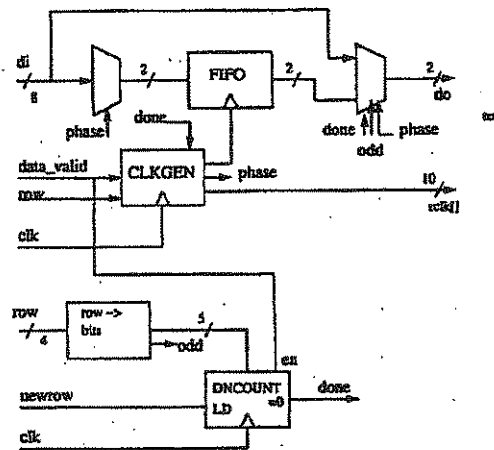


FIG. 384

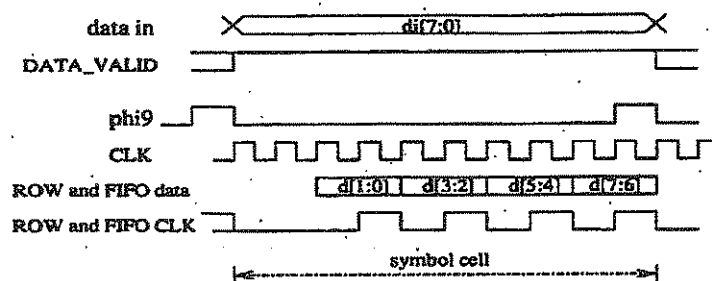


FIG. 385

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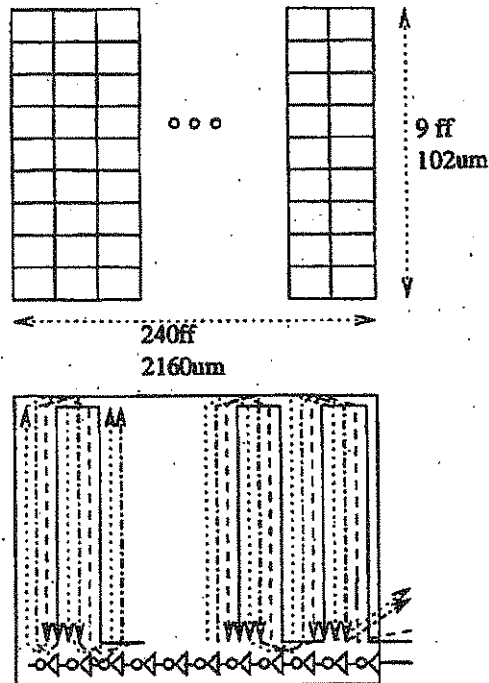


FIG. 386

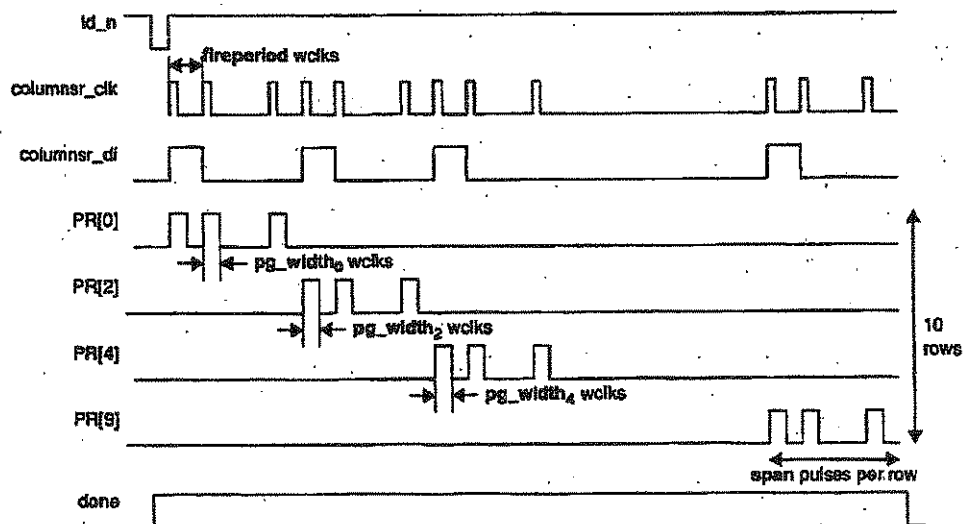


FIG. 387

```

graph LR
    DATA --> DS[DATA SAMPLER]
    CLK --> DS
    DS -- D --> DES[DESCRAMBLE]
    CLK --> DES
    DES -- ALIGN --> ALN[ALIGN]
    CLK --> ALN
    ALN -- ERROR --> ERR[ERR]
    ALN -- CLK2 --> SD[SER/IOB DECODE]
    CLK --> SD
    SD -- D/S --> D_S[D/S]
    SD -- ERR --> ERR
    SD -- Wdr --> Wdr
    SD -- Wdr --> Wdr
    SD -- CLK2 --> CLK2[CLK2]
    CLK2 --> CLK[CLK]
  
```

FIG. 390

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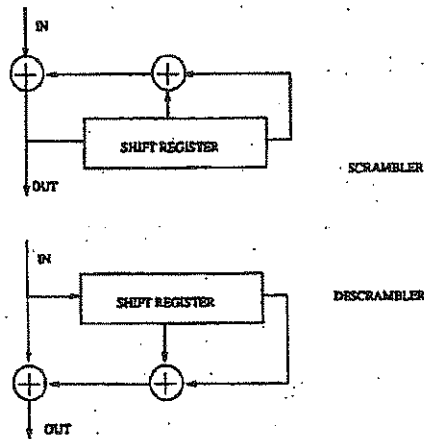


FIG. 391

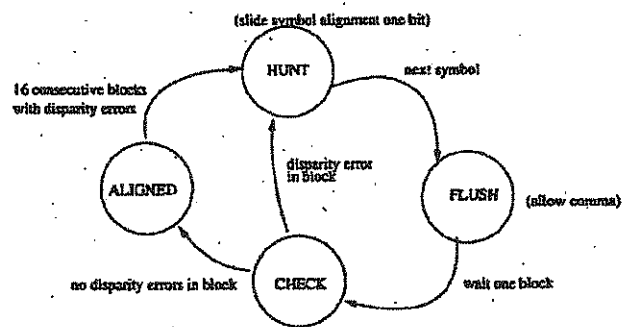


FIG. 392

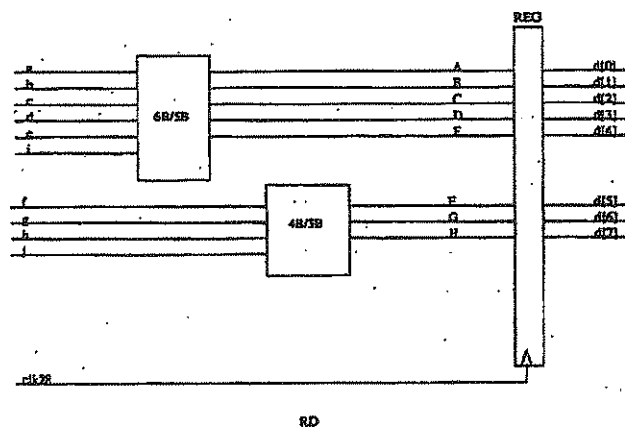


FIG. 393

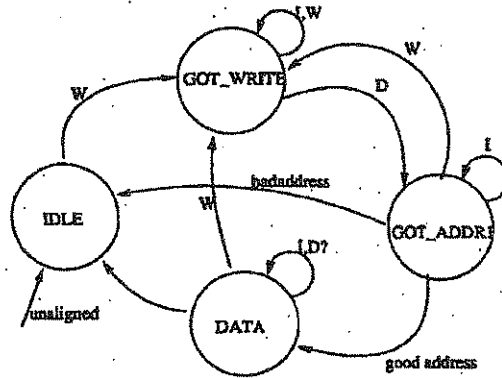


FIG. 394

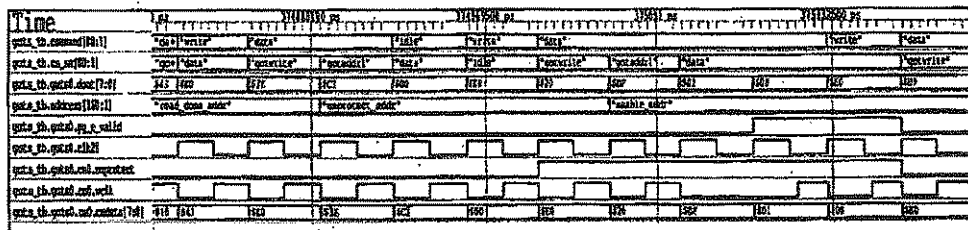


FIG. 395

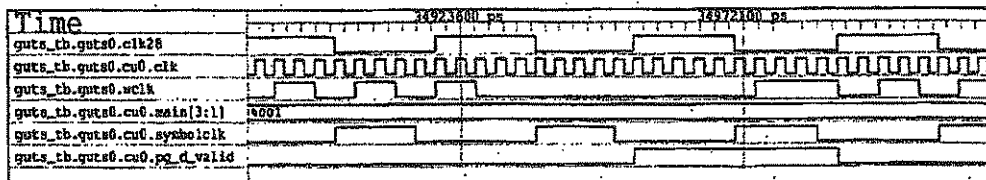


FIG. 396

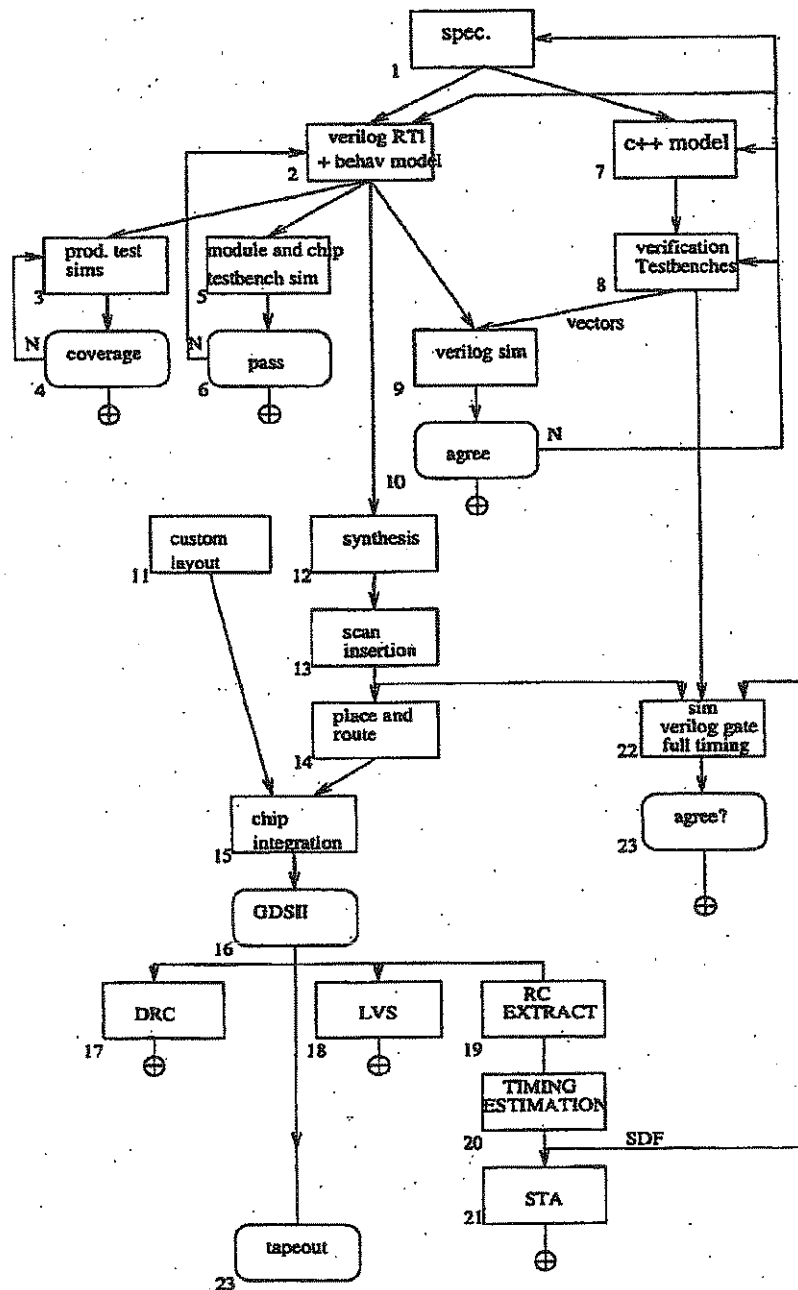


FIG. 397

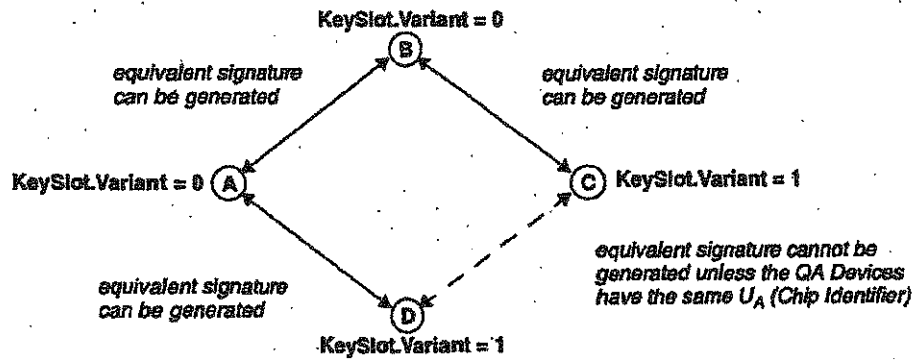


FIG. 398

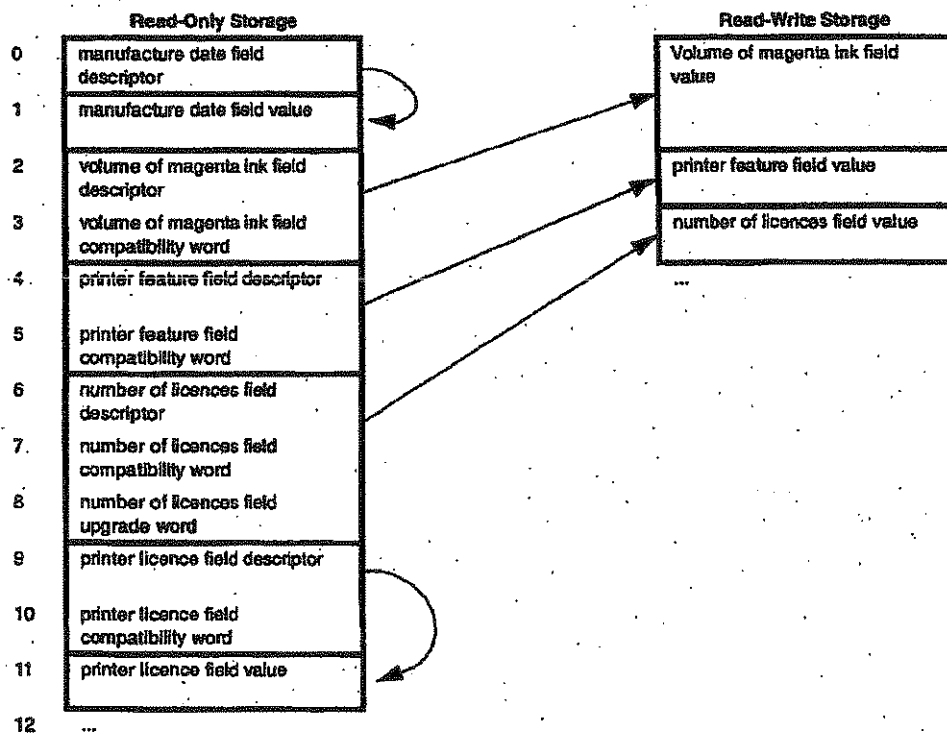


FIG. 399

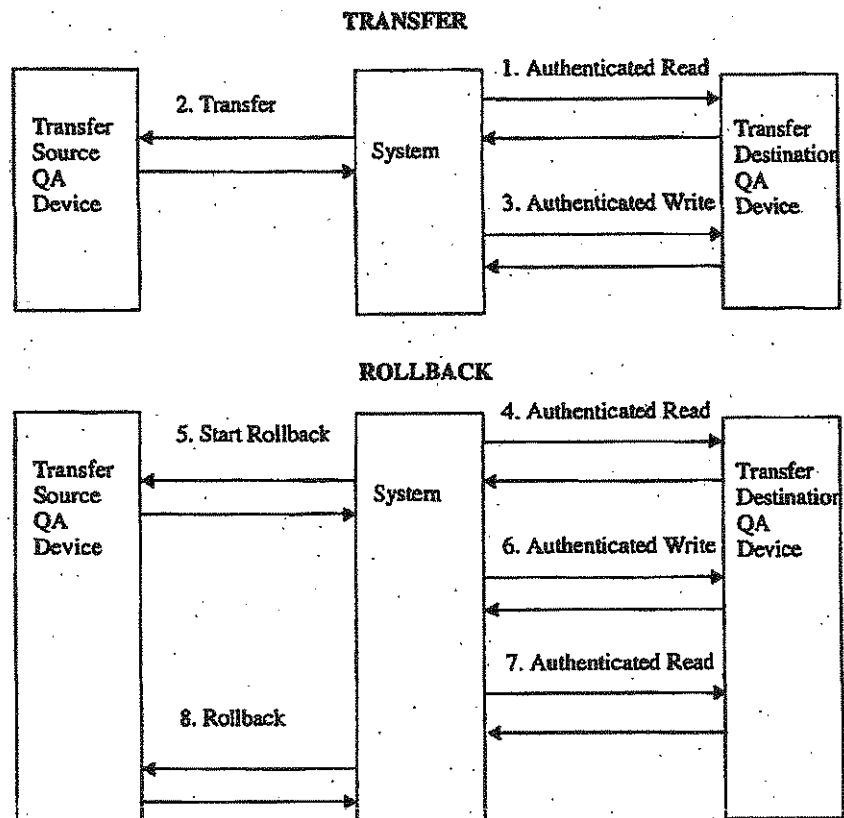


FIG. 400