

MEMORY CONTROL DEVICE AND MEMORY CONTROL METHOD

ABSTRACT

A memory control device includes a CPU 1, a flash ROM
5 4 that records therein first information having undergone
an error-correction coding process and second information
not having undergone an error-correction coding process, an
address line switch 5 that switches between a first path
that connects an address bus 2 to the ROM 4 so that the CPU
10 1 can read the first information recorded in the ROM 4 and
a second path that connects the address bus 2 to the ROM 4
so that the second information recorded in the ROM 4 can be
erased, written, and read, a decoder 7 that performs error
correction on the first information recorded in the ROM 4
15 and performs decoding, and a second switch 6 that switches
between a third path that connects the decoder 7 to the
data bus 3 so that information decoded by the decoder 7 is
transmitted to the data bus 3 and a fourth path that
connects the ROM 4 to the data bus 3 so that the second
20 information recorded in the ROM 4 can be erased, written,
and read.

Fig. 1