

Radio Paging Receiver Capable of Muting Battery Saving Function

The present invention relates to a paging receiver, and more particularly to a radio paging receiver having a battery saving function.

A conventional radio paging receiver generally includes a battery saving circuit to save battery power, as disclosed in the U.S. Patent No. 4,194,153 "Digital Radio Paging Communication System", granted to M. Masaki et al. on March 18, 1980. The battery saving circuit supplies power intermittently to the receiver during the absence of paging signals while supplying it continuously in response to the reception of the paging signals. However, while such an intermittent supply of power is effective to power saving, it inconveniences the test or adjustment to which each receiver is subjected before being marketed.

A method for placing the receiver in condition for test operation has been proposed in the pending U.S. Patent Application by H. Abe et al. entitled "Portable Radio Communication Device Structure", Serial No. 159,154, filed on June 30, 1980. This method mounts a strapping connector with magnet on top of a battery thereby to mute the battery saving circuit. This permits the receiver to be placed in condition for test operation even when placed outside its case. However, the strapping connector tends to be easily lost by mistake.

Therefore, an object of the present invention is to provide a radio paging receiver capable of muting its battery saving operation without resorting to any external manipulation such as strapping.

5 In the preferred embodiment there is a radio paging receiver capable of suspending its battery saving function by receiving a specified tone- or digital-pattern for test.

In one arrangement a radio paging receiver has a single-chip central processing unit (CPU),
10 capable of suspending its battery saving operation by receiving a specified digital-pattern signal for test.

In a particular embodiment of the invention, a radio paging receiver comprises battery saving means for intermittently supplying power to some or all of its circuits at least while signals addressed
15 thereto are being received; detecting means for detecting a specified tone- or digital-pattern for test out of received signals; and means for continuously supplying power to some or all of its circuits by suspending the operation of the battery saving means in response to the output of the detecting means, thereby placing the receiver in
20 condition for test operation.

Other objects, features and advantages of the present invention will become more apparent from the detailed description hereunder taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a schematic block diagram of a radio paging receiver according to the present invention;

FIGS. 2A to 2E show the signal formats for use in a radio paging receiver according to the present invention;

5 FIGS. 3A to 3F and 4A to 4F are operational time charts showing waveforms at various points within the receiver illustrated in FIG. 1;

FIG. 5 is a schematic block diagram of an embodiment of the present invention, wherein the decoder section of the receiver illustrated
10 in FIG. 1 is made of a single-chip CPU; and

FIG. 6 is a flow chart showing the operation of the decoder section illustrated in FIG. 5.

Referring to FIG. 1, an antenna 1 is connected to a receiver
15 section 2, signals from which are led to a waveform shaping circuit 3. The waveform shaping circuit 3 supplies the waveform-shaped output to identity detecting section 6, a bit synchronizing circuit 7 and a 31-bit shift register 8, all in a decoder 5.

The identity detecting section 6 is connected to a programmable
20 read only memory (PROM) 9 and supplies its output to an alert tone generating circuit 10, which, with its output, drives an annunciator 11. The bit synchronizing circuit 7 supplies its output to the clock terminals of the identity detecting section 6 and the shift register 8 for their bit

synchronization. The output #1 to #31 of the shift register 8 are supplied to the input terminals of an AND gate 16 either through inverters 12 to 15 or directly.

The output of the AND gate 16 is led to the set terminal of a flipflop 17 an output from whose Q terminal is led to one of the input terminals of a NOR gate 18. To the other input terminals of the NOR gate 18 are supplied the outputs of the identity detecting section 6 and an oscillation circuit 20. The output of the NOR gate 18 is led to the base terminal of a switching transistor 21 to control its switching.

The switching transistor 21 receives at its emitter power supply from a battery 22 through a switch 23, and to its collector are connected the receiver section 2 and the waveform shaping circuit 3. That is, whether or not the power is supplied depends on the switching control of the transistor 21. The battery 22 also supplies power to the detector 5 and the alert tone generating circuit 10 through the switch 23, and to the reset terminal of the flipflop 17 by way of the switch 23 and a differentiating circuit consisting of a capacitor 24 and a resistor 25.

Referring now to FIG. 2A, a paging signal includes a preamble signal P, and a call signal including an address signal A and an end-mark signal E. In this particular example, the preamble signal P comprises 38 words (5.89 sec); the address signal A, a maximum of 80 words (12.4 sec); and the end-mark signal E, 6 words (0.93 sec).

In FIG. 2B, for each of the unique words constituting the preamble signal P are assigned 31 bits of 155 msec. The preamble signal P is

intended for temporarily suspending the battery saving operation so that the signals following the preamble signal can be received. In FIG. 2C, for each of the address words constituting the address signal A are also assigned 31 bits of 155 msec. In FIG. 2D, for each word of the end-mark signal E are assigned 31 bits of 155 msec, and the end-mark signal E itself is made up of the repetition of alternating all "0" and all "1" words. The specified digital-pattern signal for test, which is a feature of the present invention, has 31 bits per word, as shown in FIG. 2E. As will be described in detail below, the receiver will suspend or mute its battery saving function upon receipt of this specified digital-pattern signal, thereby placing the receiver in condition for test operation. In such test operation condition, the receiver can be tested and readjusted.

FIGS. 3A to 3F are time charts showing waveforms at various points of FIG. 1 when the receiver is in a normal receiving operation. Referring to FIGS. 1 and 3A to 3F, the antenna 1 receives a carrier wave modulated with a paging signal having the format of FIG. 3A and supplies the carrier to the receiver section 2, which demodulates it to provide a demodulated paging signal. The demodulated signal is supplied via the waveform shaping circuit 3 to the identity detecting section 6, the bit synchronizing circuit 7 and the 31-bit shift register 8, all in the decoder 5. During the normal operation of the receiver, the decoder 5 intermittently supplies power to both the receiver section 2 and the waveform shaping circuit 3 by controlling the switching

transistor 21. The switching transistor is turned on by a signal provided from the oscillation circuit 20 via the NOR gate 18 in the cycle shown in FIG. 3B. If the preamble signal P is detected while power is supplied, the decoder 5 will continue to supply power to the receiver section 2 and the waveform shaping circuit 3 through the NOR gate 18 for a duration needed for the detection of the following call signal (usually about 20 sec), irrespective of the cycle of FIG. 3B, as shown in FIG. 3C, thereby enabling the reception of the address signal A coming in next.

In this paging receiver, the source of clock pulses needed for processing digital signals at the decoder 5 consists of the bit synchronizing circuit 7 adapted to receive signals from the waveforms shaping circuit 3. The preamble signal P serves as the frame synchronization signal of the address signal A. When receiving the call signal, the decoder 5 sequentially reads out the contents of the PROM 9 in which the paging number of the receiver is written. The identity detecting section 6 compares the demodulated call signal (FIG. 3A) with the read-out contents and, upon detection of coincidence, provides a pulse representing the detection of a desired signal D, as shown in FIG. 3F. The pulse so generated actuates the alert tone generating circuit 10. The annunciator 11 is thereby sounded to let the holder of the receiver know that a desired signal has been received. Then, the receiver under power supply again shifts to the battery saving operation upon detection of the end-mark signal E, as shown in FIG. 3C.

FIGS. 4A to 4F are time charts showing waveforms at the points of FIG. 1 like FIGS. 3A to 3F, but these charts in particular refer to the reception of the specified digital-pattern signal for test shown in FIG. 2E. The specified digital-pattern signal may be given from
5 a code generator which is also able to generate codes for the preamble, address and end-mark signals. Reception of this specified digital-pattern signal results in suspension of the battery saving function to permit, for instance, the readjustment of the high frequency section or the measurement of the local oscillation frequency by temperature
10 test or otherwise. The receiver intermittently receiving signals in the cycle of FIG. 4B, upon receipt of the preamble signal P of FIG. 4A, suspends the battery saving function for a long enough period to receive the ensuing call signals. The number of the received call signal is compared with an identification number assigned to the receiver and
15 stored in the PROM 9.

At the same time, the specified digital-pattern signal SP of FIG. 4A is monitored by the shift register 8, the inverters 12 to 15 and the AND gate 16. If the specified signal is detected, the flipflop 17 is set and, irrespective of the control signals shown in FIGS. 4B
20 and 4C, the output of the flip-flop 17 shown in FIG. 4D causes power from the battery 22 to be indefinitely supply through the NOR gate 18 and the switching transistor 21 to the receiver section 2 and the waveform shaping circuit 3, as shown in FIG. 4D. This power supply enables the pertinent parts of the receiver to be subjected to readjustment,

measurement or the like. Incidentally, return to the battery saving operation is achieved by the presetting of the switch 23.

If there is provided a timer having a prescribed length of time in which to respond to the output of the flipflop 17 and its output is
5 connected to the reset terminal of the flipflop 17, the battery saving function can be automatically restored in the prescribed length of time. The oscillation circuit 20 can be composed of an astable.
multivibrator using a transistor or a CR oscillation circuit. As the
switching transistor 21 can be used a bipolar type transistor, an FET,
10 an SCR or the like. Further, the PROM 9 can consist of a diode
matrix or a transistor matrix, such as μ PB-487R manufactured and
marketed by Nippon Electric Co., Ltd. As the decoder 5 can be
employed a low voltage single-chip CPU (for instance, μ PD 7502G
manufactured and marketed by NEC). Next will be described the
15 operation of a receiver wherein this single-chip CPU is used.

Referring to FIG. 5, a sequence of instructions to be executed is stored in a program memory 31, from which contents at an address designated by a program counter 32 are delivered to an instruction decoder 33. The instruction decoder decodes the instructions so
20 delivered to supply control signals corresponding to them to various sections in the decoder 5. The program counter 32 is usually set to "+1" after instruction is delivered from the program memory 31 to the instruction decoder 33, but its count contents are altered by a branching command, a jumping command or the like, so that instructions according

to these commands are successively executed.

An arithmetic-logic unit (ALU) 34 is a circuit for effecting various operations including arithmetic operations and logic operations; a random access memory (RAM) 42 is used for the storage of processed data, and the standby or the program counter or the program status during a subroutine or an interruption; and an accumulator 35 is employed for storing the results of operation by the ALU 34 or the exchange of data between the RAM 42 and ports 36 to 41. A data bus 43 is a signal line for the exchange of data between different sections. The ports 37, 39 and 40 are output ports for giving signals on the data bus 43 to circuits exterior to the decoder 5, and have a latching function. The ports 36, 38 and 41 are input ports for delivering signals from circuits exterior to the decoder 5 to the data bus 43. An interruption control circuit 44 has a function to deliver internal interruption signals to the data bus 43.

Hereupon, the functioning of the circuit illustrated in FIG. 5 will be described with reference to FIGS. 4A to 4F. When a battery saving control signal is supplied from the output port 37 in the stroke shown in FIG. 4B, the decoder 5 waits for the reception of the preamble signal P. When a paging signal of FIG. 4A is provided through the input port 36, the decoder 5, will be judging with its ALU 34 whether or not the paging signal is a preamble signal. Upon reception of the preamble signal, the output port 37 is kept in the state of "L" so that power is continuously supplied to the receiver for a first predetermined

period of time (about 20 sec in this embodiment). This first time period is necessary and sufficient for receiving the call signal which is to come in following the preamble signal P. With the ALU 34, the received call signal is compared with the receiver's identification number signal stored in the PROM 9 which is addressed through the output port 40 and provides its contents through the input port 41. At the same time, the received call signal is also compared with a specified digital-pattern pattern signal for test which relieves the battery saving function and, with an end-mark signal, both being written into the RAM 42.

Thus, if the specified digital-pattern pattern signal SP (FIG. 4A) for test is detected within the first predetermined time period, no return to the battery saving operation will take place even after the lapse of the first predetermined time period, but only after the lapse of a second predetermined time period (about 5 minutes in this embodiment) started by the detection of the specified digital-pattern for test. Thus, after the lapse of five minutes, a control signal from the interruption control circuit 44 restores the battery saving function.

If the desired address signal (D) is detected within the first predetermined time period, the decoder 5 will drive the alert tone generating circuit 10 via the output port 39 to sound the annunciator 11 to let the receiver holder know that he or she is being paged. Then the detection of the end-mark signal E will restore the battery saving function. Obviously, the use of a switch is also conceivable

to return the receiver, which is kept receiving continuous power supply by the detection of the specified digital-pattern for test, to the battery saving operation. The switch for this purpose can primarily comprise, as shown by broken block 50 in FIG. 5, a resistor 51 and a push
5 switch 52 which are coupled to the interruption control circuit 44.

The operation of the single-chip CPU hitherto described can be represented by the flow chart of FIG. 6. First, when the power supply of the receiver is turned on at Step 100, the CPU is initialized at Step 101. At the same time, the normal mode battery saving operation
10 is started, and as long as power is supplied to the receiver section at Step 102, the preamble signal is sought (Step 103). If 0.62 second has lapsed without the preamble signal being detected, as shown at Steps 104 to 106, power supply to the receiver section and the waveform shaping circuit is interrupted and, after the lapse of another time
15 period of 4.96 seconds, a return to Step 102 takes place to restore power supply.

Meanwhile, if the detection of the preamble signal is confirmed while power is being supplied, the process shifts to Step 107 and further to Step 108 to actuate the 20-sec timer and
20 to synchronize the frame phase in preparation for the detection of the desired address signal and the end-mark signal or the specified digital-signal, which follows the preamble signal. Upon reception of the desired address signal at Step 109, the process moves to Step 110 to give a positive pulse via
25 the output port 39 to the alert tone generating circuit 10 to activate it.

As a result of this activation, the holder of the receiver can hear an alarm from the annunciator 11. If, after the detection of the desired address signal, either the 20-sec timer counts out or the end-mark signal is detected, power supply is interrupted for a return to the battery saving operation (see Steps 111 and 113).

If, at Step 113, the specified digital-signal for suspending the battery saving function is detected before the 20-sec timer counts out, the process shifts from Step 112 to a test mode of either Route A or Route B. If Route A is taken, a 5-min timer is started at Step 114, and power is continuously supplied until this timer counts out. If, on the other hand, Route B is followed, power is continuously supplied until a control signal is provided from the external switch 50 shown in Fig. 5 (Step 116). After the execution of Step 115 or 116, the receiver will resume its normal battery saving operation.

As hitherto described, the paging receiver is supplied with a specified digital-pattern signal for test as required and, with a circuit to detect this specified digital-pattern signal. With detection of the specified digital-pattern signal, the receiver of the present invention makes it possible to automatically suspend the battery saving function. Therefore, if the receiver is mounted in a case or the like, there is no need to remove it from the case and connect or disconnect its strap or the like every time its electrical characteristics or the like are to be tested. It is easily understood from the foregoing that the feature of the present invention can be also _____

adapted to the paging receiver capable of receiving a tone signal and a specified tone-pattern signal.



64

- 14 -

Claims:

1. A radio paging receiver comprising battery saving means for intermittently supplying power to some or all of its circuits at least while signals addressed thereto are being received; detecting means for detecting a specified signal for test from received signals;
5 and means for continuously supplying power to some or all of its circuits by suspending the operation of said battery saving means in response to the output of said detecting means, thereby placing the receiver in condition for test operation.
2. A radio paging receiver comprising:
a receiver section for receiving and demodulating a carrier modulated with a preamble signal, a specified signal for test, and a call signal including an address signal;
5 means for storing in advance an identification number assigned to said radio paging receiver;
means for detecting said preamble signal from the output of said receiver section to provide a preamble detection signal;
identity detecting means for comparing said address signal supplied
10 from said receiver section and an output read out of said storing means and, upon detection of their coincidence, supplying an identity signal;
means for generating an alert signal in response to said identity signal;



15 battery saving means for supplying power from a battery to said receiver section either intermittently in a prescribed cycle so that said receiver section can receive at least said preamble signal or for a prescribed period of time so that said receiver section can receive said address signal in response to said preamble detection
20 signal;
specified signal detecting means for detecting said specified signal from the output of said receiver section and supplying a signal to suspend battery saving; and
battery saving suspending means for muting said battery saving
25 means in response to said signal to suspend battery saving and continuously supplying said power to said receiver section, thereby placing the receiver in condition for test operation.

3. A radio paging receiver as claimed in Claim 2, wherein said call signal further contains an end-mark signal after said address signal, and said receiver further comprises: means for detecting said end-mark signal from the output of said receiver section to provide
5 a battery saving restoration signal; and battery saving restoring means for inhibiting said battery saving suspending means and reactivating said battery saving means in response to said battery saving restoration signal.

4. A radio paging receiver as claimed in Claim 2 or 3 further comprising means connected to said battery for presetting said battery saving suspending means.



66

- 16 -

5. A radio paging receiver as claimed in any one of Claims 2 to 4, wherein said call signal and said specified signal are digital signals.

6. A radio paging receiver as claimed in Claim 5 further comprising synchronization means responsive to said preamble signal supplied from said receiver section for supplying synchronization pulses to said identity detecting means, specified signal detecting means and end-mark detecting means.

7. A radio paging receiver as claimed in Claim 2 or 3, wherein said identity detecting means, battery saving means, specified signal detecting means, battery saving suspending means and battery saving restoring means are incorporated into a single-chip integrated circuit.

8. A radio paging receiver substantially as described herein with reference to Figures 1, 2A to 2E, 3A to 3F, and 4A to 4F, or Figures 5 and 6 of the accompanying drawings.
