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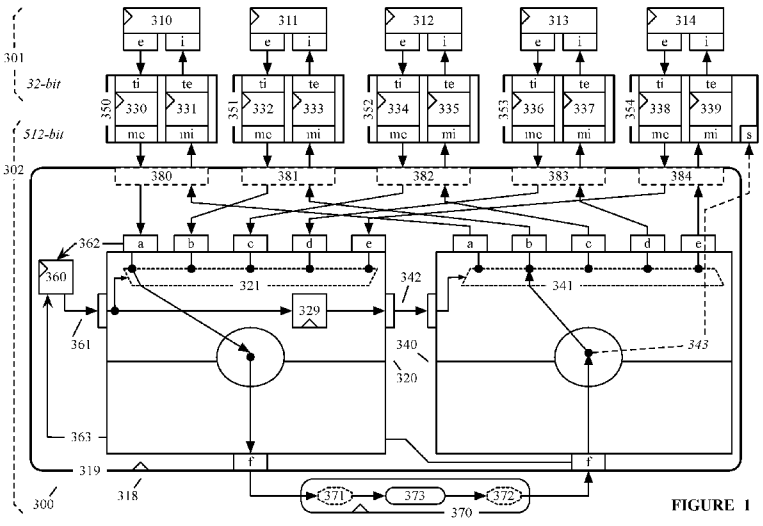

FIGURE 1

(57) Abstract: A shared memory computing architecture (300) has M interconnect masters (350, 351, 352, 353, 354), one interconnect target (370), and a timeslot based interconnect (319). The interconnect (319) has a unidirectional timeslot based interconnect (320) to transport memory transfer requests with T timeslots and a unidirectional timeslot based interconnect (340) to transport memory transfer responses with R timeslots. For each of the R timeslots, that timeslot: corresponds to one memory transfer request timeslot and starts at least L clock cycles after the start time of that corresponding memory request timeslot. The value of L is >= 3 and < T. Interconnect target (370) is connected to interconnect (319). Each interconnect master (350, 351, 352, 353, 354) is connected to interconnect (319).

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