of the semiconductor wafer to provide a density charge trap and, thereby, inhibit the formation of the high conductivity inversion or accumulation layer. For example, the layer can be deposited onto a surface that forms the interface between the high resistivity substrate and a buried oxide (BOX) to hinder the movement of charges across the interface.

[0005] The effectiveness of charge trapping in semiconductor structures depends on multiple factors including the density of crystal defects, polysilicon structure (grain size), polysilicon deposition [CVD] conditions, status of the polysilicon to silicon substrate interface, doping level, resistivity, interface states, surface contamination and thermal treatment applied during device manufacturing. To ensure a proper charge trapping efficiency, a great variety of technological parameters are carefully controlled and monitored during manufacturing of charge-trapping layer semiconductor wafers for RF device applications. A measurement of charge trapping efficiency is an important component in quality control in charge-trapping layer semiconductor structure manufacturing.

[0006] Conventional methods of measuring charge trapping efficiency in semiconductor wafers are based on testing radiofrequency (RF) device performance. RF devices are built on top of the wafers and then tested. The process of RF device manufacturing involves many technological steps and is time consuming. Feedback on the quality of the wafer processing is delayed and this may incur significant throughput and yield losses in wafer manufacturing.