

What is claimed is:

1. A semiconductor package comprising:

a first layer comprising a first panel of the semiconductor package and one or more first semiconductor chips, each of the one or more first semiconductor chips having one or more first pads exposed at a first surface of the one or more first semiconductor chips;

a second layer disposed over the first layer, the second layer comprising a second panel of the semiconductor package and one or more second semiconductor chips, each of the one or more second semiconductor chips having one or more second pads exposed at a second surface of the one or more second semiconductor chips; and

a first redistribution layer interposed between the first layer and the second layer and electrically connected to the one or more first pads,

wherein the first layer further comprises one or more first through panel vias (TPVs) extending through the first panel in a vertical direction, corresponding to a direction of thickness of the first panel, and electrically connected to the first redistribution layer,

wherein the one or more first semiconductor chips and the one or more second semiconductor chips are disposed such that the first surface and the second surface face each other across the first redistribution layer, and

wherein the one or more second pads are electrically connected to the first redistribution layer, and wherein the one or more second pads have one or more protrusions protruding toward the first redistribution layer, and

the first redistribution layer has one or more grooves receiving the one or more protrusions.

2. The semiconductor package of claim 1, wherein the first panel has one or more cavities therein accommodating the one or more first semiconductor chips, and the second panel having one or more cavities therein accommodating the one or more second semiconductor chips.

3. The semiconductor package of claim 1, further comprising one or more bumps interposed between the one or more second pads and the first redistribution layer, and wherein the one or more second pads and the first redistribution layer are electrically connected to each other through the one or more bumps.

4. The semiconductor package of claim 1, wherein the first layer comprises one or more through silicon vias (TSVs) extending in the vertical direction from the one or more first pads through a remainder of the one or more first semiconductor chips.

5. The semiconductor package of claim 4, wherein a height of the one or more first semiconductor chips in the vertical direction is equal to a height of the first layer in the vertical direction.

6. The semiconductor package of claim 1, wherein the second layer comprises one or more second TPVs extending through the second panel in the vertical direction and electrically connected to the first redistribution layer.

7. The semiconductor package of claim 6, further comprising a second redistribution layer stacked on the second layer, wherein the one or more second pads and the one or more second TPVs are electrically connected to the second redistribution layer.

8. The semiconductor package of claim 6, further comprising one or more bumps interposed between the one or more second TPVs and the first redistribution layer, and

wherein the one or more second TPVs and the first redistribution layer are electrically connected to each other through the one or more bumps.

9. The semiconductor package of claim 6, wherein the one or more second TPVs have one or more protrusions protruding toward the first redistribution layer, and the first redistribution layer has one or more grooves receiving the one or more protrusions.

10. A semiconductor package comprising:
a first layer comprising a first semiconductor chip having one or more first pads exposed at a first surface of the first semiconductor chip, a first panel having a first accommodating portion accommodating the first semiconductor chip, and one or more first through panel vias (TPVs) extending through the first panel in a vertical direction corresponding to a direction of thickness of the first panel;
a first redistribution layer disposed on the first layer in the vertical direction and electrically connected to the one or more first pads and the one or more first TPVs; and

a second layer stacked in the vertical direction on the first redistribution layer and including a second semiconductor chip having one or more second pads exposed at a second surface of the second semiconductor chip, and a second panel including a second accommodating portion accommodating the second semiconductor chip, wherein the first accommodating portion and the second accommodating portion are disposed symmetrically with respect to the first redistribution layer,

the one or more second pads are electrically connected to the first redistribution layer, and

wherein the one or more second pads have one or more protrusions protruding toward the first redistribution layer, and

the first redistribution layer has one or more grooves receiving the one or more protrusions.

11. The semiconductor package of claim 10, wherein the first layer comprises one or more through silicon vias (TSVs) extending in the vertical direction from the one or more first pads through a body of the first semiconductor chip, and

the second layer comprises one or more through silicon vias (TSVs) extending in the vertical direction from the one or more second pads and through a body of the second semiconductor chip.

12. The semiconductor package of claim 11, wherein the first accommodating portion has a height equal to a thickness of the first panel in the vertical direction.

13. The semiconductor package of claim 10, wherein the second layer comprises one or more second TPVs extending the second panel in the vertical direction,

further comprising a second redistribution layer disposed on the second layer and electrically connected to the one or more second TPVs.

14. A semiconductor package comprising:

a first panel having opposite sides and one or more chip accommodating portions therein, each of the one or more chip accommodating portions open at one of the opposite sides of the first panel;

a respective first semiconductor chip received in each of the one or more chip accommodating portions, the first semiconductor chip having a surface exposed at said one of the opposite sides of the first panel;

a redistribution layer (RDL) comprising a wiring pattern extending along said one of the opposite sides of the first panel and over the surface of the first semiconductor chip, the wiring pattern of the RDL being electrically connected to the first semiconductor chip at said surface of the first semiconductor chip;

a through panel via (TPV) extending vertically through the first panel from one of the opposite sides thereof to the other of the opposite sides thereof, the wiring pattern of the RDL extending over and electrically connected to the TPV;

a second panel disposed directly on the RDL and having one or more chip accommodating portions therein, each of the one or more chip accommodating portions of the second panel open at one of the opposite sides of the second panel; and

a respective second semiconductor chip received in each of the one or more chip accommodating portions of the second panel, the second semiconductor chip having a surface exposed at said one of the opposite sides of the second panel,;

wherein the second semiconductor chip is electrically connected to the wiring pattern of the RDL, the second semiconductor chip has one or more second pads exposed at the second

surface of the second semiconductor chip, wherein the one or more second pads are electrically connected to the RDL, and wherein the one or more second pads have one or more protrusions protruding toward the RDL, and the RDL has one or more grooves receiving the one or more protrusions.

15. The semiconductor package of claim 14, wherein the RDL is a first RDL, said one of the opposite sides of the second panel faces away from the RDL, and the second semiconductor chip has a thickness less than a thickness of the second panel, and further comprising:

a second RDL comprising a wiring pattern extending along said one of the opposite sides of the second panel and over the surface of the second semiconductor chip exposed at said one of the opposite sides of the second panel, the wiring pattern of the second RDL being electrically connected to the second semiconductor chip at said surface of the second semiconductor chip; and

a second TPV extending vertically through the second panel between and electrically connected to the wiring pattern of each of said first and second RDLs.