

processing method and device for quasi-cyclic LDPC coding, which is able to improve adaptability and flexibility of the quasi-cyclic LDPC coding.

In a first aspect, the present disclosure provides a processing method for quasi-cyclic low density parity check (LDPC) coding, comprising: determining, according to a data feature of an information bit sequence to be encoded, one or more characteristics of the quasi-cyclic LDPC coding and a base matrix to perform the quasi-cyclic LDPC coding wherein the one or more characteristics includes a maximum number of systematic columns used for the quasi-cyclic LDPC coding, and wherein the maximum number of systematic columns used for the quasi-cyclic LDPC coding is a difference between a total number of columns and a total number of rows of the base matrix of the quasi-cyclic LDPC coding; and performing, according to the one or more characteristics and based on a the base matrix and a lifting size, the quasi-cyclic LDPC coding.

In a second aspect, the present disclosure provides a processing device for quasi-cyclic low density parity check (LDPC) coding, comprising: a processor configured to: determine, according to a data feature of an information bit sequence to be encoded, one or more characteristics of the quasi-cyclic LDPC coding and a base matrix to perform the quasi-cyclic LDPC coding, wherein the one or more characteristics includes a maximum number of systematic columns used for the quasi-cyclic LDPC coding, wherein the maximum number of systematic columns used for the quasi-cyclic LDPC coding is a difference between a total number of columns and a total number of rows of the base matrix of the quasi-cyclic LDPC coding; and perform, according to the one or more characteristics and based on a the base matrix and a lifting size, the quasi-cyclic LDPC coding.

In a third aspect, the present disclosure provides a device for quasi-cyclic low density parity check (LDPC) coding, comprising: a processor configured to: determine, based on a length of an information bit sequence to be encoded and a modulation and coding scheme (MCS) index of the information bit sequence, a maximum information length supported by the quasi-cyclic LDPC coding and a difference between a total number of columns and a total number of rows of a base matrix; and perform, based on the difference, the maximum information length, and a lifting size, the quasi-cyclic LDPC coding.

In a fourth aspect, the present disclosure provides a method for quasi-cyclic low density parity check (LDPC) coding, comprising: determining, based on a length of an information bit sequence to be encoded and a modulation and coding scheme (MCS) index of the information bit sequence, a maximum information length supported by the quasi-cyclic LDPC coding and a

difference between a total number of columns and a total number of rows of a base matrix; and performing, based on the difference, the maximum information length, and a lifting size, the quasi-cyclic LDPC coding.

An embodiment of the present disclosure provides a processing method for quasi-cyclic LDPC coding. The method includes:

determining, according to a data feature of an information bit sequence to be encoded, a processing strategy for the quasi-cyclic LDPC coding; and

performing, according to the processing strategy and based on a base matrix and a lifting size, the quasi-cyclic LDPC coding and rate matching output on the information bit sequence.

An embodiment of the present disclosure provides a processing device for quasi-cyclic LDPC coding. The device includes:

a processing module, which is configured to determine, according to a data feature of an information bit sequence to be encoded, a processing strategy for the quasi-cyclic LDPC coding and perform, according to the processing strategy and based on a base matrix and a lifting size, the quasi-cyclic LDPC coding and rate matching output on the information bit sequence; and

a storage module, which is configured to store the base matrix and the lifting size.

Compared with the related art, the embodiments of the present disclosure provide a processing method and device for quasi-cyclic LDPC coding. According to a data feature of an information bit sequence to be encoded, a processing strategy for the quasi-cyclic LDPC coding is determined. According to the processing strategy and based on a base matrix and a lifting size, the quasi-cyclic LDPC coding and rate matching output are performed on the information bit sequence. Technical solutions of the embodiments of the present disclosure are able to improve adaptability and flexibility of the quasi-cyclic LDPC coding.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of a digital communication system in the related art;

FIG. 2 is a flowchart of a method for processing quasi-cyclic LDPC coding according to

WHAT IS CLAIMED IS:

1. A processing method for quasi-cyclic low density parity check (LDPC) coding, comprising:

determining, according to a data feature of an information bit sequence to be encoded, one or more characteristics of the quasi-cyclic LDPC coding and a base matrix to perform the quasi-cyclic LDPC coding

wherein the one or more characteristics includes a maximum number of systematic columns used for the quasi-cyclic LDPC coding, and

wherein the maximum number of systematic columns used for the quasi-cyclic LDPC coding is a difference between a total number of columns and a total number of rows of the base matrix of the quasi-cyclic LDPC coding; and

performing, according to the one or more characteristics and based on the base matrix and a lifting size, the quasi-cyclic LDPC coding.

2. The processing method of claim 1, wherein the data feature comprises a length of the information bit sequence or a modulation and coding scheme (MCS) index of the information bit sequence.

3. The processing method of claim 1, wherein determining the one or more characteristics to perform for the quasi-cyclic LDPC coding comprises determining a maximum number of systematic columns of the base matrix, a minimum code rate of the base matrix at a maximum length of the information bit sequence, or a maximum information length supported by the quasi-cyclic LDPC coding.

4. The processing method of claim 3, wherein the maximum number of systematic columns of the base matrix is selected from at least two integer values greater than or equal to 2 and less than or equal to 32.

5. The processing method of claim 3, wherein the minimum code rate of the base matrix at the maximum length of the information bit sequence is either $1/5$ or $1/3$.

6. The processing method of claim 3, wherein the maximum information length supported by the quasi-cyclic LDPC coding is equal to the maximum number of systematic columns of the

base matrix times a maximum lifting size.

7. A processing device for quasi-cyclic low density parity check (LDPC) coding, comprising:

a processor configured to:

determine, according to a data feature of an information bit sequence to be encoded, one or more characteristics of the quasi-cyclic LDPC coding and a base matrix to perform the quasi-cyclic LDPC coding,

wherein the one or more characteristics includes a maximum number of systematic columns used for the quasi-cyclic LDPC coding,

wherein the maximum number of systematic columns used for the quasi-cyclic LDPC coding is a difference between a total number of columns and a total number of rows of the base matrix of the quasi-cyclic LDPC coding; and

perform, according to the one or more characteristics and based on the base matrix and a lifting size, the quasi-cyclic LDPC coding.

8. The processing device of claim 7, wherein the data feature comprises a length of the information bit sequence and a modulation or coding scheme (MCS) index of the information bit sequence.

9. The processing device of claim 7, wherein the processor is configured to perform the determine the one or more characteristics to perform for the quasi-cyclic LDPC coding by being configured to:

determine a maximum number of systematic columns of the base matrix, a minimum code rate of the base matrix at a maximum length of the information bit sequence, or a maximum information length supported by the quasi-cyclic LDPC coding.

10. The processing device of claim 9, wherein the maximum number of systematic columns of the base matrix is selected from at least two integer values greater than or equal to 2 and less than or equal to 32.

11. The processing device of claim 9, wherein the minimum code rate of the base matrix at the maximum length of the information bit sequence is either $1/5$ or $1/3$.

12. The processing device of claim 9, wherein the maximum information length supported by the quasi-cyclic LDPC coding is equal to the maximum number of systematic columns of the base matrix times a maximum lifting size.
13. A device for quasi-cyclic low density parity check (LDPC) coding, comprising:
a processor configured to:
determine, based on a length of an information bit sequence to be encoded and a modulation and coding scheme (MCS) index of the information bit sequence, a maximum information length supported by the quasi-cyclic LDPC coding and a difference between a total number of columns and a total number of rows of a base matrix; and
perform, based on the difference, the maximum information length, and a lifting size, the quasi-cyclic LDPC coding.
14. The device of claim 13, wherein the maximum information length supported by the quasi-cyclic LDPC coding is equal to a product of a maximum number of systematic columns of the base matrix and a maximum lifting size.
15. The device of claim 13, wherein a minimum code rate of the base matrix at the maximum length of the information bit sequence is either $1/5$ or $1/3$.
16. A method for quasi-cyclic low density parity check (LDPC) coding, comprising:
determining, based on a length of an information bit sequence to be encoded and a modulation and coding scheme (MCS) index of the information bit sequence, a maximum information length supported by the quasi-cyclic LDPC coding and a difference between a total number of columns and a total number of rows of a base matrix; and
performing, based on the difference, the maximum information length, and a lifting size, the quasi-cyclic LDPC coding.
17. The method of claim 16, wherein the maximum information length supported by the quasi-cyclic LDPC coding is equal to a product of a maximum number of systematic columns of the base matrix and a maximum lifting size.
18. The method of claim 16, wherein a minimum code rate of the base matrix at the maximum length of the information bit sequence is either $1/5$ or $1/3$.