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(21) International Application Number: PCT/US99/09672 (22) International Filing Date: 3 May 1999 (03.05.99) (30) Priority Data: 09/096,283 11 June 1998 (11.06.98) US (71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): ALLEN, Michael, J. [US/US]; 3161 Pinchem Creek Drive, Rescue, CA 95672 (US). (74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report.
(54) Title: A STRESS-FOLLOWER CIRCUIT CONFIGURATION (57) Abstract Briefly, in accordance with one embodiment of the invention, an integrated circuit (IC) includes: a stress-follower circuit configuration (100). The stress-follower circuit (110) of the configuration is coupled to a pad (150) of the integrated circuit. The stress-follower circuit configuration is coupled so as to reduce the voltage stress on the gate of a transistor in the stack tolerates an operating voltage approximately 1.5 volts above its nominal voltage. The transistor stack (120, 130) is also coupled to the pad.		