CLAIMS

1. A semiconductor structure, comprising:

a substrate having a plurality of active areas close to a surface of the substrate;

a gate structure located in a first structure layer on the substrate, the gate structure and the active areas forming a selective transistor; and

an anti-fuse bit structure located in a second structure layer on the first structure layer, and being connected with an active area of one selective transistor through a first connecting structure, a breakdown state and a non-breakdown state of the anti-fuse bit structure representing different stored data;

wherein the anti-fuse bit structure comprises:

a first electrode connected to the active area through the first connecting structure;

a second electrode located in a same plane with the first electrode, the plane where the first electrode and the second electrode are located being parallel to the surface of the substrate; and

an anti-fuse bit dielectric layer located between the first electrode and the second electrode and connected with the first electrode and the second electrode, wherein the breakdown state is a state in which the anti-fuse bit dielectric layer is broken down, and the non-breakdown state is a state in which the anti-fuse bit dielectric layer is not broken down.

2. The semiconductor structure of claim 1, wherein the second electrodes of a plurality of anti-fuse bit structures located in an extension direction parallel to the gate structure connected with each other.

3. The semiconductor structure of claim 1, wherein a side of the first electrode close to the second electrode has a convex structure, and a side of the second electrode close to the first electrode has a concave structure corresponding to the convex structure.

4. The semiconductor structure of claim 1, wherein a projection of the anti-fuse bit structure on the substrate at least partially overlaps a projection of the gate structure on the substrate.

5. The semiconductor structure of claim 1, wherein the first structure layer further comprises a first isolation layer surrounding at least a bottom surface and side surfaces of a gate electrode of the gate structure; and

the second structure layer further comprises a second isolation layer surrounding at least a bottom surface and side surfaces of the anti-fuse bit structure, and the first connecting structure penetrates the first isolation layer and the second isolation layer.

6. The semiconductor structure of claim 5, wherein the first isolation layer is an oxide material, wherein a part of the first isolation layer in the gate structure serves as a gate dielectric of the selective transistor.

7. The semiconductor structure of claim 1, wherein the active area comprises:

a first doped region and a second doped region which are of a same doping type, the first doped region and the second doped region being respectively located at two sides of the gate structure; wherein,

the first doped region is connected with the anti-fuse bit structure through the first connecting structure.

8. The semiconductor structure of claim 7, further comprising:

a first metal line located in a third structure layer above the second structure layer; wherein the first metal line is connected with the second doped region through a second connecting structure, an extension direction of the first metal line is perpendicular to an extension direction of the gate structure.

9. The semiconductor structure of claim 8, wherein the third structure layer further comprises a third isolation layer surrounding at least a bottom surface and side surfaces of the first metal line.

10. The semiconductor structure of claim 7, wherein two adjacent ones of the anti-fuse bit structures are symmetrically arranged, and the two selective transistors connected to the two adjacent anti-fuse bit structures symmetrically arranged share a same second doped region.

11. The semiconductor structure of claim 10, further comprising:

an isolation structure located between two adjacent ones of the first doped regions, wherein, the two adjacent first doped regions are the first doped regions corresponding to two adjacent selective transistors that do not share the second doped region.

12. A method for manufacturing a semiconductor structure, comprising:

providing a substrate having a plurality of active areas close to a surface of the substrate;

forming a first structure layer comprising a gate structure on the substrate, the gate structure and the active areas constituting a selective transistor; and

forming a second structure layer comprising an anti-fuse bit structure on the first structure layer, and forming a first connecting structure connecting the anti-fuse bit structure and an active area of the selective transistor, a breakdown state and a non-breakdown state of the anti-fuse bit structure representing different stored data;

wherein forming the second structure layer comprising an anti-fuse bit structure on the first structure layer and forming the first connecting structure connecting the anti-fuse bit structure and the active area of the selective transistor comprises:

depositing an insulating material on the first structure layer, the insulating material being used for forming a second isolation layer in the second structure layer;

forming a first trench and a second trench in the insulating material, and forming a first connecting hole in the first trench, penetrating the first structure layer;

filling a conductive material in the first connecting hole to form the first connecting structure; and

filling a conductive material in the first trench and the second trench to form a first electrode and a second electrode, respectively. the insulating material at a location other than the first electrode and the second electrode serving as the second isolation layer, part of the

second isolation layer between the first electrode and the second electrode serving as an anti-fuse bit dielectric layer of the anti-fuse bit structure, wherein the breakdown state is a state in which the anti-fuse bit dielectric layer is broken down, and the non-breakdown state is a state in which the anti-fuse bit dielectric layer is not broken down.

13. The method according to claim 12, wherein an extension direction of the first trench and the second trench are parallel to an extension direction of the gate structure.

14. The method according to claim 13, wherein filling the conductive material in the first trench and the second trench to form the first electrode and the second electrode, respectively comprises:

filling the conductive material in the first trench and the second trench; and

removing at least part of the conductive material in the first trench to form a plurality of the first electrodes separated from each other and the second electrodes of a plurality of the anti-fuse bit structures in a same line parallel to an extension direction of the gate structure connected with each other.

15. A method for operating a memory comprising the semiconductor structure according to claim 8 or 9, comprising

breaking down a target anti-fuse bit structure in the anti-fuse bit structures of the memory according to data to be written to convert the target anti-fuse bit structure from a non-breakdown state to a breakdown state; and

maintaining a non-breakdown state of a non-target anti-fuse bit structure, wherein the non-target anti-fuse bit structure is an anti-fuse bit structure other than the target anti-fuse bit structure.

16. The method according to claim 15, wherein breaking down the target anti-fuse bit structure in the anti-fuse bit structures of the memory to convert the target anti-fuse bit structure from a non-breakdown state to a breakdown state comprises:

applying a first voltage to the gate structure of the selective transistor to which the

target anti-fuse bit structure is connected to turn on the selective transistor;

applying a second voltage to the first metal line to which the selective transistor is connected; and

applying a third voltage to the second electrode of the target anti-fuse bit structure to convert the target anti-fuse bit structure from the non-breakdown state to the breakdown state, wherein a voltage difference between the second voltage and the third voltage is greater than or equal to a breakdown voltage of the anti-fuse bit structure.

17. The method of claim 15, wherein,

maintaining the non-breakdown state of the non-target anti-fuse bit structure comprises:

applying a first voltage to the gate structure of the selective transistor to which the non-target anti-fuse bit structure is connected to turn on the selective transistor;

applying a fourth voltage to the first metal line to which the selective transistor is connected; and

applying a third voltage to the second electrode of the non-target anti-fuse bit structure to maintaining the non-breakdown state of the non-target anti-fuse bit structure, wherein a voltage difference between the fourth voltage and the third voltage is smaller than the breakdown voltage of the anti-fuse bit structure,

alternatively, maintaining the non-breakdown state of the non-target anti-fuse bit structure comprises:

applying a fifth voltage to the gate structure of the selective transistor to which the non-target anti-fuse bit structure is connected to turn off the selective transistor, and the non-target anti-fuse bit structure maintains in the non-breakdown state.

18. A memory, comprising:

a memory array comprising the semiconductor structure according to any one of claims 1 to 11; and

a peripheral circuit coupled to the memory array.