MULTIPLE CHIP SEMICONDUCTOR PACKAGE AND METHOD OF FABRICATING SAME

TECHNICAL FIELD

The present invention relates generally to semiconductor packaging. More particularly, the present invention relates to wafer level multichip packaging such as, for example, a system in a package solution.

BACKGROUND

State of the Art: Semiconductor dice (also referred to as chips/dice herein) are found in many electronic products today. As semiconductor dice get smaller and more complex, the problem of making electrical connections between semiconductor dice, connections to carrier substrates such as printed circuit boards, and connections to intermediate substrates such as multichip modules which are, in turn, connected to carrier substrates, has been addressed with a variety of constantly evolving solutions.

One of the earlier solutions included wire bonding from signal connection devices, such as bond pads of a semiconductor die, to pins or leads of a lead frame contained in a ceramic or plastic package. Finished packages are mounted to a carrier substrate, such as a printed circuit board, where the pins or leads make electrical connection with contact pads on the carrier substrate.

The term "signal connection devices" as used herein regarding semiconductor devices includes not only contact pads of a substrate and bond pads of a semiconductor device but also I/O connections for a semiconductor device created by adding circuitry from bond pads located on the active surface of the semiconductor device to different locations on the active surface of the semiconductor device. Such additional circuitry is typically effected using a so-called "redistribution layer" extending over the active surface or a surface of a semiconductor die.

An evolution of electrical connection technology occurred when multiple semiconductor dice were mounted on an intermediate substrate. In this instance, the semiconductor dice are typically connected to a lead frame by way of bonding wires. Signals, or electrical connections, required for coupling with an external device, such as a circuit board, are brought out to contact pads, pins or leads of the multichip module

package. Other signals or electrical interconnections may be established between multiple semiconductor dice by way of circuitry formed on the intermediate substrate.

In these solutions, using wires for connecting a semiconductor die to a substrate and wire bonding processes can create problems. Such problems may include, for example, size and pitch (spacing) requirements for the bond pads of the semiconductor die and contact pads of the substrate; inductance in the signals due to the long curved wires; wire bond breakage and wire sweep causing shorting between adjacent wires; and high signal frequency semiconductor dice making the wire bonding process difficult and expensive.

Flip-chip technologies using solder balls or bumps have helped to alleviate some of these problems. For example, instead of wire bonding, conductive bumps such as, for example, balls of solder may be formed at the locations of the bond pads of a semiconductor die. A specialized lead frame, a dielectric tape carrying circuit traces as used in tape automated bonding processes, or other carrier substrates such as a printed wiring board may have electrical connection locations such as terminals which correspond to the placement of the solder balls on the bond pads of the semiconductor die. The semiconductor die is "flipped" upside down so the solder balls are placed, for example, on the contact pads of a carrier substrate. A solder reflow process heats the solder balls until the solder begins to flow and bond with a corresponding contact pad of a carrier substrate. Upon cooling, the solder forms both mechanical and electrical connections between the carrier substrate and the semiconductor die. This packaging solution may alleviate at least some of the inductance problems, allowing for higher frequency performance and better signal integrity of the semiconductor die. Also, to a certain extent, it allows the contact pads of a substrate where bumps were formed to be larger, more widely pitched and placed anywhere on the semiconductor die active surface rather than just around the periphery or down the center thereof.

Chip scale packaging has evolved from various standard flip-chip processes to a configuration wherein the size of a package is reduced to only slightly larger than the size of the semiconductor die. Chip scale packages are typically created using an interposer substrate. The semiconductor die, with solder balls or bumps such as described above, is attached and electrically connected to the interposer substrate and an encapsulation material is applied over the chip for protection thereof from the elements. The interposer substrate can redistribute signal connections to new locations so they are physically

positioned in a desired pattern or arrangement, or to just a different pitch more suitable for mounting to an interposer substrate. An additional set of conductive bumps may then be formed at other contact pad locations on the interposer substrate. The resulting package may then be attached to a carrier substrate such as a printed circuit board.

Chip scale packaging enables small packages using desired ball grid arrays or fine ball grid arrays. However, the interposer substrate is typically made of an organic material which is the same as, or similar to, that used for printed circuit boards. There is conventionally a significant mismatch in the coefficients of thermal expansion (CTE) of the interposer substrate and the semiconductor die, often resulting in substantial stress on the mechanical and electrical interconnections formed between the semiconductor die and interposer substrate (e.g., a reflowed solder connection) during the normal thermal cycling during normal operation of the semiconductor die. The use of a ceramic substrate may alleviate some of the CTE mismatch concerns but at a considerably higher cost relative to more conventional interposer substrates.

Another advance in the area of multichip modules includes wafer scale integration. Wafer scale integration generally comprises fabricating multiple types of functional dice on a single wafer. For example, a four-chip system may be created by placing a microprocessor next to a memory controller and two memory-type semiconductor die. This pattern may then be repeated across the entire wafer. After fabrication, the wafer is sawed into individual segments with each segment containing the four different functions. However, this approach has not been a very satisfactory solution due to yield problems created by the variations in processes for forming processors and various types of memory-type semiconductor dice. For example, if a defect causes any one of the four functions to be inoperable, the entire segment is defective and not usable.

In addition to that described above, there have been advances in bump technologies where the conductive bumps act as the signal connection device. Conventional solder bumps, in some cases, have been replaced by stud bumps. Stud bumps have conventionally been gold, but copper and plated-type stud bumps have also been used recently. The stud bumps may actually comprise short wires or wire stubs applied to a semiconductor die using a conventional wire bonding process. Stud bumping has the advantages of using a more cost effective wire bonding process for application of the bumps in comparison to the more complex, multistep solder bumping process. Further, conductive and conductor-filled adhesives have also been employed to attach the

conductive bumps to a carrier substrate. The conductive or conductor-filled adhesive may provide an amount of flexibility to the mechanical and electrical connection, thereby compensating for some of the problems associated with the mismatch of CTE often associated with solder bump processes as discussed above.

However, in light of the advances made in fabricating semiconductor device packages, there is a continued need for a reliable, cost effective solution with a higher integration of various functional dice in a single package to produce, for example, a system on a chip solution. There is also a need to create smaller packages with more consistent thermal expansion properties while enabling the redistribution of signal connection devices of the various dice to a more convenient, possibly denser, and optionally standard configuration for attachment to a carrier substrate, the redistribution layers also enabling higher frequency signal performance.

Finally, it would be advantageous to provide a system on a chip packaging solution using known good dice, such use thereby increasing the yield of usable packages and, thus, improving the efficiency and cost effectiveness associated with producing such packages.

DISCLOSURE OF INVENTION

The present invention provides a multichip multilayer system on a chip solution. Greater integration is accomplished using a plurality and variety of known good dice applied in a flip-chip configuration to a silicon substrate containing at least one circuit redistribution layer. This allows the use of manufacturing processes and geometries for silicon for creating the redistribution and interconnect layers for the multichip configuration.

The redistribution layers may be terminated with conductive bumps, perhaps in a standard configuration, at the top layer such that the multichip package may be used in a typical flip-chip application to a carrier substrate such as a printed wiring board or other multichip module.

In accordance with one aspect of the invention, a substrate, such as a silicon wafer, is coated with a layer of dielectric material. A first conductive trace layer is deposited and patterned atop the dielectric layer. Circuit connection elements, such as metal columns, are formed upon the first conductive trace layer at various locations. Conductive bumps

are formed on the circuit connection elements to provide interconnection with an external device such as a carrier substrate.

A plurality of additional conductive trace layers may be formed for signal redistribution purposes. Once the desired number of conductive trace layers is formed, a final dielectric layer is formed over the last of the conductive trace layers. Vias, or holes, are formed in the final dielectric layer to accommodate connection of the conductive trace layers with the signal device connections of the semiconductor dice. The various semiconductor dice may be attached, for example, in a flip-chip configuration with the active area of the dice facing the final dielectric layer and the signal device connections on the dice positioned in the holes and contacting the underlying conductive trace layer.

The entire assembly may then be covered with an encapsulation layer covering the various dice and the top dielectric layer to protect them from the elements. However, the encapsulation layer is configured so that portions of the circuit connection elements are exposed therethrough. Conductive bumps may then be applied to the exposed portions of the circuit connection elements, thereby providing an external connection mechanism for electrical interconnection with, for example, a carrier substrate or another multichip module.

Multiple semiconductor device packages may be formed on a silicon wafer with each package functioning as a system on a chip module. Each individual package may be tested through appropriate electrical connection with the conductive bumps prior to the packages being singulated.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings, which illustrate what is currently considered to be the best mode for carrying out the invention:

FIGS. 1A and 1B show a perspective view and a cross-sectional view, respectively, of an exemplary semiconductor die which may be used in conjunction with various embodiments of the present invention;

FIGS. 2A-2F show cross-sectional views of a semiconductor device package according to an embodiment of the present invention at various stages of fabrication;

FIG. 3 is a plan view showing a substrate having a plurality of semiconductor device packages formed thereon according to an embodiment of the invention;

FIG. 4 is a plan view showing a memory device including a multichip semiconductor device package according to an embodiment of the present invention; and

FIG. 5 is a block diagram of a computing system including a multichip semiconductor device package according to an embodiment of the present invention.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

Referring first to drawing FIGS. 1A and 1B, an exemplary semiconductor die 100 which may be utilized in conjunction with the present invention is shown. The semiconductor die 100 includes internal circuitry (not shown) which is coupled to a plurality of signal device connections shown in the form of conductive bumps 102 electrically coupled with bond pads 104 which are formed on the active surface 106 of the die. It is noted that the semiconductor die 100 may exhibit a configuration which is different from that depicted in drawing FIGS. 1A and 1B as will be appreciated by those of ordinary skill in the art. For example, while the conductive bumps 102 are generally shown as spherical balls, such may actually be formed in other shapes such as, for example, stud bumps or columnar members. Furthermore, while the semiconductor die 100 is shown to have only a single row of conductive bumps 102 which extend longitudinally along the active surface 106 thereof, varying arrangements of the conductive bumps 102 may be employed which might include, for example, an arrangement of conductive bumps 102 around the periphery of the active surface 106 or an array of conductive bumps across the field of the active surface 106.

Referring now to drawing FIGS. 2A through 2F, the process of fabricating a semiconductor device package according to an embodiment of the present invention is shown. Referring first to drawing FIG. 2A, a substrate 110, such as, for example, a silicon wafer, is coated with a layer of dielectric material generally referred to herein as a first dielectric layer 112. A first conductive trace layer 114, which may also be referred to as a redistribution layer, is formed over the first dielectric layer 112. The first conductive trace layer 114 may be formed using a conventional metal deposition and patterning process to create a desired configuration of metal interconnect lines.

As shown in drawing FIG. 2B, circuit connection elements 116 are electrically coupled to the first conductive trace layer 114 at various locations. The circuit connection elements 116 may be configured and arranged for electrical connection with an external device as shall be discussed in greater detail below. While the circuit connection

elements 116 are generally depicted as conductive columns, other configurations may be utilized without departing from the spirit and scope of the invention. Such circuit connection elements 116 may be formed of, for example, solder, gold or other metallic compositions. The top surface of the circuit connection elements 116 may be plated with a UMB layer 118, the UMB layer typically being an alloy or combination of different metals, to improve adhesion between the circuit connection elements 116 and additional electrical connection members as will be described in further detail below.

Still referring to drawing FIG. 2B, a second dielectric layer 120 is formed over the first conductive trace layer 114 and first dielectric layer 112. A second conductive trace layer 122 is then formed over the second dielectric layer 120 and is electrically coupled to the first conductive trace layer 114. The first and second conductive trace layers 114 and 122 may be coupled by forming a plurality of vias in the second dielectric layer 120, thereby exposing a plurality of connection areas 124 associated with the first conductive trace layer 114. The second conductive trace layer 122 may then contact the first conductive trace layer 114 through the plurality of connection areas 124.

If desired, a predetermined number of additional circuit redistribution layers may be formed by disposing, in a laminar fashion, additional dielectric layers and conductive trace layers over existing layers and electrically coupling each new conductive trace layer with an adjacent underlying conductive trace layer. Thus, while only one additional circuit redistribution layer is shown in drawing FIGS. 2B-2F, the process of forming additional redistribution layers may be repeated a desired number of times to form multiple redistribution layers. Multiple circuit redistribution layers may be desired to create power planes, ground planes, and/or difficult signal interconnections not easily accomplished on only one or two layers. It is further noted that, in some embodiments, no additional circuit redistribution layers may be required. Thus, only the first conductive trace layer 114 may be required as will be recognized and appreciated by those of ordinary skill in the art.

A final dielectric layer 126 is formed over the second conductive trace layer 122 and second dielectric layer 120 (or the outermost circuit connection layer if additional circuit connection layers are utilized). A plurality of vias 128 is formed in the final dielectric layer 126, such as through a conventional etching process, to expose the second conductive trace layer 122, creating a plurality of exposed connection areas 130 associated with the second conductive trace layer 122.

The vias 128 are sized, arranged and configured to cooperatively mate with the plurality of conductive bumps 102 of a plurality of semiconductor dice 100 (FIGS. 1A and 1B). A metallization layer 132, such as a conventional under bump metallization (UBM) layer, may be formed over each of the exposed connection areas 130 of the second conductive trace layer 122. The metallization layer 132 is formed of a metallic composition which helps to improve electrical and mechanical contact between the exposed connection areas 130 of the second conductive trace layer 122 and, for example, the conductive bumps 102 of the semiconductor dice 100 (FIGS. 1A and 1B). An exemplary UMB layer may include alloys of various metals, such as nickel-gold alloys, titanium-nickel-gold alloys, etc.

Referring to drawing FIG. 2C, in accordance with one embodiment of the present invention, an attachment layer 134 may be formed over a portion of the final dielectric layer 126 and over the metallization layer 132 formed on each exposed connection area 130 of the second conductive trace layer 122. In another embodiment, the attachment layer 134 might be formed to cover the entire surface of the final dielectric layer 126. The attachment layer 134 may be formed of, for example, anisotropic conductive film, anisotropic conductive paste, nonconductive film or nonconductive paste.

Next, as shown in drawing FIG. 2D, a plurality of semiconductor dice 100, such as those shown in drawing FIGS. 1A and 1B, may be attached in a flip-chip configuration to the substrate 110 and its associated layers, with the conductive bumps 102 being aligned with the plurality of exposed connection areas 130 of the second conductive trace layer 122. After placement of the semiconductor dice 100, the attachment layer 134 is cured, thereby forming a reliable electrical and mechanical bond.

The electrical connection mechanism is somewhat different depending on whether anisotropic or nonconductive material is used. When anisotropic materials are used to form the attachment layer 134, the unidirectional conductive properties of the material provide for electrical conduction along an axis between the conductive bumps 102 and the metallization layer 132 while preventing conduction in a direction which is substantially transverse thereto.

On the other hand, if a nonconductive adhesive is used to form the attachment layer 134, the conductive bumps 102 are pulled firmly against the metallization layer 132 due to the reduction of volume or the shrinking of the attachment layer 134 during curing, resulting in a secure electrical connection therebetween.

When using an attachment layer 134 comprising either an anisotropic or nonconductive material, the conductive bumps 102 may comprise, for example, gold, copper or other plated-type alloys. As noted above, regardless of whether anisotropic or nonconductive material is used, the attachment layer 134 also provides a firm mechanical bond between the final dielectric layer 126 and the semiconductor dice 100.

If the conductive bumps 102 are formed as solder-type connections, the process of forming an electrical interconnection between the semiconductor die 100 and substrate 110 may be accomplished by reflowing the solder material such as with controlled collapse chip connect (C4) technology. Additionally, if the conductive bumps 102 are formed as solder-type connections, an underfill material may be used in place of the attachment layer 134 to fill the space between the active surface 106 of the semiconductor dice 100 and the final dielectric layer 126. The underfill material helps to protect the signal connection devices from the surrounding environment and, in some cases, reduces stress that may be generated in the resulting soldered connections due to a mismatch of coefficients of thermal expansion between the semiconductor die 100 and the substrate 110 with its various layers.

Referring now to drawing FIG. 2E, with the semiconductor dice 100 being electrically coupled to the second conductive trace layer 122, an encapsulation layer 140 may be applied over the semiconductor dice 100 as well as the final dielectric layer 126 to protect them from the surrounding environment. A portion of the circuit connection elements 116 including the UBM layer metal 118 remains exposed through the encapsulation layer 140.

Referring now to drawing FIG. 2F, a plurality of conductive bumps 142 may be formed with each conductive bump being disposed on, and electrically coupled to, the exposed portion of a respective circuit connection element 116. The conductive bumps 142 may be formed as, for example, solder bumps or stud bumps comprised of gold, copper, or other plated-type alloys. With the conductive bumps 142 formed, testing of the resulting semiconductor device package may be conducted through appropriate electrical connection with the conductive bumps 142. It is noted, however, that testing might occur at other stages of fabrication as well through appropriate electrical connection with the circuit connection elements 116 prior to formation of the conductive bumps 142.

Referring now to drawing FIG. 3, a wafer assembly 150 is shown having a plurality of semiconductor device packages 152 according to an embodiment of the

present invention. It is noted that the semiconductor device packages 152 are shown without the encapsulation layer for purposes of clarity. Each semiconductor device package 152 may include a plurality of semiconductor dice 100A-100D. The wafer assembly 150 is sawed into individual segments along sawing lines 160 to form the individual semiconductor device packages 152. Having multiple semiconductor dice 100A -100D in each package 152, each individual semiconductor device package may function as a system on a chip module. For example, semiconductor die 100A might be a processor, semiconductor die 100B might be a memory controller and semiconductor dice 100C and 100D might be memory chips. Although FIG. 3 shows a semiconductor device package 152 containing four semiconductor dice 100A-100D, it should be understood that the number of dice within a semiconductor device package 152 might be some other number depending on the design and intended use thereof. It is further noted that while the circuit connection elements 116 have been shown to be located and arranged generally adjacent the periphery of the semiconductor device package 152, other arrangements and configurations may be used as will be appreciated by those of ordinary skill in the art.

Referring now to drawing FIG. 4, a memory device 200, also referred to as a memory module, is shown which incorporates at least one semiconductor device package 152 according to the present invention. The memory device 200 includes a carrier substrate 210, such as a printed circuit board, to which one or more semiconductor device packages 152 may be electrically and operably coupled. A plurality of electrical connectors 220 id formed on the carrier substrate 210 to provide input and output connections from an external device, such as, for example, the motherboard of a computer, to the one or more semiconductor device packages 152.

Referring now to drawing FIG. 5, a computing system 300 is shown which includes a carrier substrate 302 such as, for example, a motherboard. The carrier substrate 302 may be operably coupled to at least one processor 304, such as, for example, a central processing unit (CPU) and at least one memory device 200. The memory device 200 may include one or more semiconductor device packages 152 such as described above. The carrier substrate 302 is operably coupled with at least one input device 310 such as, for example, a keyboard, a mouse, a sensor or another computing device. The carrier substrate 302 is also operably coupled with at least one output device 312 such as, for example, a printer, a monitor, an actuator or another computing

device. Alternatively, the packaged multichip semiconductor device 152 may be coupled directly with the carrier substrate 302.

Specific embodiments have been shown by way of example in the drawings and have been described in detail herein; however, the invention may be susceptible to various modifications and alternative forms. It should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention includes all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor device package using a substrate having a surface comprising:

forming a first dielectric layer on the surface of the substrate;

forming a conductive trace layer on the first dielectric layer;

forming a plurality of circuit connection elements and electrically coupling each circuit connection element of the plurality to the conductive trace layer;

forming a second dielectric layer over the conductive trace layer;

forming a plurality of vias in the second dielectric layer exposing a plurality of connection areas on the conductive trace layer;

providing a plurality of semiconductor dice, each semiconductor die of the plurality having a plurality of signal connection devices; and

electrically coupling the plurality of signal connection devices of each of the plurality of semiconductor dice with the plurality of connection areas on the conductive trace layer.

2. The method of claim 1, further comprising applying a layer of encapsulation material over the plurality of semiconductor dice while leaving a portion of each of the plurality of circuit connection elements exposed therethrough.

3. The method of claim 1, wherein electrically coupling the plurality of signal connection devices further comprises forming a metallization layer on the plurality of connection areas on the conductive trace layer.

4. The method of claim 1, further comprising depositing a barrier metal layer on a surface of each of the plurality of circuit connection elements.

5. The method of claim 4, further comprising forming a plurality of conductive bumps wherein each conductive bump of the plurality is disposed on the barrier metal layer of each of the circuit connection elements.

6. The method of claim 5, wherein forming a plurality of conductive bumps further comprises forming the plurality of conductive bumps to comprise at least one of the group consisting of solder bumps, gold stud bumps, copper stud bumps, and plated alloy stud bumps.

7. The method of claim 5, further comprising singulating the substrate into a plurality of multichip packages wherein each multichip package of the plurality includes at least two semiconductor dice.

8. The method of claim 7, further comprising arranging the plurality of semiconductor dice such that the at least two semiconductor dice of each multichip package are of at least two functional varieties.

9. The method of claim 1, wherein electrically coupling the plurality of signal connection devices of each of the plurality of semiconductor dice with the plurality of connection areas on the conductive trace layer includes forming a soldered connection between each of the plurality of signal connection devices and each of the plurality of connection areas.

10. The method of claim 1, further comprising forming an attachment layer over at least a portion of the first dielectric layer prior to electrically coupling the plurality of signal connection devices with the plurality of connection areas.

11. The method of claim 10, wherein forming an attachment layer includes forming the attachment layer of a material comprising at least one of an anisotropic conducting film, an anisotropic conducting paste, a nonconductive film, and a nonconductive paste.

12. A method of manufacturing a multichip semiconductor device package using a substrate having a surface comprising:

forming a first dielectric layer on the surface of the substrate;

forming a first conductive trace layer on the first dielectric layer;

forming a plurality of circuit connection elements wherein each circuit connection element is electrically coupled with the first conductive trace layer;

forming at least one additional dielectric layer over the first conductive trace layer;

forming at least one additional conductive trace layer over the at least one additional dielectric layer and electrically coupling the at least one additional conductive trace layer with the first conductive trace layer;

forming a final dielectric layer over the at least one additional conductive trace layer;

forming a plurality of vias in the final dielectric layer, thereby exposing a plurality of connection areas on the at least one additional conductive trace layer;

forming a metallization layer on the plurality of connection areas;

providing a plurality of semiconductor dice, each semiconductor die of the plurality having a plurality of signal connection devices;

electrically coupling each of the plurality of signal connection devices with the metallization layer on each of the plurality of connection areas; and

forming an encapsulation layer over the plurality of semiconductor dice and the final dielectric layer while leaving a portion of the circuit connection elements exposed therethrough.

13. The method of claim 12, further comprising forming a plurality of conductive bumps with each conductive bump being disposed on a respective one of the plurality of circuit connection elements.

14. The method of claim 13, further comprising forming a barrier metal layer over the plurality of circuit connection elements prior to forming the plurality of conductive bumps.

15. The method of claim 13, further comprising forming an attachment layer over the final dielectric layer prior to electrically coupling the plurality of signal connection devices with the metallization layer on the plurality of connection areas.

16. The method of claim 15, wherein forming an attachment layer includes forming the attachment layer of a material comprising at least one of an anisotropic conducting film, an anisotropic conducting paste, a nonconductive film, and a nonconductive paste.

17. A method of manufacturing a semiconductor device package comprising:

providing a substrate;

forming a first dielectric layer on a surface of the substrate;

forming a conductive trace layer on the first dielectric layer;

forming a plurality of circuit connection elements and electrically coupling each circuit connection element of the plurality to the conductive trace layer;

forming a second dielectric layer over the conductive trace layer;

forming a plurality of vias in the second dielectric layer exposing a plurality of connection areas on the conductive trace layer;

providing a plurality of semiconductor dice, each die of the plurality having a plurality of signal connection devices; and

electrically coupling the plurality of signal connection devices of each of the plurality of semiconductor dice with the plurality of connection areas on the conductive trace layer.

18. The method of claim 17, further comprising applying a layer of encapsulation material over the plurality of semiconductor dice while leaving a portion of each of the plurality of circuit connection elements exposed therethrough.

19. The method of claim 17, wherein electrically coupling the plurality of signal connection devices further comprises forming a metallization layer on the plurality of connection areas on the conductive trace layer.

20. The method of claim 17, further comprising depositing a barrier metal layer on a surface of each of the plurality of circuit connection elements.

21. The method of claim 20, further comprising forming a plurality of conductive bumps wherein each conductive bump of the plurality is disposed on the barrier metal layer of each of the circuit connection elements.

22. The method of claim 21, wherein forming a plurality of conductive bumps further comprises forming the plurality of conductive bumps to comprise at least one of the group consisting of solder bumps, gold stud bumps, copper stud bumps, and plated alloy stud bumps.

23. The method of claim 21, further comprising singulating the substrate into a plurality of multichip packages wherein each multichip package of the plurality includes at least two semiconductor dice.

24. The method of claim 23, further comprising arranging the plurality of semiconductor dice such that the at least two semiconductor dice of each multichip package are of at least two functional varieties.

25. The method of claim 17, wherein electrically coupling the plurality of signal connection devices of each of the plurality of semiconductor dice with the plurality of connection areas on the conductive trace layer includes forming a soldered connection between each of the plurality of signal connection devices and each of the plurality connection areas.

26. The method of claim 17, further comprising forming an attachment layer over at least a portion of the first dielectric layer prior to electrically coupling the plurality of signal connection devices with the plurality of connection areas.

27. The method of claim 26, wherein forming an attachment layer includes forming the attachment layer of a material comprising at least one of an anisotropic conducting film, an anisotropic conducting paste, a nonconductive film, and a nonconductive paste.

28. A method of manufacturing a multichip semiconductor device package comprising:

providing a substrate;

forming a first dielectric layer on a surface of the substrate;

forming a first conductive trace layer on the first dielectric layer;

forming a plurality of circuit connection elements wherein each circuit connection element is electrically coupled with the first conductive trace layer;

forming at least one additional dielectric layer over the first conductive trace layer;

forming at least one additional conductive trace layer over the at least one additional dielectric layer and electrically coupling the at least one additional conductive trace layer with the first conductive trace layer;

forming a final dielectric layer over the at least one additional conductive trace layer;

forming a plurality of vias in the final dielectric layer, thereby exposing a plurality of connection areas on the at least one additional conductive trace layer;

forming a metallization layer on the plurality of connection areas;

providing a plurality of semiconductor dice, each semiconductor die of the plurality having a plurality of signal connection devices;

electrically coupling each of the plurality of signal connection devices with the metallization layer on each of the plurality of connection areas; and

forming an encapsulation layer over the plurality of semiconductor dice and the final dielectric layer while leaving a portion of the circuit connection elements exposed therethrough.

29. The method of claim 28, further comprising forming a plurality of conductive bumps with each conductive bump being disposed on a respective one of the plurality of circuit connection elements.

30. The method of claim 29, further comprising forming a barrier metal layer over the plurality of circuit connection elements prior to forming the plurality of conductive bumps.

31. The method of claim 29, further comprising forming an attachment layer over the final dielectric layer prior to electrically coupling the plurality of signal connection devices with the metallization layer on the plurality of connection areas.

32. The method of claim 31, wherein forming an attachment layer includes forming the attachment layer of a material comprising at least one of an anisotropic conducting film, an anisotropic conducting paste, a nonconductive film, and a nonconductive paste.

33. A semiconductor device package comprising:

a substrate;

a first dielectric layer disposed over a surface of the substrate;

a conductive trace layer disposed over the first dielectric layer;

a second dielectric layer disposed over the conductive trace layer, the second dielectric layer defining a plurality of vias therethrough exposing a plurality of connection areas on the conductive trace layer;

a metallization layer electrically coupled with the plurality of connection areas;

a plurality of semiconductor dice, each semiconductor die having a plurality of signal connection devices wherein

the plurality of signal connection devices is electrically coupled with the metallization layer;

an encapsulation layer disposed over the plurality of semiconductor dice; and

a plurality of circuit connection elements electrically coupled to the conductive trace layer, wherein each of the plurality of circuit connection elements extends through the first dielectric layer and the second dielectric layer and has a portion thereof exposed through the encapsulation layer.

34. The semiconductor device package of claim 33, further comprising a plurality of conductive bumps wherein each conductive bump is electrically coupled with the exposed portion of one of the plurality of circuit connection elements.

35. The semiconductor device package of claim 34, wherein the plurality of conductive bumps is selected from the group consisting of solder bumps, gold stud bumps, copper stud bumps, and plated alloy stud bumps.

36. The semiconductor device package of claim 35, wherein the plurality of signal connection devices comprises solder bumps.

37. The semiconductor device package of claim 33, further comprising a final dielectric layer disposed adjacent the metallization layer and an attachment layer overlaying at least a portion of the final dielectric layer and the metallization layer.

38. The semiconductor device package of claim 37, wherein the attachment layer is selected from the group consisting of anisotropic conducting film, anisotropic conducting paste, nonconductive film, and nonconductive paste.

39. The semiconductor device package of claim 38, wherein the plurality of signal connection devices is selected from the group consisting of gold stud bumps, copper stud bumps, and plated stud bumps.

40. A semiconductor device package comprising:

a substrate;

a first dielectric layer disposed over a surface of the substrate;

a first conductive trace layer disposed over the first dielectric layer;

at least one additional dielectric layer disposed over the first conductive trace layer;

at least one additional conductive trace layer disposed over the at least one additional dielectric layer, the at least one additional dielectric layer being electrically coupled with the first conductive trace layer;

a final dielectric layer disposed over the at least one additional conductive trace layer;

a plurality of semiconductor dice, each semiconductor die having a plurality of signal connection devices wherein

the plurality of signal connection devices is electrically coupled with the at least one additional conductive trace layer;

an encapsulation layer disposed over the plurality of semiconductor dice; and

a plurality of circuit connection elements electrically coupled with the first conductive trace layer, wherein each of the plurality of circuit connection elements extends through the first dielectric layer, and the at least one additional dielectric layer and has a portion thereof exposed through the encapsulation layer.

41. The semiconductor device package of claim 40, further comprising a plurality of conductive bumps wherein each conductive bump is disposed on and electrically coupled with the exposed portion of a one of the plurality of circuit connection elements.

42. The semiconductor device package of claim 41, wherein the plurality of conductive bumps is selected from the group consisting of solder bumps, gold stud bumps, copper stud bumps, and plated alloy stud bumps.

43. The semiconductor device package of claim 41, further comprising a plurality of openings in the final dielectric layer exposing a plurality of connection areas on the at least one additional conductive trace layer and wherein the plurality of signal connection devices is electrically coupled with the plurality of exposed connection areas.

44. The semiconductor device package of claim 43, further comprising a metallization layer disposed between the plurality of signal connection devices and the plurality of exposed connection areas.

45. The semiconductor device package of claim 44, further comprising an attachment layer disposed over the final dielectric layer and the metallization layer.

46. The semiconductor device package of claim 45, wherein the attachment layer is selected from the group consisting of anisotropic conducting film, anisotropic conducting paste, nonconductive film, and nonconductive paste.

47. The semiconductor device package of claim 46 wherein the plurality of signal connection devices is selected from the group consisting of gold stud bumps, copper stud bumps, and plated stud bumps.

48. A memory device comprising:

a carrier substrate;

a plurality of electrical contacts coupled with electrical circuitry formed in the carrier substrate; and

at least one semiconductor device package coupled with the electrical circuitry in the carrier substrate, the at least one semiconductor device package comprising:

a substrate;

a first dielectric layer disposed over a surface of the substrate;

a conductive trace layer disposed over the first dielectric layer;

a second dielectric layer disposed over the conductive trace layer, the second dielectric layer defining a plurality of vias therethrough exposing a plurality of connection areas on the conductive trace layer;

a metallization layer electrically coupled with the plurality of connection areas;

a plurality of semiconductor dice, each semiconductor die having a plurality of signal connection devices wherein the plurality of signal connection devices is electrically coupled with the metallization layer;

an encapsulation layer disposed over the plurality of semiconductor dice; and

a plurality of circuit connection elements electrically coupled to the conductive trace layer, wherein each of the plurality of circuit connection elements extends through the first dielectric layer and the second dielectric layer and has a portion thereof exposed through the encapsulation layer.

49. A computing system comprising:

a carrier substrate;

a processor operably coupled to circuitry formed in the carrier substrate;

at least one input device operably coupled with the circuitry formed in the carrier substrate;

at least one output device operably coupled with the circuitry formed in the carrier substrate; and

a memory device operably coupled to the circuitry formed in the carrier substrate, the memory device including at least one semiconductor device package, the at least one semiconductor device package comprising:

a substrate;

a first dielectric layer disposed over a surface of the substrate;

a conductive trace layer disposed over the first dielectric layer;

a second dielectric layer disposed over the conductive trace layer, the second dielectric layer defining a plurality of vias therethrough exposing a plurality of connection areas on the conductive trace layer;

a metallization layer electrically coupled with the plurality of connection areas;

a plurality of semiconductor dice, each semiconductor die having a plurality of signal connection devices wherein the plurality of signal connection devices is electrically coupled with the metallization layer;

an encapsulation layer disposed over the plurality of semiconductor dice; and

a plurality of circuit connection elements electrically coupled to the conductive trace layer, wherein each of the plurality of circuit connection elements extends through the first dielectric layer and the second dielectric layer and has a portion thereof exposed through the encapsulation layer.

50. A computing system comprising:

a carrier substrate;

at least one input device operably coupled with circuitry formed in the carrier substrate;

at least one output device operably coupled with the circuitry formed in the carrier substrate; and

at least one semiconductor device package operably coupled with the circuitry formed in the carrier substrate, the at least one semiconductor device package comprising:

a substrate;

a first dielectric layer disposed over a surface of the substrate;

a conductive trace layer disposed over the first dielectric layer;

a second dielectric layer disposed over the conductive trace layer, the second dielectric layer defining a plurality of vias therethrough exposing a plurality of connection areas on the conductive trace layer;

a metallization layer electrically coupled with the plurality of connection areas;

a plurality of semiconductor dice, each semiconductor die having a plurality of signal connection devices wherein the plurality of signal connection devices is electrically coupled with the metallization layer;

an encapsulation layer disposed over the plurality of semiconductor dice; and

a plurality of circuit connection elements electrically coupled to the conductive trace layer, wherein each of the plurality of circuit connection elements extends through the first dielectric layer and the second dielectric layer and has a portion thereof exposed through the encapsulation layer.