SEMICONDUCTOR DEVICE HAVING TIPLESS EPITAXIAL SOURCE/DRAIN REGIONS

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The invention is in the field of Semiconductor Devices.

DESCRIPTION OF RELATED ART

For the past several years, the performance of semiconductor devices, such as Metal Oxide Semiconductor Field-Effect Transistors (MOS-FETs), has been greatly enhanced by the incorporation of strained channel regions into the active portions of a semiconductor substrate, e.g. the use of compressively strained silicon channel regions to enhance hole mobility in P-type Metal Oxide Semiconductor Field-Effect Transistors (PMOS-FETs). The presence of such strained channel regions may greatly enhance the rate at which charge migrates in a channel when a semiconductor device is in an ON state.

Figures 1A-C illustrate cross-sectional views representing a typical process flow for forming strain-inducing source/drain regions in a PMOS-FET, in accordance with the prior art. Referring to Figure 1A, a non-strained PMOS-FET 100 is first formed. Non-strained PMOS-FET 100 is comprised of a channel region 102. A gate dielectric layer 104 sits above channel region 102 and a gate electrode 106 sits above gate dielectric layer 104. Gate dielectric layer 104 and gate electrode 106 are isolated by gate isolation spacers 108. Tip extensions 110 and source/drain regions 112 are formed by implanting dopant atoms into substrate 114 and are formed, in part, to reduce the parasitic resistance of non-strained PMOS-FET 100. Thus, the source/drain regions 112 are initially formed from the same material as the channel region 102. Therefore, the lattice mismatch between the source/drain regions 112 and the channel region 102 is negligible, resulting in effectively no strain on the channel region 102.

Referring to Figure 1B, portions of substrate 114, including source/drain regions 112, are removed by an etch process to form recessed regions 116 in substrate 114. Subsequently, strain-inducing source/drain regions 120 are formed by selectively growing an epitaxial film into recessed regions 116, as depicted in Figure 1C. Strain-inducing source/drain regions 120 can be doped with charge-carrier atoms, e.g. boron in the case of a PMOS-FET, which may be carried out *in situ* or after epitaxial film growth, or both. In an example, substrate 114, and hence channel region 102, is comprised of crystalline

silicon and the film grown to form strain-inducing source/drain regions 120 is comprised of epitaxial silicon/germanium. The lattice constant of the epitaxial silicon/germanium film is greater than that of crystalline silicon by a factor of ~ 1% (for 70% Si, 30% Ge) and so strain-inducing source/drain regions 120 are comprised of a material with a larger lattice constant than that of channel region 102. Therefore, a uniaxial compressive strain, depicted by the arrows in Figure 1C, is rendered on channel region 102 in strained PMOS-FET 130, which can enhance hole mobility in the device.

One drawback to this approach is that gate isolation spacers 108 are required to inhibit undesirable material growth on gate electrode 106 during epitaxial film growth to form strain-inducing source/drain regions 120, e.g. to inhibit the growth of silicon/germanium on a polysilicon gate electrode. The location of the strain-inducing source/drain regions 120 relative to channel region 102 is therefore restricted by the width of gate isolation spacers 108. Thus, the parasitic resistance-reducing ability and the strain-inducing ability of strain-inducing source/drain regions 120 may be limited. Tip extensions 110 may be formed in substrate 114 to reduce the resistance of strained PMOS-FET 130. However, tip extensions 110 are formed from the same material as channel region 102. Therefore, the lattice mismatch between tip extensions 110 and the channel region 102 is negligible, resulting in effectively no additional strain on the channel region 102 from tip extensions 110.

Thus, a semiconductor device having tipless epitaxial source/drain regions and a method for its formation are described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-C illustrate cross-sectional views representing a typical process flow for forming strain-inducing source/drain regions in a PMOS-FET, in accordance with the prior art.

Figure 2 illustrates a cross-sectional view representing a planar MOS-FET having tipless epitaxial source/drain regions, in accordance with an embodiment of the present invention.

Figures 3A-J illustrate cross-sectional views representing the formation of a planar MOS-FET having tipless epitaxial source/drain regions, in accordance with an embodiment of the present invention.

Figures 4A-G illustrate cross-sectional views representing the formation of a trigate MOS-FET having tipless epitaxial source/drain regions, in accordance with an embodiment of the present invention.

Figures 5A-B illustrate cross-sectional views representing the formation of a planar MOS-FET having tipless epitaxial source/drain regions and dielectric spacers, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

A semiconductor device having tipless epitaxial source/drain regions and a method for its formation are described. In the following description, numerous specific details are set forth, such as specific dimensions and chemical regimes, in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known processing steps such as patterning steps or wet chemical cleans are not described in detail in order to not unnecessarily obscure the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

Disclosed herein are a semiconductor device having tipless epitaxial source/drain regions and a method to form such a device. In an embodiment, the semiconductor device comprises a gate stack on a substrate. The gate stack may be comprised of a gate electrode above a gate dielectric layer and may be above a channel region in the substrate. In one embodiment, the semiconductor device also comprises a pair of source/drain regions in the substrate on either side of the channel region. The pair of source/drain regions may be in direct contact with the gate dielectric layer and the lattice constant of the pair of source/drain regions may be different than the lattice constant of the channel region. In a specific embodiment, the semiconductor device is formed by using a dielectric gate stack placeholder.

A semiconductor device comprising tipless epitaxial source/drain regions may exhibit improved performance resulting from an increase in the strain-inducing ability of such source/drain regions. That is, the formation of strain-inducing source/drain regions in the absence of gate isolation spacers may enable the formation of strain-inducing source/drain regions directly adjacent to the gate stack and, hence, closer to the channel region directly underneath the gate stack. Thus, in accordance with an embodiment of the present invention, strain-inducing source/drain regions are formed in direct contact with

the gate dielectric layer of a semiconductor device, optimizing the proximity of the strain-inducing source/drain regions to the channel region of the semiconductor device. In one embodiment, this structural arrangement provides for an increased mobility of charge-carriers in the channel region when the semiconductor device is in an ON state. In a specific embodiment, this structural arrangement eliminates the need for tip extensions because the parasitic resistance is mitigated by forming the strain-inducing source/drain regions proximate to the channel region.

The formation of strain-inducing source/drain regions directly adjacent to the gate stack may be carried out by using a dielectric gate stack placeholder in a replacement gate scheme. Thus in accordance with an embodiment of the present invention, material growth is inhibited on a dielectric gate stack placeholder, eliminating the need for gate isolation spacers during the fabrication of strain-inducing epitaxial source/drain regions. In one embodiment, the dielectric gate stack placeholder is subsequently replaced with an actual gate stack following the formation of strain-inducing epitaxial source/drain regions.

A semiconductor device may be formed having epitaxial source/drain regions in direct contact with a gate stack. Figure 2 illustrates a cross-sectional view representing a planar MOS-FET having tipless epitaxial source/drain regions, in accordance with an embodiment of the present invention.

Referring to Figure 2, a semiconductor device 200 is comprised of a substrate 202 having a channel region 204. A gate stack comprised of a gate dielectric layer 206 and a gate electrode 218 sits above channel region 204. Strain-inducing epitaxial source/drain regions 208 are formed in substrate 202 on either side of and undercutting channel region 204. Strain-inducing epitaxial source/drain regions 208 are in direct contact with the gate stack and, in particular, with gate dielectric layer 204. An inter-layer dielectric film 210 is formed above strain-inducing epitaxial source/drain regions 208 and directly adjacent to the sidewalls of gate the gate stack.

Semiconductor device 200 may be any semiconductor device incorporating a gate, a channel region and a pair of source/drain regions. In accordance with an embodiment of the present invention, semiconductor device 200 is selected from the group consisting of a planar MOS-FET, a memory transistor or a Microelectromechanical System (MEMS). In one embodiment, semiconductor device 200 is a planar MOS-FET and is an isolated device or is one device in a plurality of nested devices. In a specific embodiment, semiconductor device 200 is a planar isolated PMOS-FET having isolation regions 214 on either side of strain-inducing epitaxial source/drain regions 208, as depicted in Figure 2.

As will be appreciated for the typical integrated circuit, both N- and P-channel transistors may be fabricated on a single substrate to form a CMOS integrated circuit.

Substrate 202 and, hence, channel region 204 may be comprised of any semiconductor material that can withstand a manufacturing process and in which charge can migrate. In an embodiment, substrate 202 is comprised of a crystalline silicon, silicon/germanium or germanium layer doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron or a combination thereof. In one embodiment, the concentration of silicon atoms in substrate 202 is greater than 97%. In another embodiment, substrate 202 is comprised of an epitaxial layer grown atop a distinct crystalline substrate, e.g. a silicon epitaxial layer grown atop a boron-doped bulk silicon mono-crystalline substrate. Substrate 202 may also comprise an insulating layer in between a bulk crystal substrate and an epitaxial layer to form, for example, a silicon-on-insulator substrate. In an embodiment, the insulating layer is comprised of a material selected form the group consisting of silicon dioxide, silicon nitride, silicon oxy-nitride or a high-k dielectric layer. Substrate 202 may alternatively comprise a III-V material. In an embodiment, substrate 202 is comprised of a III-V material such as, but not limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide, indium gallium phosphide or a combination thereof. Channel region 204 may be formed in a well of charge-carrier dopant impurity atoms. In one embodiment, substrate 202 is comprised of crystalline silicon and the charge-carrier dopant impurity atoms are selected from the group consisting of boron, arsenic, indium or phosphorus. In another embodiment, substrate 202 is comprised of a III-V material and the charge-carrier dopant impurity atoms are selected from the group consisting of carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

The strain-inducing epitaxial source/drain regions 208 may be comprised of a low defect density mono-crystalline film having a lattice constant different than the lattice constant of substrate 202. The lattice constants are based on the atomic spacings and the unit cell orientations within each of the channel region 204 and the strain-inducing epitaxial source/drain regions 208. Thus, a pair of semiconductor regions formed within a crystalline substrate and having a lattice constant different than that of the crystalline substrate may impart a uniaxial strain to the portion of the crystalline substrate in between the pair of semiconductor regions. For example, in accordance with an embodiment of the present invention, the lattice constant of strain-inducing epitaxial source/drain regions 208

is larger than the lattice constant of channel region 204 and imparts a uniaxial compressive strain to the lattice of channel region 204. Thus, when the lattice constant of strain-inducing epitaxial source/drain regions 208 is larger than the lattice constant of channel region 204, the lattice-forming atoms of the strain-inducing epitaxial source/drain regions 208 are pushed together from their normal resting state and induce a compressive strain on channel region 204 as they attempt to relax. In a specific embodiment, this uniaxial compressive strain invoked on channel region 204 increases hole mobility in channel region 204. In an alternative embodiment of the present invention, the lattice constant of strain-inducing epitaxial source/drain regions 208 is smaller than the lattice constant of channel region 204 and imparts a uniaxial tensile strain to the lattice of channel region 204. Thus, when the lattice constant of strain-inducing epitaxial source/drain regions 208 is smaller than the lattice constant of channel region 204, the lattice-forming atoms of the strain-inducing epitaxial source/drain regions 208 are pulled apart from their normal resting state and induce a tensile strain on channel region 204 as they attempt to relax. In a specific embodiment, this uniaxial tensile strain invoked on channel region 204 increases electron mobility in channel region 204.

Strain-inducing epitaxial source/drain regions 208 may be comprised of any material having a lattice constant different than the lattice constant of channel region 204 and having a resistivity sufficiently low to mitigate parasitic resistance. In one embodiment, channel region 204 is comprised of Si_xGe_{1-x} and strain-inducing epitaxial source/drain regions 208 are comprised of Si_yGe_{1-y} where $0 \leq x, y \leq 1$ and $x \neq y$. In a specific embodiment, semiconductor device 200 is a PMOS-FET, channel region 204 is comprised of silicon (i.e. $x = 1$) and strain-inducing epitaxial source/drain regions 208 are comprised of silicon/germanium having an atomic ratio of 70:30 (i.e. $y = 0.7$). In another embodiment, channel region 204 is comprised of silicon and strain-inducing epitaxial source/drain regions 208 are comprised of carbon-doped silicon. In a specific embodiment, semiconductor device 200 is an NMOS-FET, channel region 204 is comprised of silicon and strain-inducing epitaxial source/drain regions 208 are comprised of carbon-doped silicon having an atomic concentration of substitutional carbon atoms in the range of 0.5 – 1.5%. In an alternative embodiment, channel region 204 is comprised of a III-V material selected from the group consisting of $Al_xGa_{1-x}As$, $In_xGa_{1-x}As$, $In_xGa_{1-x}P$ or $Al_xIn_{1-x}Sb$ and strain-inducing epitaxial source/drain regions 208 are comprised of $Al_yGa_{1-y}As$, $In_yGa_{1-y}As$, $In_yGa_{1-y}P$ or $Al_yIn_{1-y}Sb$, respectively, where $0 \leq x, y \leq 1$ and $x \neq y$. In a particular embodiment, source/drain regions 208 are comprised of a material having a

lattice constant different than the lattice constant of channel region 204 by a factor of at least 0.1%.

Strain-inducing epitaxial source/drain regions 208 may further comprise charge-carrier dopant impurity atoms. In one embodiment, strain-inducing epitaxial source/drain regions 208 are comprised of epitaxial silicon/germanium and the charge-carrier dopant impurity atoms are boron atoms. In a specific embodiment, semiconductor device 200 is a PMOS-FET, channel region 204 is comprised of silicon and strain-inducing epitaxial source/drain regions 208 are comprised of silicon/germanium having a germanium atomic concentration in the range of 20 – 35% with a concentration of boron dopant impurity atoms in the range of $5 \times 10^{19} - 5 \times 10^{20}$ atoms/cm^3. In another embodiment, strain-inducing epitaxial source/drain regions 208 are comprised of a III-V material and the charge-carrier dopant impurity atoms are selected from the group consisting of carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium. Regions of out-diffusion 212 from strain-inducing epitaxial source/drain regions 208 and in substrate 202 may be formed adjacent to the periphery of strain-inducing epitaxial source/drain regions 208, as depicted in Figure 2. In one embodiment, strain-inducing epitaxial source/drain regions 208 are comprised of boron-doped silicon/germanium and the regions of out-diffusion 212 are comprised of boron atoms. In a particular embodiment, the concentration of boron atoms in regions of out-diffusion 212 is in the range of $1 \times 10^{17} - 5 \times 10^{20}$ atoms/cm^3.

The gate stack comprised of gate dielectric layer 206 and gate electrode 218 above channel region 204 and in direct contact with strain-inducing epitaxial source/drain regions 208 may be any stack of materials having a conductive region with a dielectric layer between the channel region 204 and the gate stack. In one embodiment, the gate dielectric layer is formed only between the gate electrode 218 and channel region 204. In another embodiment, the gate dielectric layer 206 extends along the sidewalls of gate electrode 218 and directly adjacent to inter-layer dielectric film 210, as depicted in Figure 2.

Gate dielectric layer 206 may comprise any dielectric material suitable to insulate a conductive region 218 from channel region 204. For example, in accordance with an embodiment of the present invention, gate dielectric layer 206 is comprised of a high-k dielectric layer. In one embodiment, the high-k dielectric layer is selected from the group consisting of hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide,

lead zinc niobate or a combination thereof. Furthermore, a portion of gate dielectric layer 206 may comprise a layer of native oxide formed from the top few layers of substrate 202. In an embodiment, gate dielectric layer 206 is comprised of a top high-k portion and a lower portion comprised of an oxide of a semiconductor material. In one embodiment, gate dielectric layer 206 is comprised of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride. In an alternative embodiment, gate dielectric layer 206 is comprised substantially of an oxide layer of the semiconductor material of substrate 202. In a specific embodiment, substrate 202 is comprised substantially of silicon and gate dielectric layer 206 is comprised substantially of silicon dioxide or silicon oxy-nitride.

Gate electrode 218 may be comprised of any conductive material having a suitable workfunction. In an embodiment, gate electrode 218 is a metal gate electrode. In one embodiment, gate electrode 218 is comprised of a metal layer selected from the group consisting of metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides, e.g. ruthenium oxide. In a specific embodiment, gate electrode 218 is comprised of a non-workfunction-setting fill material formed above a metal workfunction-setting layer. In an alternative embodiment, gate electrode 218 is comprised of doped polycrystalline silicon.

Inter-layer dielectric film 210 covers strain-inducing epitaxial source/drain regions 208 and is directly adjacent to the sidewalls of the gate stack. Inter-layer dielectric film 210 may be comprised of any material suitable withstand the fabrication of a plurality of interconnects above semiconductor device 200 while maintaining a sufficient electrical isolation between semiconductor device 200 and any neighboring semiconductor devices. In one embodiment, inter-layer dielectric film 210 is comprised of silicon dioxide or silicon oxy-nitride. In another embodiment, inter-layer dielectric film 210 is comprised of a low-k dielectric material. In a specific embodiment, inter-layer dielectric film 210 is comprised of carbon-doped silicon oxide having a dielectric constant in the range of 2.5 – 4.

Tipless strain-inducing epitaxial source/drain regions may be incorporated into a semiconductor device by using a dielectric gate stack placeholder in a replacement gate integration scheme. Figures 3A-J illustrate cross-sectional views representing the formation of a planar MOS-FET having tipless epitaxial source/drain regions, in accordance with an embodiment of the present invention.

Referring to Figure 3A, a pre-patterned dielectric gate stack placeholder layer 330 is formed above a substrate 302. Substrate 302 may be any substrate described in association with substrate 202 from Figure 2. In accordance with an embodiment of the present invention, isolation regions 314 are incorporated into substrate 302, as depicted in Figure 3A. In a specific embodiment, isolation regions 314 are comprised substantially of silicon dioxide and are fabricated by a shallow-trench isolation (STI) integration scheme.

Pre-patterned dielectric gate stack placeholder layer 330 may be comprised of any dielectric material suitable to be patterned selective to substrate 302 and isolation regions 314 and suitable to inhibit growth of a semiconductor material during a subsequent epitaxial deposition process. In one embodiment, pre-patterned dielectric gate stack placeholder layer 330 is comprised of a material selected from the group consisting of silicon dioxide, silicon oxy-nitride and silicon nitride. In a specific embodiment, substrate 302 is comprised substantially of silicon, isolation regions 314 are comprised of silicon dioxide and pre-patterned dielectric gate stack placeholder layer 330 is comprised substantially of silicon nitride. A protecting layer may be incorporated between pre-patterned dielectric gate stack placeholder layer 330 and substrate 302. In one embodiment, a native layer of silicon dioxide is formed between pre-patterned dielectric gate stack placeholder layer 330 and substrate 302. However, in an alternative embodiment, pre-patterned dielectric gate stack placeholder layer 330 is formed directly on the top surface of substrate 302, as depicted in Figure 3A. Thus, in one embodiment, a distinct gate dielectric placeholder is not required in a replacement gate integration scheme.

Pre-patterned dielectric gate stack placeholder layer 330 may be deposited by any technique suitable to provide a reliable (i.e. uniform composition and thickness) dielectric layer above the top surface of substrate 302. In accordance with an embodiment of the present invention, pre-patterned dielectric gate stack placeholder layer 330 is formed by a chemical vapor deposition (CVD) process. In one embodiment, pre-patterned dielectric gate stack placeholder layer 330 is comprised of stoichiometric silicon nitride (Si_3N_4) and is deposited by a CVD process utilizing the precursors SiH_4 and NH_3 at a temperature in the range of 500 – 850 degrees Celsius. Pre-patterned dielectric gate stack placeholder layer 330 may be deposited to any thickness suitable to define the height of a subsequently formed gate stack. In accordance with an embodiment of the present invention, pre-patterned dielectric gate stack placeholder layer 330 is deposited to a thickness in the range of 50 – 200 nanometers.

Referring to Figure 3B, pre-patterned dielectric gate stack placeholder layer 330 is patterned to form dielectric gate stack placeholder 332 without substantially impacting substrate 302 or isolation regions 314. In accordance with an embodiment of the present invention, a lithography/etch process is used to provide dielectric gate stack placeholder 332. For example, in one embodiment, pre-patterned dielectric gate stack placeholder layer 330 is patterned by first patterning a positive photo-resist layer above pre-patterned dielectric gate stack placeholder layer 330 upon exposure to a wavelength of light selected from the group consisting of 248 nm, 193 nm and 157 nm. In another embodiment, an e-beam direct-write process is used to pattern the positive photo-resist layer. An etch process may then be used to pattern pre-patterned dielectric gate stack placeholder layer 330. In one embodiment, a dry etch process is used. In a particular embodiment, pre-patterned dielectric gate stack placeholder layer 330 is comprised substantially of silicon and the dry etch process comprises an anisotropic plasma etch process wherein the plasma is generated from gases selected from the group consisting of HBr and Cl_2. In one embodiment, a hard-mask layer is utilized in between the positive photo-resist and pre-patterned dielectric gate stack placeholder layer 330. Dielectric gate stack placeholder 332 may be patterned to any width suitable to provide a channel region having a desired channel length in substrate 302. That is, the width of dielectric gate stack placeholder 332 may subsequently determine the width of a gate stack above substrate 302. In one embodiment, the width of dielectric gate stack placeholder 332 is the width of the critical dimension of the lithographic process used to pattern pre-patterned dielectric gate stack placeholder layer 330. In another embodiment, the width of dielectric gate stack placeholder 332 is in the range of 5 – 500 nanometers. In a specific embodiment, the width of dielectric gate stack placeholder 332 is in the range of 10 – 100 nanometers.

Referring to Figures 3C and 3C', etched-out regions 340 and 340' may be formed in substrate 302 selective to dielectric gate stack placeholder 332 and isolation regions 314. Etched-out regions 340 and 340' may be formed by any technique suitable to selectively remove a portion of substrate 302 and to undercut dielectric gate stack placeholder 332. In one embodiment, etched-out regions 340 and 340' are formed by etching any exposed portions of substrate 302 with a dry etch process, a wet etch process or a combination thereof. In one embodiment, etched-out regions 340 are formed by a dry plasma etch using a plasma generated from a gas selected from the group consisting of NF_3 or SF_6 to form isotropic etched-out regions 340, as depicted in Figure 3C. In an alternative embodiment, etched-out regions 340' are formed by a wet etch using NH_4OH

or tetramethylammonium hydroxide. The wet etch may be anisotropic in that the etch rate is significantly slow in directions of high crystal density. For example, in a specific embodiment, the wet etch is hindered by <111> crystal planes in a (100) silicon substrate to provide etched-out regions 340' having an undercut profile θ of approximately 55 degrees, as depicted in Figure 3C'. The extent of undercut underneath dielectric gate stack placeholder 332 may be increased by first carrying out a brief dry etch followed by an anisotropic wet etch process. Etched-out regions 340 and 340' may have any depth suitable for subsequently defining the depth of an epitaxially grown strain-inducing source/drain region. In one embodiment, the depth of etched-out regions 340 and 340' is in the range of 50 – 150 nanometers. Etched-out regions 340 and 340' may undercut dielectric gate stack placeholder 332 by any amount suitable to optimize the performance of a subsequently formed semiconductor device. In one embodiment, etched-out regions 340 and 340' undercut dielectric gate stack placeholder 332 by an amount in the range of 2 – 20% of the cross-section width of dielectric gate stack placeholder 332 on either side of dielectric gate stack placeholder 332.

Referring to Figures 3D and 3D', strain-inducing epitaxial source/drain regions 308 and 308' are formed in etched-out regions 340 and 340', respectively, and a channel region 304 is thus defined in substrate 302. Strain-inducing epitaxial source/drain regions 308 and 308' may be comprised of any material described in association with strain-inducing epitaxial source/drain regions 208 from Figure 2. Additionally, in accordance with an embodiment of the present invention, strain-inducing epitaxial source/drain regions 308 and 308' have a lattice constant different from the lattice constant channel region 304. Thus, in one embodiment, a uniaxial strain is imparted to channel region 304. In a particular embodiment, the top surfaces of strain-inducing epitaxial source/drain regions 308 and 308' are raised above the top surface of channel region 304, as depicted in Figures 3D and 3D'.

Strain-inducing epitaxial source/drain regions 308 and 308' may be formed by any technique suitable to form a highly uniform and low defect epitaxial layer. Particularly, strain-inducing epitaxial source/drain regions 308 and 308' may be formed by a process that does not leave material deposited on polar dielectric surfaces, such as on the surface of isolation regions 314 or dielectric gate stack placeholder 332. Thus, in accordance with an embodiment of the present invention, a totally selective deposition process is used to form strain-inducing epitaxial source/drain regions 308 and 308' in substrate 302. In an embodiment, strain-inducing epitaxial source/drain regions 308 and 308' are deposited by

a process selected from the group consisting of chemical vapor epitaxy, molecular-beam epitaxy or laser-abolition epitaxy. In one embodiment, strain-inducing epitaxial source/drain regions 308 and 308' are comprised of silicon/germanium and are deposited using the precursors SiH_4 and GeH_4. A wet chemical clean may be carried out immediately prior to the deposition of strain-inducing epitaxial source/drain regions 308 and 308'. In one embodiment, the wet chemical cleaning process step comprises the application of an aqueous solution of hydrofluoric acid, ammonium fluoride or both to a silicon substrate 302. In a particular embodiment of the present invention, upon deposition of strain-inducing epitaxial source/drain regions 308 and 308', regions of out-diffusion 312 may be formed adjacent to the periphery of strain-inducing epitaxial source/drain regions 308, as depicted in Figures 3D and 3D'. In one embodiment, the regions of out-diffusion 312 are a consequence of the deposition temperature used to form strain-inducing epitaxial source/drain regions 308 and 308'. For convenience, the structure of Figure 3D' having strain-inducing epitaxial source/drain regions 308' is illustrated throughout remaining Figures 3E-J.

Referring to Figure 3E, a blanket dielectric film 350 is deposited above isolation regions 314, strain-inducing epitaxial source/drain regions 308' and dielectric gate stack placeholder 332. Blanket dielectric film 350 may be comprised of any material described in association with inter-layer dielectric film 210 from Figure 2. Blanket dielectric film 350 may be deposited by any technique suitable to provide a substantially conformal film over isolation regions 314, strain-inducing epitaxial source/drain regions 308' and dielectric gate stack placeholder 332. In one embodiment, blanket dielectric film 350 is deposited by technique selected from the group consisting of a CVD process and a spin-on coating process. Blanket dielectric film 350 may be deposited to any thickness suitable to entirely cover isolation regions 314, strain-inducing epitaxial source/drain regions 308' and dielectric gate stack placeholder 332. In one embodiment, blanket dielectric film 350 is deposited to a thickness in the range of 250 – 400 nanometers.

Referring to Figure 3F, blanket dielectric film 350 is planarized to form inter-layer dielectric film 310 and to expose the top surface of dielectric gate stack placeholder 332. Blanket dielectric film may be planarized by any technique suitable to provide a substantially flat surface for inter-layer dielectric film 310 without dishing below the top surface of dielectric gate stack placeholder 332. In one embodiment, a timed planarization step is utilized. In another embodiment, a chemical-mechanical polish step is used to

planarize blanket dielectric film 350 and the top surface of dielectric gate stack placeholder 332 acts as a natural polish-stop indicator.

Referring to Figure 3G, dielectric gate stack placeholder 332 is removed to provide trench 360 in inter-layer dielectric film 310, above channel region 304 and directly adjacent to strain-inducing epitaxial source/drain regions 308'. Dielectric gate stack placeholder may be removed by any technique suitable to minimally impact the exposed surfaces of inter-layer dielectric film 310, channel region 304 and strain-inducing epitaxial source/drain regions 308'. In accordance with an embodiment of the present invention, dielectric gate stack placeholder 332 is removed by using a dry or a wet etch process step. In one embodiment, dielectric gate stack placeholder 332 is comprised substantially of silicon nitride, inter-layer dielectric film 310 is comprised of silicon dioxide, channel region 304 is comprised of silicon, strain-inducing epitaxial source/drain regions 308' are comprised of silicon/germanium and a dry etch process utilizing at least the gas HBr is used to remove dielectric gate stack placeholder 332. In another embodiment, dielectric gate stack placeholder 332 is removed by using a wet etch comprised of aqueous phosphoric acid having a temperature in the range of 130 – 165 degrees Celsius. In a specific embodiment, a thin layer of silicon dioxide is used between dielectric gate stack placeholder 332 and channel region 304 to act as an etch stop. The thin layer of silicon dioxide is subsequently removed by a quick wet etch step comprising ultra-dilute aqueous HF.

Referring to Figure 3H, a gate dielectric layer 306 is deposited into trench 360 above channel region 304 and in direct contact with strain-inducing epitaxial source/drain regions 308'. Gate dielectric layer 306 may be comprised of any material or material combination described in association with gate dielectric layer 206 from Figure 2. Gate dielectric layer 306 may be deposited by any technique that provides substantially conformal coverage of the exposed surface of channel region 304. Furthermore, gate dielectric layer 306 may be deposited by any technique that provides substantially conformal coverage of the sidewalls of inter-layer dielectric film 310, as depicted in Figure 3H. In accordance with an embodiment of the present invention, gate dielectric layer 306 is deposited by a technique selected from the group consisting of atomic layer deposition, chemical vapor deposition and thermal consumption of the top surface of channel region 304. Gate dielectric layer may be deposited to any thickness suitable to form a high performance capacitor with channel region 304 and a subsequently formed gate electrode. In one embodiment, gate dielectric layer is comprised substantially of a

high-k dielectric layer having a thickness in the range of 10 – 60 Angstroms. In a specific embodiment, gate dielectric layer is comprised substantially of a top layer of hafnium oxide having a thickness in the range of 5 – 40 Angstroms and a bottom layer of silicon dioxide having a thickness in the range of 3 – 6 Angstroms. In an alternative embodiment, a gate dielectric layer is formed between pre-patterned dielectric gate stack placeholder layer 330 and substrate 302 from Figure 3A. The gate dielectric layer is subsequently patterned and carried through all of the process steps described in association with Figures 3B-G.

Referring to Figure 3I, a conductive layer 370 is formed above the top surfaces of gate dielectric layer 306 and in trench 360. Conductive layer 370 may be comprised of any material described in association with gate electrode 218 from Figure 2. In one embodiment, conductive layer 370 is comprised of a thin workfunction-settling portion below a bulk trench-fill portion. Conductive layer 370 may be deposited by any technique and that can substantially fill trench 360 with minimal risk of void formation. In one embodiment, conductive layer 370 is deposited by a technique selected from the group consisting of electro-deposition, electroless-plating, atomic vapor deposition, chemical vapor deposition and physical vapor deposition.

Referring to Figure 3J, the portions of gate dielectric layer 306 and conductive layer 370 above inter-layer dielectric film 310 are removed to provide gate electrode 318. The portions of gate dielectric layer 306 and conductive layer 370 above inter-layer dielectric film 310 may be removed by any technique suitable to provide a substantially flat surface of inter-layer dielectric film 310. In one embodiment, the portions of gate dielectric layer 306 and conductive layer 370 above inter-layer dielectric film 310 are removed by a chemical-mechanical polish step.

Thus, tipless strain-inducing epitaxial source/drain regions may be incorporated into a semiconductor device by using a dielectric gate stack placeholder in a replacement gate integration scheme. In one embodiment, strain-inducing epitaxial source/drain regions 308' are comprised substantially of boron-doped silicon/germanium, channel region 304 is comprised substantially of silicon, and a compressive uniaxial strain is invoked on channel region 304, as depicted by the arrows in Figure 3J. The structure described in association with Figure 3J may then undergo typical process steps to complete the formation of a semiconductor device and to incorporate the device into an integrated circuit. For example, in accordance with an embodiment of the present invention, contact holes are subsequently formed in inter-layer dielectric film 310 and

above strain-inducing epitaxial source/drain regions 308'. A through-contact silicidation step is then carried out prior to formation of back-end metal layers. In an alternative embodiment, a silicide layer is formed on strain-inducing epitaxial source/drain regions 308' prior to the deposition of blanket dielectric film 350 from Figure 3E.

The present invention is not limited to planar semiconductor devices. Figures 4A-G illustrate cross-sectional views representing the formation of a trigate MOS-FET having tipless epitaxial source/drain regions, in accordance with an embodiment of the present invention.

Referring to Figure 4A, a dielectric gate stack placeholder 432 is formed above a three-dimensional substrate 402 comprising a bulk semiconductor portion 402A and an isolation portion 402B. Etched-out regions 440 are formed in the exposed portions of bulk semiconductor portion 402A of three-dimensional substrate 402, as depicted in Figure 4B. In accordance with an embodiment of the present invention, a channel region 404 is retained underneath dielectric gate stack placeholder 432. Referring to Figure 4C, strain-inducing epitaxial source/drain regions 408 are formed selectively in etched-out regions 440, directly adjacent to channel region 404 and in direct contact with dielectric gate stack placeholder 432. A blanket dielectric layer 450 is then deposited above dielectric gate stack placeholder 432, strain-inducing epitaxial source/drain regions 408 and isolation portion 402B of three-dimensional substrate 402, as depicted in Figure 4D. Referring to Figure 4E, blanket dielectric layer 450 and the top portion of dielectric gate stack placeholder 43 are planarized to form inter-layer dielectric film 410 and planarized dielectric gate stack placeholder 434. Planarized dielectric gate stack placeholder 434 is then removed to form trench 460 in inter-layer dielectric film 410 and to expose channel region 404, as depicted in Figure 4F. Referring to Figure 4G, a gate dielectric layer 406 and a gate electrode 418 are then formed in trench 460. Therefore, tipless strain-inducing epitaxial source/drain regions may be incorporated into a trigate device by using a dielectric gate stack placeholder in a replacement gate integration scheme. The trigate device may be incorporated into an integrated circuit by conventional processing steps, as known in the art.

The present invention is also not limited to the formation of spacer-free semiconductor devices. A semiconductor gate stack placeholder may be used having thin outside dielectric spacers that inhibit deposition on the semiconductor gate stack placeholder during an epitaxial growth process. Figures 5A-B illustrate cross-sectional views representing the formation of a planar MOS-FET having tipless epitaxial

source/drain regions and dielectric spacers, in accordance with an embodiment of the present invention.

Referring to Figure 5A, a semiconductor gate stack placeholder 332 is provided having dielectric sidewall spacers 590. This structure corresponds with Figure 3B, described above, but with the added feature of dielectric sidewall spacers. In one embodiment, semiconductor gate stack placeholder 332 is comprised substantially of polycrystalline silicon and dielectric sidewall spacers 590 are comprised substantially of a dielectric material. Referring to Figure 5B, strain-inducing epitaxial source/drain regions 508 are formed on either side of dielectric sidewall spacers 590 and undercut both dielectric sidewall spacers 590 and replacement gate electrode 518. This structure corresponds with Figure 3J, described above, but with the added feature of dielectric sidewall spacers.

Thus, a semiconductor device having tipless epitaxial source/drain regions and a method for its formation have been disclosed. In an embodiment, the semiconductor device comprises a gate stack on a substrate. The gate stack is comprised of a gate electrode above a gate dielectric layer and is above a channel region in the substrate. The semiconductor device also comprises a pair of source/drain regions in the substrate on either side of the channel region. The pair of source/drain regions is in direct contact with the gate dielectric layer and the lattice constant of the pair of source/drain regions is different than the lattice constant of the channel region. In one embodiment, the semiconductor device is formed by using a dielectric gate stack placeholder.

What is claimed is:

1. A method of forming a semiconductor device, comprising:

forming a gate stack on a substrate, wherein said gate stack is comprised of a metal gate electrode above a channel region, and a high-k gate dielectric layer formed between said metal gate electrode and said channel region and along the sidewalls of said metal gate electrode;

forming a pair of source/drain regions on either side of said gate stack and in said substrate to define a channel region in said substrate, wherein said pair of source/drain regions is in direct contact with said high-k gate dielectric layer, and wherein the lattice constant of said pair of source/drain regions is different than the lattice constant of said channel region, said pair of source/drain regions formed with an undercut profile of approximately 55 degrees with respect to a horizontal axes;

forming regions of boron out-diffusion in said substrate and adjacent to the periphery of said pair of source/drain regions; and

forming an inter-layer dielectric film directly adjacent to the portions of said high-k gate dielectric layer along the sidewalls of said metal gate electrode.

2. The method of claim 1, wherein said channel region is comprised substantially of silicon atoms, and wherein said pair of source/drain regions is comprised substantially of silicon/germanium having an atomic concentration of germanium atoms in the range of 20-35%.

3. The method of claim 1, wherein the lattice constant of said pair of source/drain regions is different than the lattice constant of said channel region by a factor of at least 0.1%.