formed on a side wall of the first n-type diffusion layer 117 is larger than the sum of the thicknesses of the metal film 110b and polysilicon film 111b.

Even if the seventh resist is formed in a misaligned manner and the contact holes are formed by overetching, a short circuit between the contact 148 and the gate electrode 114b can be prevented.

[0080]

The center line of the gate line 114c is displaced from a line that connects the center point of the first pillar-shaped silicon layer 104 to the center point of the second pillar-shaped silicon layer 105 by a first predetermined distance.

The silicide 138 that connects the second n-type diffusion layer 118 to the second p-type diffusion layer 121 is easily formed. Therefore, high degree of integration can be achieved.

[0081]

In the present invention, various embodiments and modifications can be made without departing from the broad ~~sprit~~spirit and scope of the present invention. Furthermore, the above-described embodiment is provided to describe one embodiment of the present invention, and the scope of the present invention is not limited thereto.

[0082]

Claims

1. A method of producing a semiconductor device, the method which comprises the following:

a first step including forming a planar silicon layer on a silicon substrate, and

forming a first pillar-shaped silicon layer and a second pillar-shaped silicon layer on the planar silicon layer;

a second step, subsequent to the first step, including forming a gate insulating film around each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer,

forming a metal film and a polysilicon film around the gate insulating film, wherein a thickness of the polysilicon film is smaller than half a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer,

forming a resist, and

after forming the resist, forming a gate line by performing anisotropic etching of at least the polysilicon film, and

subsequent to performing the anisotropic etching, removing the resist; and

a third step, subsequent to the second step, including depositing a further resist so that a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer is exposed, removing the exposed portion of the polysilicon film by etching, removing the further resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode, wherein the first gate electrode and the second gate electrode are connected to the gate line.

2. The method for producing a semiconductor device according to claim 1, which comprises etching upper portions of the first pillar-shaped silicon layer and second pillar-shaped silicon layer by the anisotropic etching.

3. The method for producing a semiconductor device according to claim 1, wherein an upper surface of the resist for forming the gate line is located at a lower position than an upper surface of the polysilicon film on each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer.

4. The method for producing a semiconductor device according to claim 1, further comprising a fourth step including forming a first n-type diffusion layer in an upper portion of the first pillar-shaped silicon layer,

forming a second n-type diffusion layer in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer,

forming a first p-type diffusion layer in an upper portion of the second pillar-shaped silicon layer, and

forming a second p-type diffusion layer in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

5. The method for producing a semiconductor device according to claim 4, further comprising a fifth step including forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.

6~~11~~. The method for producing a semiconductor device according to claim 1, wherein the step of forming the gate line by performing anisotropic etching includes also removing portions of the metal film that are not protected by the resist.

7~~6~~. A semiconductor device, comprising:

a planar silicon layer formed on a silicon substrate;

first and second pillar-shaped silicon layers formed on the planar silicon layer;

a gate insulating film formed around the first pillar-shaped silicon layer;

a first gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

a gate insulating film formed around the second pillar-shaped silicon layer;

a second gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

a gate line connected to the first and second gate electrodes, wherein a center line of the gate line is displaced by a predetermined distance from a imaginary line joining a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer; and wherein the thickness of each of the polysilicon films being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer so that a portion of the gate line between the first and second pillar-shaped silicon layers also mutually connects the first and second gate electrodes;

an upper surface of the gate line being located at a lower position than upper surfaces of the first and second gate electrodes;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped silicon layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer;

a first p-type diffusion layer formed in an upper portion of the second pillar-shaped silicon layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

8~~7~~. The semiconductor device according to claim 6, wherein the gate line has a laminated structure of the metal film and a silicide.

9~~8~~. The semiconductor device according to claim 6, wherein the thickness of the insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the sum of the thicknesses of the metal film and polysilicon film.

~~9. The semiconductor device according to claim 6, wherein the center line of the gate line is displaced from a line that connects a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer by a first predetermined distance.~~

10. The semiconductor device according to claim 9, further comprising silicides formed on the first and second n-type diffusion layers and the first and second p-type diffusion layers.