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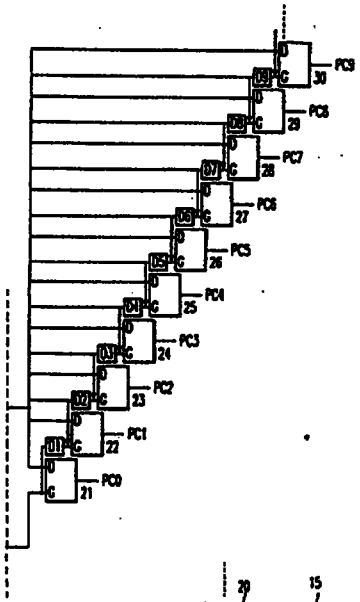
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(54) Title: POWER CONTROL STAGGERING

(57) Abstract

A power control circuit for a device such as personal computer, including a laptop or notebook computer, which can conserve battery use, prevent power surges to promote longer battery charges and longer battery life, and can assure that circuitry is correctly biased. The power control circuitry of the present invention achieves these objectives by appropriately staggering the powering on of circuit components of the computer. A circuit for achieving these objectives may feature at least one memory (20, 22, 24) for storing power control state data and a multiplexer (15) for receiving the power control state data stored in the at least one memory (20, 22, 24). Further, a plurality of serially connected power control output circuits (21-30) connected to the multiplexer (15) output power control signals based on the power control state data stored in the at least one memory (20, 22, 24). A first of the plurality of serially connected power control output circuits (21-30) has a minimum delay and each succeeding of the plurality of serially connected power control output circuits (21-30) has an increasing delay.



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