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(54) FIELD EFFECT TRANSISTOR AMPLIFIER CIRCUITS

(71) We, RCA CORPORATION, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention is directed to a self-biased multistage amplifier circuit, and more particularly to an amplifier in which the stages are direct coupled and in which addition of separate input signals is achieved in various stages of the amplifier.

It is to be recalled from Patent No. 1,157,759 of the same inventor that in a multistage amplifier useful for a.c. signal voltage amplification, there may be provided n stages cascaded in a direct coupled fashion. Each such stage of the amplifier includes a first insulated gate field effect transistor (such a device being hereinafter referred to as an IGFET) connected in the common source configuration and a series impedance connected to the drain electrode thereof, with the drain electrode of a transistor in one stage being directly coupled to the gate electrode of the transistor in the next succeeding stage. Self-biasing in such an amplifier is achieved by means of a feedback element coupled between the drain electrode of the last stage common source IGFET and the gate electrode of the first stage common source IGFET. With such an arrangement, conduction of the first stage common source IGFET is varied in response to drift signal changes occurring at the last stage output connection. In one of the amplifier stages (for example the first stage), the series impedance is the source-drain path of a second IGFET connected in the source-follower configuration, with the source electrode of the second transistor connected to the drain electrode of the first transistor of that same stage. When an in-

put signal voltage from a first source is applied to the input or gate electrode of the source-follower transistor, the source-drain path of the associated common source IGFET serves as a load impedance for the source-follower IGFET.

According to the invention we provide a direct coupled amplifier circuit which has: n stages connected in cascade, with each stage including a first insulated gate field effect transistor connected in the common source configuration and a series impedance coupled to the drain electrode thereof, and with the drain electrode of a transistor in each of the first $(n-1)$ stages being direct coupled to the gate electrode of a transistor in the next succeeding stage; and self-biasing means including a feedback element coupled between the drain electrode of the first transistor in the last stage and the gate electrode of the first transistor in the first stage; and in which: the series impedance of one stage is a second insulated gate field effect transistor connected in the source-follower configuration, with a source electrode thereof connected to the drain electrode of the first transistor of that stage; and with the gate electrode of the source-follower transistor isolated from the gate electrode of the common source transistor of the same stage and adapted for connection to an input signal source; wherein the series impedance of another stage is a further insulated gate field effect transistor connected in the source-follower configuration with the source electrode thereof connected to the drain electrode of the first transistor of that same stage; wherein the gate electrode of the said further transistor is adapted for connection to another input signal source that the another stage functions in common source mode with respect to signals applied to the one stage and in source-follower mode with respect to signals applied to the another stage; and wherein aforementioned one stage immediately precedes the aforementioned another stage, and wherein the an-

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other stage has unity voltage gain with respect to signals received at the gate electrode of its associated first transistor.

In the detailed description which follows, reference is made to the accompanying drawings in which:

Figure 1 is a schematic circuit diagram of a direct coupled amplifier of the type mentioned above and which is shown and claimed in Patent No. 1,157,759; and

Figure 2 is a schematic circuit diagram of an amplifier forming a preferred embodiment of the present invention.

In the description which follows, it is to be remembered that an IGFET may generally be defined as a majority carrier field effect device which includes a body of semiconductor material. A carrier conduction channel within the semiconductive body is bounded at one end thereof by a source region and at the other end thereof by a drain region. The gate or control electrode means overlies at least a portion of the carrier conduction channel and is separated therefrom by a region of insulating material. Due to the insulation between the gate electrode and the channel, the input impedance of the insulated gate field effect transistor is very large, being on the order of 10^{15} ohms or more, so that substantially no d.c. current flows in the gate electrode circuit. Thus, the insulated gate field effect transistor is a voltage controlled device. Signals or voltages applied to the gate electrode means control, by field effect, the conductance of the channel.

Such transistors may be of either the enhancement type or the depletion type. In a depletion type transistor there is current flow through the conduction channel when the source and gate electrodes have the same voltage ($V_{gs}=0$). This current flow either increases or decreases depending upon the polarity of the applied voltage between the gate and source electrodes. In an enhancement type transistor there is substantially no current flow through the conduction channel until V_{gs} is at least equal in magnitude to the threshold voltage V_t and of the same polarity as the drain-to-source voltage (V_{ds}).

An IGFET may be of either a P-type or an N-type transistor depending upon the majority carriers involved in drain current conduction. A P-type transistor is one in which the majority carriers are holes; whereas an N-type unit is one in which the majority carriers are electrons.

Direct coupled amplifier circuit embodying the present invention may be constructed either with discrete components or by means of integrated circuit processes. As used herein the term, integrated circuit, refers to those techniques by which an entire circuit can be formed as by diffusion or by thin films in or on one or more chips of suitable

substrate material. For example, in the case of metal oxide semiconductors (MOS) type IGFETs, the substrate material could be silicon; while for the case of thin film IGFETs, the substrate material could be an insulator, such as glass or sapphire. Direct coupled amplifiers are particularly suited for integrated circuit structures and devices, because they employ no a.c. coupling elements (such as transformers and capacitors), which elements at the present time either are impractical (as in the case of transformers) or not economically feasible (as in the case of capacitors) to fabricate in integrated form. Integrated circuit structures or chips upon which amplifiers are formed are useful as basic building blocks which may be interconnected and combined with appropriate power supplies and signal sources to form various signal translating systems.

Reference now is made to Figure 1, which shows a self-biased direct coupled amplifier circuit. The amplifier has n cascaded stages of amplification identified in a progressive order from the first stage to the last stage by the references $10_1, 10_2, \dots$, and 10_n . Each of the stages 10 is connected between a pair of supply connections 11 and 12 . The supply connection 11 is connected to the positive terminal of a source 13 of suitable operating potential, the negative terminal of which is connected to a point of fixed reference potential, illustrated in Figure 1 as circuit ground by the conventional symbol therefor. The source 13 , for example, may be a battery capable of providing a voltage of V_0 volts d.c. The supply connection 12 is connected to the fixed reference potential or circuit ground.

A source 19 of input signal voltage has an output terminal connected by way of a direct current conducting means, for example, a conductor, to the input connection 17_1 of the first stage 10_1 . The other terminal of the source 19 is connected to the ground reference by way of the supply connection 12 . The source 19 may be any suitable source for applying an a.c. input signal voltage e_s to the input connection 17_1 . The a.c. signal can be any time varying signal.

The amplifier stages 10_1 through 10_n are self-biased by means of direct coupling connections which connect the stages in cascade about a closed loop. To this end, the stage 10_1 has its output connection 15_1 connected to the input connection 17_2 of the second stage 10_2 , which in turn has its output connection 15_2 connected to the input of the third stage (not shown) and so on to form a direct coupled cascade amplifier. The output connection 15_n of the last stage 10_n is connected to an output terminal 50 , which in turn is connected to a suitable utilization device shown as a load 51 connected between

output terminal 50 and the ground reference by way of supply connection 12.

To complete the closed loop, the last stage output connection 15_n is further connected by way of a feedback path to a feedback point 18 at the first stage 10₁. The feedback path includes a suitable series feedback impedance 40. Although the impedance 40 may be a resistor, it preferably is the source-drain path of an insulated gate field-effect transistor, illustrated as a P-type IGFET. Transistor 40 has its source electrode 40s connected to the last stage output connection 15_n and its drain electrode 40d connected to the self-biasing point 18 for the first stage 10₁. The gate electrode 40g is connected to a suitable source of fixed voltage such as the V₀ volts supply connection 11. The feedback point 18 is also connected to the ground reference by way of a bypass filter capacitor 41, designated as C. It should be noted that the gate electrode 40g may be connected to any fixed voltage which biases IGFET 40 in such a manner so that its source-drain path exhibits a desired impedance value.

In the first stage 10₁, the amplifying device 20 is illustrated as a P-type IGFET connected in a common drain or source-follower configuration. To this end, the gate electrode 20g is connected to the first stage input connection 17₁. The drain electrode 20d is connected to the ground reference via the supply connection 12, while the source electrode 20s is connected both to the first stage output connection 15₁ and the source-drain path of another P-type IGFET 21 which serves as a series load impedance for the source-follower transistor 20. Transistor 21 has its drain electrode 21d connected to the first stage output connection 15₁ and its source electrode 21s connected to the supply connection 11. The gate electrode 21g is connected to the feedback point 18.

Each of the stages from 10₂ through 10_n have like circuit connections such that the following description of the stage 10₂ is applicable to the succeeding stages through stage 10_n. In stage 10₂, the amplifying device 14₂ is illustrated as a P-type IGFET connected in a common source configuration. To this end, the source electrode 14s₂ is connected to the supply connection 11, while the drain electrode 14d₂ is connected both to the second stage output connection 15₂ and a load impedance 16₂. The gate electrode 14g₂ is connected to the second stage input connection 17₂.

Although the load impedance 16₂ may be a resistor, it preferably takes the form of the source-drain path of a P-type enhancement IGFET. To this end, the source electrode 16s₂ is connected to the output connection 15₂ and the drain electrode 16d₂ is connected to the supply connection 12. The

gate electrode 16g₂ is connected to circuit ground by way of the supply connection 12. It should be noted that gate electrode 16g₂ should alternately be connected to some fixed potential other than the one to which drain electrode 16d₂ is connected so long as the fixed potential maintains IGFET 16₂ in a conductive condition throughout the range of linear amplification.

As mentioned previously, IGFET 16₂ is preferred over a resistor as the series load impedance for common source IGFET 14₂. This is because the illustrated IGFET stage 10₂ provides an extremely linear amplifier since the absolute value of the voltage gain is proportional to the relative linear dimensions of the IGFET's 14₂ and 16₂, which dimensions are easily controlled in integrated circuits. Assuming that the effective mobility μ of the carriers, the permittivity ϵ of the gate insulator and the thickness T of the gate insulator are the same for both IGFET's, the voltage gain G_v of the stage 10₂ (as well as the succeeding stages inclusive of stage 10_n) can be expressed as

$$G_v = -\sqrt{W_{14}L_{16}/W_{16}L_{14}} = -g_{m14}R_L \quad (1);$$

where W₁₄ and L₁₄ are the width and length, respectively, of the channel of IGFET 14, where W₁₆ and L₁₆ are the width and length, respectively, of the IGFET 16, where g_{m14} is the transconductance of IGFET 14 and where R_L is the load impedance. What this means is that G_v is essentially a constant so that as g_{m14} increases with applied signal voltage, R_L decreases at the same rate such that the product g_{m14}R_L remains constant throughout the range of linear amplification. For the case where the load impedance 16₂ is a constant-valued load resistor, the voltage gain product g_{m14}R_L varies directly with applied signal voltage since R_L is constant. Consequently, the linear amplifying range for the constant-valued resistor load stage is somewhat limited compared to that for the IGFET load stage. It should be noted that the IGFET load is sometimes referred to as a field-effect diode or MOS diode where MOS field-effect devices are employed.

The entire amplifier is self-biased by means of the source-drain path of the feedback IGFET 40 which sets up the d.c. voltage condition of V_{gs} equals V_{ds} for IGFET 21 for stage 10₁ and for each of the IGFET's 14 in the stages 10₂ through 10_n. This condition is achieved since there can be substantially no current flow through the source-drain path of IGFET 40 due to the insulated gate of IGFET 21 and the bypass capacitor 41. This feedback is essentially d.c. since the bypass capacitor 41 shorts the signal voltage to ground throughout the frequency range of interest, that is, IGFET

40 and capacitor 41 cooperate as a low pass filter to pass only d.c. or slowly varying signals, such as drift signals.

5 As is known, slowly varying signals or drift signals may occur due to factors internal to the amplifier such as thermal effects, threshold voltage changes, component aging, etc. or due to external factors such as supply voltage drift. The net effect of drift due to any of these factors is to cause a slowly varying drift signal ΔV at the output connection 15_n of the last stage 10_n. Assuming that such a drift signal is positive ($+\Delta V$) and that the number of stages n is an odd number, the $+\Delta V$ drift signal is fed back in a degenerative fashion so as to become self-correcting. That is, the feedback loop is operative to feed back an amplified drift signal which is out-of-phase with the drift signal ΔV . It should be noted that first stage IGFET 21 acts as a common source amplifier for drift signals with IGFET 20 as a load. For the case where the IGFET'S 20 and 16₂ through 16_n have substantially identical geometries and IGFET'S 21 and 14₂ through 14_n have substantially identical geometries, the feedback loop is operative to reduce the total drift to a value of

$$30 \quad -G_V \Delta V / (1 + G_V^n)$$

which is approximately equal to $-\Delta V$. It should be noted that the preceding discussion is concerned only with slowly varying d.c. or drift signals and is not indicative of the a.c. or signal gain. Assuming that the gain of the source-follower IGFET 20 is unity, the a.c. signal voltage gain is $1 + G_V^{n-1}$ such that the amplifier is non-inverting for signal voltage. It should be noted that for the case where the IGFET geometry differs from stage to stage, the a.c. signal gain becomes the product of the gains in each stage.

40 A general advantage of the amplifier is that the source impedance Z_s of source 19 is completely isolated from the low pass filter feedback network, whereby Z_s has no effect on the stability of the d.c. feedback network, and the amplifier input impedance is determined primarily by the input impedance of the source-follower IGFET 20. Due to the insulated gate of IGFET 20, the amplifier input impedance is extremely high, on the order of 10^{15} ohms or more, whereby the amplifier may be driven directly without the use of coupling capacitors or transformers from a very high impedance source which is referenced to ground. For example, the source 19 may be a parallel tuned circuit or a transducer, such as a microphone.

60 At the amplifier output terminal 50, no coupling capacitor or transformer is necessary so long as the load or utilization device 51 does not draw d.c. current. For loads

51 that are capable of drawing d.c. current, an a.c. coupling device should be used in order to prevent disruption of the d.c. bias conditions of the amplifier.

In the amplifier of Fig. 1 all of the IGFET's are preferably of the enhancement type since the d.c. operating condition of $V_{gs} = V_{ds}$ occurs in the linear portion of the transfer characteristic. For depletion type IGFET's, the operating point for $V_{gs} = V_{ds}$ generally occurs in the nonlinear portion of the transfer characteristic such that a non-linear amplifier results.

Automatic gain control (AGC) for the Fig. 1 amplifier may be achieved by providing an additional IGFET having its source-drain path connected as a feedback element in one of the internal stages 10₂ through 10_n. For example, the additional IGFET could have its source-drain path connected in stage 10₂ between the gate electrode 14g₂ and the drain electrode 14d₂ without disturbing the d.c. condition of $V_{gs} = V_{ds}$. Automatic gain control signals could be applied to the gate electrode of the additional IGFET.

As described above, the signal source 19 is preferably coupled to the gate electrode 20g of the first stage IGFET 20. However, the signal source 19 could just as well be coupled to the gate electrode of any of the load IGFET's of stages 10₂ through 10_n. For example, an inverting type amplifier could be obtained by connecting the signal source 19 between gate electrode 16g₂ of IGFET 16₂ in stage 10₂ and the grounded supply connection 12. The gate electrode 20g of IGFET 20 would then be coupled to supply connection 12.

Moreover, signal addition can be achieved by connecting two or more signal sources to different gate electrodes of the IGFET'S 20 and 16₂ through 16_n. For example, separate signal sources could be connected to the gate electrodes of IGFET 20 and IGFET'S 16₂ through 16_n and the stage gains (transistor geometries) could be weighted, that is, different gains, to obtain a desired linear signal addition at the output terminal 50.

The foregoing description of the Fig. 1 amplifier applies to the amplifier shown in Fig. 2, which is an embodiment of the present invention. The Fig. 2 amplifier accomplishes algebraic addition of input signals. More specifically the amplifier shown in Fig. 2 accomplishes signal subtraction (difference function) for two input signals, e_1 and e_2 .

It should be noted that various circuit elements shown in Fig. 2 which correspond to similar elements in the Fig. 1 amplifier are identified by reference numerals having corresponding units and tens digits and also having a hundreds digit. Thus, the IGFET 114₂ in stage 110₂ of Fig. 2 corresponds to IGFET 14₂ in stage 10₂ in Fig. 1. In Fig. 2,

the signal provided by the first signal source 119 is identified as e_1 instead of e_2 as for source 19 in Fig. 1.

Another signal source 122 of input signal voltage has an output terminal connected by way of a direct current conducting means, for example, a conductor, to one input connection 123 of the second stage 110₂. The other terminal of the source 122 is connected to the ground reference by way of the supply connection 112. The source 122 may be any suitable source for applying an a.c. or time varying input signal voltage e_2 to the input connection 123. The other connections for the stage 110₂ are similar to the connections for stage 10₂ of Fig. 1. The stages 110₃ through 110_n are similar to the stages 10₃ through 10_n of Fig. 1 as illustrated by stages 110₁ and 110_n such that a detailed description is unnecessary.

The stages 110₃ through 110_n operate as common source stages both for a.c. (input signals) and for d.c. (drift and other slowly varying signals) signals. The stage 110₁ operates as a source-follower for input signal e_1 and as a common source stage for d.c. signals. Finally, stage 110₂ acts as a source follower for input signal e_2 and as a common source stage both for signal e_1 and for d.c. signals. The voltage gain G for any of the stages 110₁ through 110_n then is given by equation (1).

The voltage gain of a source follower stage for an input signal is only slightly less than unity such that the source follower IGFETs 120 and 116₂ translate the associated input signals e_1 and e_2 to the first and second stage outputs 115₁ and 115₂, respectively, without appreciable amplification or attenuation.

The difference or signal subtraction function for input signals e_1 and e_2 is achieved at the second stage output 115₂ by utilizing the second stage IGFET 114₂ as a common source unity gain inverter for the signal e_1 . That is, the ratio of the linear dimensions of second stage transistors 114₂ and 116₂ in equation (1) is unity. Thus, the signals e_2 and e_1 are combined at the second stage output 115₂ to form a difference signal $e_2 - e_1$. The difference signal $e_2 - e_1$ is amplified by the remaining stages 110₃ through 110_n and translated to the load 151.

The operating or bias point for any of the amplifier stages 110₁ through 110_n is dependent on the gain of the stage. For instance, the d.c. drain voltage V_d of the common source IGFET is given by

$$V_d = V_o - V_T - G(V_g - V_T) \quad (2)$$

where V_o is the supply voltage, V_T is the threshold voltage of the common source IGFET, and V_g is the gate voltage of the common source IGFET. When all the stages have the same gain (or same ratio of linear

dimensions), V_d turns out to be equal to V_g for all stages in the amplifier. However, when one of the stages has unity gain (i.e., the ratio of linear dimension is one) and the other stages have gains appropriate to produce amplification, V_g and V_d are not identical for all stages to be biased in the high gain or active region of their respective transfer characteristics for linear amplification.

To obtain bias points for each stage in the Fig. 3 amplifier which permit a maximum signal swing in the linear or high gain region, the stage gains are built up symmetrically in each direction from the unity gain stage to a maximum gain. That is, the two stages 110₁ and 110₃ on either side of the unity gain stage 110₂ have identical gains which are larger than unity. Similarly, the gains of stages 110_n and 110₄ have identical gains which are larger than the gains of stages 110₁ and 110₃, and so on, until a maximum gain is achieved. It is noted that for an odd number of stages two of the stages have the maximum gain. The table below shows the ratios of the relative linear dimensions of the IGFETs in each stage for a seven stage amplifier optimized to obtain a maximum linear signal swing.

Ratios of Linear Dimensions
For Seven Stage Amplifier

Stage	Ratio
1	3.24
2	1
3	3.24
4	6.25
5	9.0
6	9.0
7	6.25

Although the symmetrical gain build-up about the self-biasing loop is optimum, it is to be understood that the difference amplifier stage gains need not be optimum. What is necessary to obtain a linear amplifier is that the gains in a given direction about the closed loop of stages of respective stages increase as a function of their removal from the unity gain stage to a maximum at the stage or stages most remote from the unity gain stage within the closed loop.

While the invention has been illustrated with P-type IGFETs, it is apparent that N-type IGFETs may also be employed so long as the polarity of the source of operating voltage is accordingly changed.

WHAT WE CLAIM IS:—

1. A direct coupled amplifier circuit which has: n stages connected in cascade,

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Another signal source 122 of input signal voltage has an output terminal connected by way of a direct current conducting means, for example, a conductor, to one input connection 123 of the second stage 110₂. The other terminal of the source 122 is connected to the ground reference by way of the supply connection 112. The source 122 may be any suitable source for applying an a.c. or time varying input signal voltage e_2 to the input connection 123. The other connections for the stage 110₂ are similar to the connections for stage 10₂ of Fig. 1. The stages 110₃ through 110_n are similar to the stages 10₃ through 10_n of Fig. 1 as illustrated by stages 110₃ and 110_n such that a detailed description is unnecessary.

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dimensions), V_d turns out to be equal to V_g for all stages in the amplifier. However, when one of the stages has unity gain (i.e., the ratio of linear dimension is one) and the other stages have gains appropriate to produce amplification, V_g and V_d are not identical for all stages to be biased in the high gain or active region of their respective transfer characteristics for linear amplification.

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WHAT WE CLAIM IS:—

1. A direct coupled amplifier circuit 120 which has: n stages connected in cascade,



with each stage including a first insulated gate field effect transistor connected in the common source configuration and a series impedance coupled to the drain electrode thereof, and with the drain electrode of a transistor in each of the first (n-1) stages being direct coupled to the gate electrode of a transistor in the next succeeding stage; and self-biasing means including a feedback element coupled between the drain electrode of the first transistor in the last stage and the gate electrode of the first transistor in the first stage; and in which: the series impedance of one stage is a second insulated gate field effect transistor connected in the source-follower configuration, with a source electrode thereof connected to the drain electrode of the first transistor of that stage; and with the gate electrode of the source-follower transistor isolated from the gate electrode of the common source transistor of the same stage and adapted for connection to an input signal source; wherein the series impedance of another stage is a further insulated gate field effect transistor connected in the source-follower configuration with the source electrode thereof connected to the drain electrode of the first transistor of that same stage; wherein the gate electrode of the said further transistor is adapted for connection to another input signal source so that the another stage functions in common source mode with respect to signals applied to the one stage and in source-follower

mode with respect to signals applied to the another stage; and wherein aforementioned one stage immediately precedes the aforementioned another stage, and wherein the another stage has unit voltage gain with respect to signals received at the gate electrode of its associated first transistor.

2. An amplifier circuit as claimed in claim 1, wherein within each of the remainder of said stages said series impedances are the source-drain path of respective additional insulated gate field effect transistors.

3. An amplifier circuit as claimed in claim 1 or 2, wherein the gains in a given direction about the closed loop of stages of respective stages increase as a function of their removal from the unity gain stage to a maximum at the stage or stages most remote from the unity gain stage within the closed loop.

4. An amplifier circuit as claimed in claim 3, wherein the stage gains are symmetrical with respect to the unity gain stage in either direction around the loop.

5. A direct coupled amplifier circuit substantially as described with reference to Figure 2 of the accompanying drawings.

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