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ABSTRACT OF THE DISCLOSURE

"Dual Loc Semiconductor Assembly Employing Floating Lead Finger Structure"

A method and apparatus for increasing integrated circuit density in a semiconductor die assembly, and specifically, a dual LOC semiconductor die assembly. A first and a second die are substantially symmetrically back bonded to a die attach site on a opposing sides of a base lead frame. A first and a second offset lead frame, each having a plurality of lead fingers, are then attached to the base lead frame on opposing sides thereof so that their lead fingers respectively extend over the first and second dice in a cantilevered manner. Wire bonds are formed between lead ends of each of the lead fingers to corresponding bond pads on the first and second dice for electrical connection therebetween. The assembly is then encapsulated in a transfer molding process, after which the stacked dual LOC semiconductor assembly is subjected to a trim and form operation.

[Fig. 1(h)]

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