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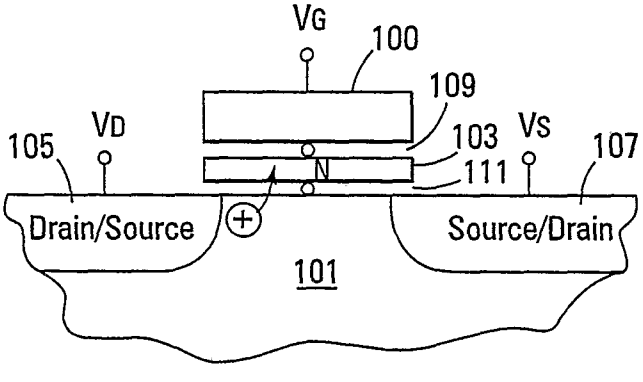
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(54) Title: MULTI-STATE MEMORY CELL WITH ASYMMETRIC CHARGE TRAPPING



(57) Abstract: A multi-state NAND memory cell is comprised of two drain/source areas in a substrate. An oxide - nitride - oxide structure is formed above the substrate between the drain/source areas. The nitride layer acting as an asymmetric charge trapping layer. A control gate is located above the oxide - nitride - oxide structure. An asymmetrical bias on the drain/source areas causes the drain/source area with the higher voltage to inject an asymmetric distribution hole by gate induced drain leakage injection into the trapping layer substantially adjacent that drain/source area.

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