ABSTRACT

METHOD TO DEPOSIT A COPPER SEED LAYER FOR DUAL DAMASCENE INTERCONNECTS

A new method of depositing a copper seed layer in the manufacture of an integrated circuit device has been achieved. The copper seed layer is thin and conformal and well-suited for subsequent electroless plating of copper. A dielectric layer, which may comprise a stack of dielectric material, is provided overlying a semiconductor substrate. The dielectric layer patterned to form vias and trenches for planned dual damascene interconnects. A barrier layer comprising tantalum, titanium, or tungsten is deposited overlying the dielectric layer to line the vias and trenches. A copper seed layer is deposited overlying the barrier layer by the reaction of CuF2 vapor with the barrier layer, and the integrated circuit is completed.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)