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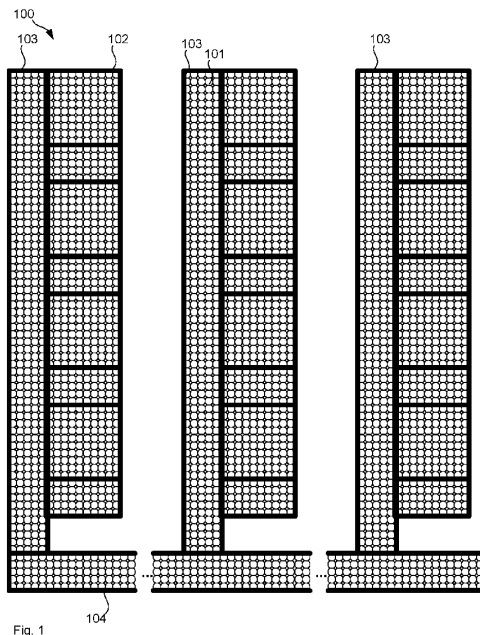
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(54) **Title: "QUANTUM ERROR CORRECTION"**



(57) **Abstract:** This disclosure relates to a quantum processor comprising multiple patches of digital qubits and a quantum bus of digital qubits. The quantum bus is configured to connect the multiple patches of digital qubits and to transmit quantum information constituting long-range interactions between the patches of digital qubits. The quantum processor is controlled by a first method of error correction on each of the patches connected by the bus to reduce a relatively high error rate in the digital qubits to a relatively low error rate of each patch, and by a second method of error correction on the multiple patches to correct the relatively low error rate. The number of patches can be increased to increase the distance of the second method and therefore reduce the final error rate. Due to the quantum bus, the patches can be arranged such that there is sufficient space between them for control circuitry.

WO 2022/082254 A1