low as about 2.5 Å or even about 2 Å as measured with an atomic force microscope (AFM) at scan sizes of about 1 µm x about 1 µm to about 100 µm x about 100 µm. For purposes of this specification, surface roughness is expressed as the root mean square (RMS) unless indicated otherwise. Rough polishing typically results in removal of about 1 µm to about 20 µm and, more typically, from about 5 µm to about 15 µm of material from the surface of the wafer.

[0023] The rough polish (and the finish polish described below) may be achieved by, for example, chemical-mechanical planarization (CMP). CMP typically involves the immersion of the wafer in an abrasive slurry and polishing of the wafer by a polymeric pad. Through a combination of chemical and mechanical action the surface of the wafer is smoothed. Typically the polish is performed until a chemical and thermal steady state is achieved and until the wafers have achieved their targeted shape and flatness. The rough polish may be performed on a double-side polisher commercially available from Peter Wolters (e.g., AC2000 polisher; Rendsburg, Germany) or Fujikoshi (Tokyo, Japan), Speedfam (Kanagawa, Japan). Stock removal pads for silicon polishing are available from Psiloquest (Orlando, Florida) and Dow Chemical Company (Midland, Michigan) and silica based slurries may be purchased from Dow Chemical Company, Cabot (Boston, Massachusetts), Nalco (Naperville, Illinois), Bayer MaterialScience (Leverkusen, Germany), DA NanoMaterials (Tempe, Arizona) and Fujimi (Kiyoso, Japan).

[0024] The rough polishing step may occur for about 300 seconds to about 60 minutes and at a pad pressure of from about 150 g/cm2 to about 700 g/cm2 with a slurry flow rate of about 50 ml/min to about 300 ml/min (or from about

[0031] One or more polishing slurries may be supplied to the polishing pad at various sequences at the first table (i.e., first polishing pad) of the polishing apparatus. In accordance with embodiments of the present disclosure, suitable slurries that may be used alone or in combination in the polishing sequences include a first polishing slurry comprising an amount of silica particles, a second polishing slurry also comprising an amount of silica particles but at a concentration less than the first slurry, a third polishing slurry that is alkaline (i.e., caustic) and typically does not contain silica particles and a fourth polishing slurry that is deionized water. In this regard, it should be noted that the term "slurry" as referenced herein denotes various suspensions and solutions (including solutions without particles therein such as caustic solution and deionized water) and is not intended to imply the presence of particles in the liquid.

[0032] The silica particles of the first and second slurries may be colloidal silica and the particles may be encapsulated in a polymer. Suitable first silica-containing polishing slurries include Syton-HT50 (Du Pont Air Products NanoMaterials; Tempe, Arizona) and DVSTS029 (Nalco Water; St. Paul, Minnesota). Suitable second silica-containing polishing slurries include Glanzox-3018 from (Fujimi; Tokyo, Japan) and NP 8020 (Nitta Haas; Osaka, Japan).

[0033] The concentration of silica in the first and second polishing slurries may be varied by using less silica particles in the second slurry. More typically, the concentration is varied by using silica particles that include less silica in the particles

off-set the increased edge roll-off due to increased lifetime of the pad. Alternatively, the amount of third slurry (i.e., alkaline slurry) may be adjusted.

[0061] In some embodiments, the polishing process is adjusted based on, at least in part, the measured flatness of the second semiconductor wafer. As shown in Figure 9, an increase in doming (i.e., the thickness difference between the wafer center and edge area) causes an increase in the edge roll-off. This increase may be off-set by decreasing the amount of first silica-containing polishing slurry supplied to the pad (e.g., relative to the second silica-containing slurry), such that the edge roll-off that occurs during the finish polish may be reduced. Alternatively, the amount of alkaline slurry may be adjusted.

[0062] As compared to conventional methods for polishing substrates, methods of the present disclosure have several advantages. By measuring the edge roll-off of a first semiconductor substrate or batch of substrates after a new polishing pad has been installed on the polishing table, the pad-to-pad variation of the pad may be determined which allows the polishing process to be adjusted for subsequently polished substrates. Deviations from the average expected roll-off for the polishing pad may be offset dynamically within the finish polish sequence by reducing or increasing the amount of polishing slurry containing silica or an alkaline polishing slurry. Adjusting the polishing process to account for the impact on edge roll-off attributed to the lifetime of the polishing pad and/or the flatness of the semiconductor to be polished allows the polishing process to be further

CLAIMS

1. A method for polishing semiconductor substrates, each substrate having a front surface and a back surface generally parallel to the front surface, the method comprising:

contacting the front surface of a first semiconductor substrate with a polishing pad;

supplying a first semiconductor substrate polishing slurry to the polishing pad to finish polish the front surface of the first semiconductor substrate and produce a polished first semiconductor substrate;

measuring the edge roll-off of the first semiconductor substrate;

contacting the front surface of a second semiconductor substrate with the polishing pad;

supplying a second semiconductor substrate polishing slurry to the polishing pad to finish polish the front surface of the second semiconductor substrate; and

controlling an amount of the second semiconductor substrate polishing slurry supplied to the polishing pad while contacting the second semiconductor substrate with the polishing pad based on, at least in part, the measured edge roll-off of the first semiconductor substrate.

2. The method as set forth in claim 1 wherein the first semiconductor substrate is one of a batch of semiconductor substrates, the method comprising:

contacting the front surface of each semiconductor substrate of the batch of semiconductor substrates with the polishing pad;

supplying the first semiconductor substrate polishing slurry to the polishing pad for each semiconductor substrate of the batch to finish polish the front surface of each of the semiconductor substrates of the batch to produce a batch of polished semiconductor substrates;

measuring the edge roll-off of each of the polished semiconductor substrates of the batch; and

controlling the amount of the second semiconductor substrate polishing slurry supplied to the polishing pad while contacting the second semiconductor substrate with the polishing pad based on, at least in part, the measured edge roll-off of the batch of polished semiconductor substrates.

3. The method as set forth in claim 2 wherein the measured edge roll-off of each of the polished semiconductor substrates of the batch is averaged, the amount of the second semiconductor substrate polishing slurry supplied to the polishing pad while contacting the second semiconductor substrate with the polishing pad being based on, at least in part, the averaged roll-off amount of the batch.

4. The method as set forth in claim 3 further comprising comparing the average edge roll-off of the batch of semiconductor substrates to an average edge roll-off of polishing pads that are the same as the polishing pad used to polish the first semiconductor substrate to determine a pad-to-pad variance of the polishing pad.

5. The method as set forth in claim 2 wherein the batch comprises at least 5 semiconductor substrates.

6. The method as set forth in claim 1 wherein the amount of the second semiconductor substrate polishing slurry supplied to the polishing pad while contacting the second semiconductor substrate with the polishing pad is controlled based on, at least in part, the lifetime of the polishing pad.

7. The method as set forth in claim 1 wherein the amount of the second semiconductor substrate polishing slurry supplied to the polishing pad while contacting the second semiconductor substrate with the polishing pad is controlled based on, at least in part, the flatness of the second semiconductor substrate.

8. The method as set forth in claim 1 wherein the second semiconductor substrate polishing slurry is supplied in at least two steps, the second semiconductor substrate polishing slurry being a first step polishing slurry comprising silica, the first step polishing slurry being supplied to the polishing pad at a first step polishing slurry volume, the method further comprising:

supplying a second step polishing slurry to the polishing pad at a second step polishing slurry volume, the first step polishing slurry comprising a higher concentration of silica relative to the second step polishing slurry, wherein the amount of the first step polishing slurry supplied to the polishing pad is controlled by controlling a ratio of the first step polishing slurry volume to the second step polishing slurry volume.

9. The method as set forth in claim 8 wherein the second step polishing slurry comprises silica.

10. The method as set forth in claim 8 wherein the ratio of the first step polishing slurry volume to the second step polishing slurry volume is controlled by controlling the time at which the first step polishing slurry and second step polishing slurry are applied to the polishing pad.

11. The method as set forth in claim 8 wherein the first step polishing slurry and the second step polishing slurry are separately supplied to the polishing pad.

12. The method as set forth in claim 1 wherein the amount of second semiconductor polishing slurry supplied to the polishing pad is the total amount of second semiconductor polishing slurry supplied while polishing at a first table of a polishing apparatus, the method comprising transferring the substrate to a second table of the polishing apparatus.

13. The method as set forth in claim 1 wherein the back surfaces of the first and second semiconductor substrates are not contacted with a polishing pad while polishing the front surface of the substrate.

14. The method as set forth in claim 1 wherein:

the finish polish of the first semiconductor substrate removes about 0.5 μm or less of material from the front surface of the first semiconductor substrate; and

the finish polish of the second semiconductor substrate removes about 0.5 μm or less of material from the front surface of the second semiconductor substrate.

15. The method as set forth in claim 1 wherein the first semiconductor substrate is one of the first five, first ten or first twenty substrates polished by the polishing pad.

16. The method as set forth in claim 1 wherein the first semiconductor substrate is the first substrate polished by the polishing pad.

17. The method as set forth in claim 1 wherein the amount of the second semiconductor substrate polishing slurry supplied to the polishing pad while contacting the second semiconductor substrate with the polishing pad is based on, at least in part, the difference between the measured edge roll-off of the first semiconductor substrate and the average edge roll-off of the same polishing pads.