(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 May 2006 (18.05.2006)

PCT

(10) International Publication Number
WO 2006/052992 A2

(51) International Patent Classification:
G06F 11/00 (2006.01)

(21) International Application Number:
PCT/US2005/040478

(22) International Filing Date:
7 November 2005 (07.11.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/626,120 8 November 2004 (08.11.2004) US

(71) Applicant *(for all designated States except US)*: **ZMOS TECHNOLOGY, INC.** [US/US]; 1290 Oakmead Parkway, Suite 318, Sunnyvale, CA 94085 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **SOHN, Joeng-duk** [KR/US]; 1841 Paseo Del Cajon, Pleasanton, CA 94566 (US). **KIM, Young, Tae** [KR/US]; 390 Elan Village Lane #110, San Jose, CA 95134 (US).

(74) Agent: **O'BANION, John, P.**; O'banion & Ritchey LLP, Suite 1550, 400 Capitol Mall, Sacramento, CA 95814 (US).

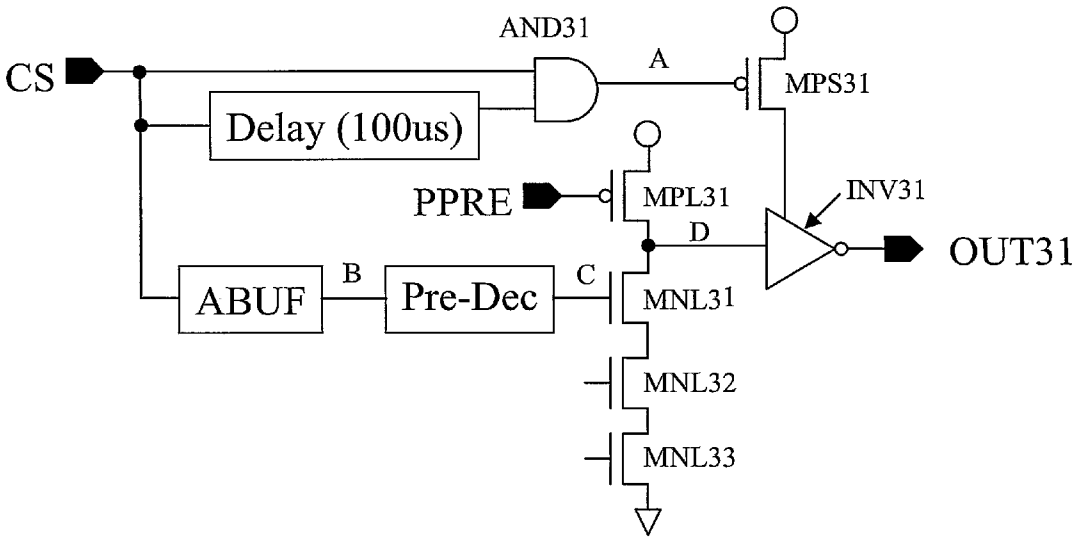
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** HIGH SPEED AND LOW POWER SRAM MACRO ARCHITECTURE AND METHOD



(57) **Abstract:** Circuits and methods are described for reducing leakage power in integrated circuit devices whose logic transistors (e.g., logic circuits, latches, and/or output stages) are powered through one or more controllable source transistors. By way of example the circuit has at least one source transistor (e.g., power, ground, or both power and ground) for selectively supplying power to a stage within an integrated circuit device. A means for modulating the state of the source transistor operates in response to changes in the operating mode of the integrated circuit to turn on the source transistor prior to turning on the logic transistors, and/or to turn off the source transistor after turning off the logic transistors. In one aspect, the delay prior to turning off the logic transistors can be sufficiently extended to reduce power consumption arising from unnecessarily turning on and off the source transistors for short periods.

WO 2006/052992 A2