CLAIMS:

1. A semiconductor structure comprising:
a plurality of silicon pillars in a substrate; and
a plurality of trenches isolating each silicon pillar of the plurality of silicon pillars, wherein at least one of the plurality of trenches or the plurality of silicon pillars has a width of less than 44 nm.

2. The semiconductor structure of claim 1, wherein the width of the each pillar of the plurality of silicon pillars and the width of each trench of the plurality of trenches is less than 44 nm.

3. A semiconductor structure comprising a plurality of active areas separated by isolation regions, the plurality of active areas including recessed access device trenches therein respectively having a width of less than a minimum feature size.

4. The semiconductor structure of claim 3, wherein the width of the isolation regions is less than the minimum feature size.

5. The semiconductor structure of claim 3, wherein the width of the plurality of active areas is less than the minimum feature size.

6. The semiconductor structure of claim 3, further comprising conductive gate material within the recessed access device trenches and a plurality of conductive lines elevationally outward of the plurality of active areas and recessed access device trenches, some of the conductive lines connecting with the conductive gate material within the recessed access device trenches.

7. The semiconductor structure of claim 1, wherein the trenches comprise insulative material therein.

8. The semiconductor structure of claim 7, wherein the insulative material fills the trenches.

9. The semiconductor structure of claim 2, wherein the width of the each pillar of the plurality of silicon pillars and the width of each trench of the plurality of trenches are equal.

10. The semiconductor structure of claim 6, wherein the conductive lines have widths of less than the minimum feature size.

11. The semiconductor structure of claim 6, wherein the conductive lines run parallel the recessed access device trenches.

12. The semiconductor structure of claim 6, wherein another some of the conductive lines do not connect with the conductive gate material within the recessed access device trenches.

13. The semiconductor structure of claim 12, wherein the another some of the conductive lines have widths of less than the minimum feature size.

14. The semiconductor structure of claim 12, wherein the another some of the conductive lines comprise grounded gate lines.

15. The semiconductor structure of claim 14, wherein the grounded gate lines have widths of less than the minimum feature size.

16. The semiconductor structure of claim 6, wherein the some gate lines comprise word lines, and further comprising another some of the conductive lines which comprise grounded gate lines, two of the word lines being received between two immediately adjacent of the grounded gate lines.

17. The semiconductor structure of claim 16, wherein the grounded gate lines have widths of less than the minimum feature size.

18. The semiconductor structure of claim 16, wherein the word lines have widths of less than the minimum feature size.

19. The semiconductor structure of claim 16, wherein the word lines have widths of less than the minimum feature size and the grounded gate lines have widths of less than the minimum feature size.

CLAIMS:

1. A semiconductor structure comprising:
a plurality of silicon pillars in a substrate; and
a plurality of trenches isolating each silicon pillar of the plurality of silicon pillars, wherein the plurality of trenches and the plurality of silicon pillars have equal width of less than 44 nm.

2. A semiconductor structure comprising a plurality of active areas separated by isolation regions, the plurality of active areas including recessed access device trenches therein respectively having a width of less than a minimum feature size, a transistor gate being within individual of the recessed access device trenches, the width of the plurality of active areas laterally outward of the transistor gates being less than the minimum feature size.

3. The semiconductor structure of claim 2, wherein the width of the isolation regions is less than the minimum feature size.

4. A semiconductor structure comprising:
a plurality of active areas separated by isolation regions,
the plurality of active areas including recessed access device trenches therein respectively having a width of less than a minimum feature size;
conductive gate material within the recessed access device trenches; and
a plurality of conductive lines elevationally outward of the plurality of active areas and recessed access device trenches, some of the conductive lines connecting with the conductive gate material within the recessed access device trenches.

5. The semiconductor structure of claim 1, wherein the trenches comprise insulative material therein.

6. The semiconductor structure of claim 5, wherein the insulative material fills the trenches.

7. The semiconductor structure of claim 4, wherein the conductive lines have widths of less than the minimum feature size.

8. The semiconductor structure of claim 4, wherein the conductive lines run parallel the recessed access device trenches.

9. A semiconductor structure comprising a plurality of active areas separated by isolation regions, the plurality of active areas including recessed access device trenches therein respectively having a width of less than a minimum feature size, conductive gate material within the recessed access device trenches; and
a plurality of conductive lines elevationally outward of the plurality of active areas and recessed access device trenches, some of the conductive lines connecting with the conductive gate material within the recessed access device trenches, another some of the conductive lines not connecting with the conductive gate material within the recessed access

device trenches.

10. The semiconductor structure of claim 9, wherein the another some of the conductive lines have widths of less than the minimum feature size.

11. The semiconductor structure of claim 9, wherein the another some of the conductive lines comprise grounded gate lines.

12. The semiconductor structure of claim 11, wherein the grounded gate lines have widths of less than the minimum feature size.

13. A semiconductor structure comprising a plurality of active areas separated by isolation regions, the plurality of active areas including recessed access device trenches therein respectively having a width of less than a minimum feature size, conductive gate material within the recessed access device trenches; and
a plurality of conductive lines elevationally outward of the plurality of active areas and recessed access device trenches, some of the conductive lines connecting with the conductive gate material within the recessed access device trenches, the some of the conductive lines comprising word lines, and further comprising another some of the conductive lines which comprise grounded gate lines, two of the word lines being received between two immediately adjacent of the grounded gate lines.

14. The semiconductor structure of claim 13, wherein the grounded gate lines have widths of less than the minimum feature size.

15. The semiconductor structure of claim 13, wherein the word lines have widths of less than the minimum feature size.

16. The semiconductor structure of claim 13, wherein the word lines have widths of less than the minimum feature size and the grounded gate lines have widths of less than the minimum feature size.

17. The semiconductor structure of claim 2, wherein the isolation regions comprise conductive lines.

18. The semiconductor structure of claim 2, wherein the isolation regions comprise dielectric material.

19. The semiconductor structure of claim 18, wherein the dielectric material comprises oxide.