CLAIM

What is claimed is:

1. A circuit package comprising:

an electronic integrated circuit comprising a plurality of processing elements, each processing element comprising a message router including photonic-channel interfaces; and

a plurality of bidirectional photonic channels connecting the processing elements into an electro-photonic network, each bidirectional photonic channel interfacing at a first end with a photonic-channel interface of the message router of a first one of the processing elements and at a second end with a photonic-channel interface of the message router of a second one of the processing elements and being configured to optically transfer a packet between the message routers of the first and second processing elements,

wherein each bidirectional photonic channel comprises one or more unidirectional photonic links in both directions, and

wherein each unidirectional photonic link comprises an optical modulator at an input end, a photodetector at an output end, and an optical waveguide connecting the optical modulator to the photodetector, and wherein each photonic-channel interface comprises a modulator driver for each unidirectional photonic link with which it interfaces at the input end and a transimpedance amplifier for each unidirectional photonic link with which it interfaces at the output end.

2. The circuit package of claim 1, wherein each bidirectional photonic channel comprises multiple unidirectional photonic links in both directions, and wherein the multiple unidirectional photonic links in each direction are bonded together.

3. The circuit package of claim 1, wherein the optical modulators are electro-absorption modulators (EAMs).

4. The circuit package of claim 1, wherein the optical modulators comprise at least one of a ring modulator, Mach-Zehnder modulator, quantum-confined Stark effect (QCSE) electro-absorption modulator.

5. The circuit package of claim 1, wherein the electronic integrated circuit is implemented in an electronic circuit layer and the plurality of bidirectional photonic channels are implemented in a photonic circuit layer.

6. The circuit package of claim 5, wherein the electronic circuit layer is implemented in a first semiconductor chip and the photonic circuit layer is implemented in a second semiconductor chip.

7. The circuit package of claim 5, wherein each modulator driver is placed directly above or below the optical modulator with which it is associated and each transimpedance amplifier is placed directly above or below the photodetector with which it is associated.

8. The circuit package of claim 6, wherein distances between the optical modulators and their associated modulator drivers and between the photodetectors and their associated transimpedance amplifiers are smaller than 200 μm.

9. The circuit package of claim 6, further comprising, in the photonic circuit layer of the semiconductor chip, optical input waveguides supplying optical carrier signals provided by one or more laser light sources to the optical modulators of the photonic links, the optical carrier signals being modulated by the optical modulators in accordance with drive signals applied by the associated modulator drivers to generate modulated optical signals carrying the packet.

10. The circuit package of claim 9, further comprising the one or more laser light sources integrated into the circuit package.

11. The circuit package of claim 10, wherein the one or more laser light sources are integrated with the optical input waveguides in one or more photonic integrated circuits (PICs) in the photonic circuit layer.

12. The circuit package of claim 10, wherein the one or more laser light sources are implemented in an interposer co-packaged with the semiconductor chips and are edge-coupled with one or more PICs in the photonic circuit layer that include the optical input waveguides.

13. The circuit package of claim 9, wherein the one or more laser light sources are implemented externally to the circuit package and optically coupled via one or more optical fibers to one or more PICs in the circuit package.

14. The circuit package of claim 13, wherein the one or more optical fibers are coupled to the one or more PICs via one or more fiber attach units (FAUs) located over grating couplers implemented in the PICs.

15. The circuit package of claim 13, wherein the one or more optical fibers are edge-coupled to the one or more PICs.

16. The circuit package of claim 13, further comprising, in the photonic circuit layer of the semiconductor chip, one or more optical splitters each splitting an input optical carrier signal received from an associated one of the one or more laser light sources between multiple of the input optical waveguides.

17. The circuit package of claim 1, wherein the electronic integrated circuit is an application-specific integrated circuit (ASIC).

18. The circuit package of claim 17, wherein the ASIC comprises digital and mixed-signal electronic circuitry.

19. The circuit package of claim 17, wherein each processing element further comprises a dot product engine implementing a combinatorial tree of multipliers and adders for computing dot products between vectors.

20. The circuit package of claim 19, wherein each processing element further comprises a tensor engine for obtaining and processing vectors computed as output of the dot product engine.

21. The circuit package of claim 19, wherein each processing element further comprises a memory system.

22. The circuit package of claim 17, further comprising at least one of a peripheral component interconnect express (PCIE) interface, an advanced RISC machine core, an image processor, or an external memory controller.

23. The circuit package of claim 17, further comprising high bandwidth memory (HBM), the ASIC further comprising a RAM controller communicatively coupling the processing elements to the HBM.

24. The circuit package of claim 1, wherein the message routers of the processing elements are configured to route a packet having routing information in a portion of the packet, wherein a path through the electro-photonic network is determined by using the routing information.

25. The circuit package of claim 24 wherein the message router of each processing element is configured to determine, based on the routing information in the packet received on one of its photonic-channel interfaces, a destination of the packet, and to route the packet either to a local port if the destination is a local memory or a processing engine within the processing element or to another one of the photonic-channel interfaces if the destination is not the local memory or processing engine within the processing element.

26. The circuit package of claim 24, wherein the processing elements are arranged in a regular grid, and wherein the routing information in the packet

specifies relative locations in first and second dimensions along the grid to a processing element that is a destination of the packet.

27. The circuit package of claim 26, wherein each bidirectional photonic channels connects a pair of immediately adjacent processing elements in the grid in one of the first dimension or the second dimension, and wherein the message router of each processing element is configured to decrement a value in the routing information associated with the relative location in the first dimension when routing the packet to an immediately adjacent processing element along the first dimension and to decrement a value in the routing information associated with the relative location in the second dimension when routing the packet to an immediately adjacent processing element along the second dimension.

28. The circuit package of claim 24, wherein the plurality of bidirectional photonic channels are configured to connect the processing elements into an electro-photonic network having a grid topology defining at least two dimensions, wherein the routing information in the packet specifies coordinates in the at least two dimensions relative to a processing element that is a destination of the packet, and wherein the message router of each processing element, when routing the packet to a topologically immediately adjacent processing element along one of the at least two dimensions, modifies the routing information in the packet by decrementing a value associated with one of the at least two dimensions.

29. The circuit package of claim 1, wherein the electronic circuit is configured as an arrangement of tiles each corresponding to one of the processing elements.

30. The circuit package of claim 29, wherein the tiles are rectangular tiles arranged in a rectangular grid.

31. The circuit package of claim 30, wherein the plurality of bidirectional photonic channels is configured to directly connect each pair of immediately

adjacent tiles in the rectangular grid to result in a quadrilateral mesh topology of the electro-photonic network.

32. The circuit package of claim 31, wherein the plurality of bidirectional photonic channels is configured to further directly connect one or more pairs of non-adjacent tiles in the rectangular grid.

33. The circuit package of claim 31, further comprising bidirectional photonic channels configured to directly connect pairs of tiles on opposite edges of the rectangular grid to result in a wrapped toroidal mesh topology of the electro-photonic network.

34. The circuit package of claim 1, wherein the bidirectional photonic channels are configured to connect the processing elements into an electro-photonic network having a cubic grid topology.