

Description

Title of the Invention: DEPOSITION METHOD AND
DEPOSITION APPARATUS

5 Technical Field

[0001] The present invention relates to a deposition method and a deposition apparatus.

Background Art

[0002] Electronic devices typified by 3D-NAND flash
10 memories are becoming more multi-layered and the number of layers tends to increase more and more. For this reason, the deposition method of a coating film (e.g., an insulation layer) included in the multilayer structure is particularly important.

15 [0003] As a method of forming a coating film, there is a sputtering method, which has a relatively high deposition rate and exhibits a favorable film thickness distribution. Among these, there is a sputtering method in which high-frequency power is supplied to the
20 sputtering target side and the substrate side and the phases of the respective high-frequency power sources are controlled to improve the deposition rate and film thickness distribution (see, for example, Patent Literature 1).

25 Citation List

Patent Literature

[0004] Patent Literature 1: Japanese Patent

Application Laid-open No. 1996-302467

Disclosure of Invention

Technical Problem

5 [0005] However, the embedding characteristics of the coating film formed by the deposition method described above change in some cases depending on the phase of the high-frequency power supplied to the substrate side. For this reason, an optimum condition with
10 improved step coverage of the coating film is desired.

[0006] In view of the circumstances as described above, it is an object of the present invention to provide a deposition method and a deposition apparatus with improved step coverage of a coating film.

15 Solution to Problem

[0007] In order to achieve the above-mentioned object, in a deposition method according to an embodiment of the present invention, a deposition apparatus including a first electrode, a second
20 electrode, a first power supply source, a second power supply source, and a phase adjuster is used.

The first electrode includes a sputtering target.

The second electrode faces the first electrode and is capable of supporting a substrate.

25 The first power supply source includes a first high-frequency power source and a first matching

circuit, the first high-frequency power source outputting first high-frequency power, the first matching circuit being connected between the first high-frequency power source and the first electrode.

5 The second power supply source includes a second high-frequency power source and a second matching circuit, the second high-frequency power source outputting second high-frequency power that has the same period as the first high-frequency power and is
10 lower than the first high-frequency power, the second matching circuit being connected between the second high-frequency power source and the second electrode and including an input terminal, an output terminal, a first variable capacitor, and a second variable
15 capacitor, the input terminal being connected to the second high-frequency power source, the output terminal being connected to the second electrode, the first variable capacitor being connected between the input terminal and a ground potential, the second variable
20 capacitor being connected between the input terminal and the output terminal in series.

 The phase adjuster adjusts a phase of the first high-frequency power that is output from the first high-frequency power source and input to the first
25 matching circuit and a phase of the second high-frequency power that is output from the second high-

frequency power source and input to the second matching circuit.

The first high-frequency power source is caused to output the first high-frequency power to form discharge plasma between the first electrode and the second electrode.

The second high-frequency power source is caused to output the second high-frequency power and the phase adjuster is caused to operate to provide a phase difference θ between the phase of the first high-frequency power and the phase of the second high-frequency power.

A voltage value V_{pp} of the second high-frequency power and a capacitance value $C1$ of the first variable capacitor that correspond to the phase difference θ in a state where output impedance of the second high-frequency power source and load-side impedance connected to the second high-frequency power source match are detected.

The voltage value V_{pp} and the capacitance value $C1$ are selected in combination in a predetermined range of the phase difference θ to form a sputtering film on the substrate.

[0008] According to such a deposition method, a sputtering film with excellent step coverage is formed.

[0009] In the deposition method,

the phase difference θ may be formed by delaying the phase of the second high-frequency power with respect to the phase of the first high-frequency power;

a profile curve of the voltage value V_{pp} and a
5 profile curve of the capacitance value C_1 that correspond to the phase difference θ may be obtained by changing the phase difference θ ; and

the phase difference θ may be set in a first range or a second range and forming the sputtering film may
10 be formed on the substrate in a state where the output impedance and the load-side impedance match, the first range being a range of +30 degrees to +50 degrees from a phase difference θ_1 of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the
15 lowest, the second range being a range of +10 degrees to -10 degrees from a phase difference θ_2 of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the largest.

[0010] According to such a deposition method, a
20 sputtering film with excellent step coverage is formed.

[0011] In the deposition method, the sputtering film may be formed on the substrate by changing the phase difference θ in a stepwise manner in the first range or the second range.

25 [0012] According to such a deposition method, a sputtering film with low damage and excellent step

coverage is formed.

[0013] In the deposition method, after forming the sputtering film on the substrate in the first range or the second range, the sputtering film may be formed on the substrate in a third range in which the phase difference θ is smaller than the second range and larger than the first range.

[0014] According to such a deposition method, a sputtering film with low damage and excellent step coverage is formed.

[0015] In the deposition method, the third range may be a range of -50 degrees to -30 degrees from the phase difference θ_2 .

[0016] According to such a deposition method, a sputtering film with low damage and excellent step coverage is formed.

[0017] In order to achieve the above-mentioned object, a deposition apparatus according to an embodiment of the present invention, the controller stores data obtained by causing the first high-frequency power source to output the first high-frequency power to form discharge plasma between the first electrode and the second electrode, causing the second high-frequency power source to output the second high-frequency power and causing the phase adjuster to operate to provide a phase difference θ between the

phase of the first high-frequency power and the phase of the second high-frequency power, and detecting a voltage value V_{pp} of the second high-frequency power and a capacitance value C_1 of the first variable capacitor that correspond to the phase difference θ in a state where output impedance of the second high-frequency power source and load-side impedance connected to the second high-frequency power source match.

The controller selects the voltage value V_{pp} and the capacitance value C_1 in combination in a predetermined range of the phase difference θ to form a sputtering film on the substrate.

[0018] According to such a deposition apparatus, a sputtering film with excellent step coverage is formed.

[0019] In the deposition apparatus, the controller may store a profile curve of the voltage value V_{pp} and a profile curve of the capacitance value C_1 that correspond to the phase difference θ obtained by forming the phase difference θ by delaying the phase of the second high-frequency power with respect to the phase of the first high-frequency power and changing the phase difference θ .

The controller may set the phase difference θ in a first range or a second range and form the sputtering film on the substrate in a state where the output

impedance and the load-side impedance match, the first range being a range of +30 degrees to +50 degrees from a phase difference θ_1 of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the lowest, the second range being a range of +10 degrees to -10 degrees from a phase difference θ_2 of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the largest.

[0020] According to such a deposition apparatus, a sputtering film with excellent step coverage is formed.

[0021] In the deposition apparatus, the sputtering film may be formed on the substrate by changing the phase difference θ in a stepwise manner in the first range or the second range.

[0022] According to such a deposition apparatus, a sputtering film with excellent step coverage is formed.

[0023] In the deposition apparatus, after forming the sputtering film on the substrate in the first range or the second range, the sputtering film may be formed on the substrate in a third range in which the phase difference θ is smaller than the second range and larger than the first range.

[0024] According to such a deposition apparatus, a sputtering film with excellent step coverage is formed.

[0025] In the deposition apparatus, the third range may be a range of -50 degrees to -30 degrees from the

phase difference θ_2 .

[0026] According to such a deposition apparatus, a sputtering film with excellent step coverage is formed.

Advantageous Effects of Invention

5 [0027] As described above, according to the present invention, a deposition method and deposition apparatus with improved step coverage of a coating film are provided.

Brief Description of Drawings

10 [0028] [Fig. 1] Fig. 1 is a schematic block configuration diagram showing an example of a deposition apparatus according to this embodiment.

[Fig. 2] Part (a) of Fig. 2 is a graph describing an example of a profile curve of a voltage value V_{pp} .

15 Part (b) of Fig. 2 is a graph describing an example of a profile curve of a capacitance value C_1 .

[Fig. 3] Part (a) of Fig. 3 is a cross-sectional SEM image of a recessed pattern before a sputtering film is formed. Part (b) to Part (e) of Fig. 3 are each
20 a cross-sectional SEM image of the sputtering film after the sputtering film is formed in the recessed pattern.

[Fig. 4] Fig. 4 shows profile curves of the voltage value V_{pp} and the capacitance value C_1 in a
25 test A.

[Fig. 5] Fig. 5 is a cross-sectional SEM image of

the sputtering film after the sputtering film is formed in the recessed pattern.

[Fig. 6] Fig. 6 shows profile curves of the voltage value V_{pp} and the capacitance value C_1 according to a modified example 2.

[Fig. 7] Parts (a) and (b) of Fig. 7 are each a schematic cross section showing a deposition method according to the modified example 2. Part (c) of Fig. 7 is a cross-sectional SEM image of a sputtering film after a sputtering film is formed in a recessed pattern.

Mode(s) for Carrying Out the Invention

[0029] An embodiment of the present invention will be described below with reference to the drawings.

Further, the same members or members having the same function will be denoted by the same reference symbols in some cases, and the description will be omitted as appropriate in some cases after describing the members. Further, numerical values shown below are examples and the present invention is not limited to these examples.

[0030] (Deposition apparatus)

[0031] Fig. 1 is a schematic block configuration diagram showing an example of a deposition apparatus according to this embodiment.

[0032] A deposition apparatus 1 includes an electrode 11 (first electrode), an electrode 12 (second

electrode), a power supply source 21 (first power supply source), a power supply source 22 (second power supply source), a phase adjuster 50, and a controller 60.

5 [0033] The electrode 11 includes a sputtering target 111 and a back plate (support plate) 112. The sputtering target 111 contains a coating material to be sputter-deposited on a substrate 121. Examples of the coating material include alumina, an insulator such as
10 silicon oxide, and a metal such as aluminum. The back plate 112 is formed of, for example, a conductive metal.

[0034] The electrode 12 faces the electrode 11. The electrode 12 functions also as a support stand capable
15 of supporting the substrate 121. An electrostatic chuck may be provided on the support surface of the electrode 12 supporting the substrate 121. The substrate 121 includes a semiconductor wafer, a silicon oxide layer, and the like. Patterns such as lines and spaces and
20 through holes are formed on the deposition surface of the substrate 121 facing the electrode 11.

[0035] The power supply source 21 includes a high-frequency power source 31 (first high-frequency power source) and a matching circuit 41 (first matching
25 circuit). The high-frequency power source 31 outputs first high-frequency power. The first high-frequency

power is typically RF power of 13.56 MHz. For example, 100 W to 5000 W can be output.

[0036] The matching circuit 41 is connected between the high-frequency power source 31 and the electrode 11. The matching circuit 41 includes an input terminal 415, an output terminal 416, a variable capacitor 411, a variable capacitor 412, and an inductance 413. The input terminal 415 is connected to the high-frequency power source 31. The output terminal 416 is connected to the electrode 11. The variable capacitor 411 is connected to the input terminal 415 and a ground potential. The variable capacitor 412 is connected between the input terminal 415 and the output terminal 416 in series. The inductance 413 is connected to the variable capacitor 412 between the input terminal 415 and the output terminal 416 in series. Each of the variable capacitor 411 and the variable capacitor 412 of the matching circuit 41 is driven by the controller 60 to perform automatic matching in which the output impedance of the high-frequency power source 31 and the load-side impedance (impedance on the side of the electrode 11) connected to the high-frequency power source 31 match.

[0037] The load-side impedance connected to the high-frequency power source 31 includes the electrode 11, a cable between the electrode 11 and the matching

circuit 41, discharge plasma, a vacuum chamber (not shown) housing the electrodes 11 and 12, and the like.

[0038] The power supply source 22 includes a high-frequency power source 32 (second high-frequency power

5 source) and a matching circuit 42 (second matching circuit). The high-frequency power source 32 outputs second high-frequency power that has the same period as the first high-frequency power and is lower than the first high-frequency power. The second high-frequency
10 power is typically RF power of 13.56 MH, and 50 W to 500 W can be output. Note that the high-frequency power is not limited to this example as long as it is in the same frequency band.

[0039] The matching circuit 42 is connected between

15 the high-frequency power source 32 and the electrode 12. The matching circuit 42 includes an input terminal 425, an output terminal 426, a variable capacitor 421 (first variable capacitor), a variable capacitor 422 (second variable capacitor), and an inductance 423. The
20 input terminal 425 is connected to the high-frequency power source 32. The output terminal 426 is connected to the electrode 12. The variable capacitor 421 is connected between the input terminal 425 and a ground potential. The variable capacitor 422 is connected
25 between the input terminal 425 and the output terminal 426 in series. The inductance 423 is connected to the

variable capacitor 422 between the input terminal 425 and the output terminal 426 in series. Each of the variable capacitor 421 and the variable capacitor 422 of the matching circuit 42 is driven by the controller 60 to perform automatic matching in which the output impedance of the high-frequency power source 32 and the load-side impedance (impedance on the side of the electrode 12) connected to the high-frequency power source 32 match.

10 [0040] The load-side impedance connected to the high-frequency power source 32 includes the electrode 12, a cable between the electrode 12 and the matching circuit 42, discharge plasma, a vacuum chamber (not shown) housing the electrodes 11 and 12, and the like.

15 [0041] Here, the capacitance of the variable capacitor 421 is represented by the capacitance value C1 (maximum 1000 pF), the capacitance (maximum 500 pF) of the variable capacitor 422 is represented by a capacitance value C2. Further, a sensor 424 that
20 detects a voltage value Vpp (Voltage peak to peak) of high-frequency power in the matching circuit 42 and a voltage value Vdc (Voltage direct current) at the output terminal 426 is mounted on the matching circuit 42. The voltage value Vpp means the difference between
25 the maximum voltage and the minimum voltage of the AC voltage. The voltage value Vdc means the voltage at the

midpoint between the maximum value and the minimum value of V_{pp} while the voltage of the voltage value V_{pp} applied to the electrode 12 floats at an entirely constant voltage. The voltage value V_{dc} is referred to also as an offset voltage or a bias voltage. In the case of RF discharge, the voltage value V_{dc} is generally a low potential with respect to a plasma potential (V_p). For example, if the plasma potential is a positive potential, the voltage value V_{dc} is a potential lower than this positive potential or is a negative potential.

[0042] Note that in the matching circuit 42, the variable capacitor 421 is mainly applied to match the output impedance of the high-frequency power source 32 and the load-side impedance connected to the high-frequency power source 32, and the variable capacitor 422 is mainly applied to match the phase of a voltage wave and the phase of a current wave.

Therefore, even when the output impedance of the high-frequency power source 32 and the load-side impedance connected to the high-frequency power source 32 match, the second high-frequency power is preferentially supplied from the input terminal 425 to the output terminal 426, part of the second high-frequency power

is discharged to the ground potential, or the second high-frequency power is does not reach the output terminal 426 and is discharged to the ground potential, depending on the capacitance value C1 of the variable capacitor 421. For example, the second high-frequency power is more preferentially supplied from the input terminal 425 to the output terminal 426 as the capacitance value C1 of the variable capacitor 421 becomes relatively larger.

[0043] In the power supply source 22, the high-frequency power source 32 includes a display unit, and the voltage value Vpp, the voltage value Vdc, the capacitance value C1, and the capacitance value C2 are displayed on this display unit. Further, these values are transmitted to the controller 60 and stored in a storage unit (not shown) within the controller 60. Note that such a sensor 424 may be mounted also on the matching circuit 41.

[0044] The phase adjuster 50 is capable of adjusting the phase of the first high-frequency power that is output from the high-frequency power source 31 and input to the matching circuit 41. The phase adjuster 50 is capable of adjusting the phase of the second high-frequency power that is output from the high-frequency power source 32 and input the matching circuit 42. The phase adjuster 50 is capable of providing a phase

difference θ between the phase of the first high-frequency power and the phase of the second high-frequency power.

[0045] The controller 60 controls the power supply source 21, the power supply source 22, and the phase adjuster 50. The controller 60 may be provided independently of the power supply source 21, the power supply source 22, and the phase adjuster 50, and part of the controller 60 may be incorporated in one of the power supply source 21, the power supply source 22, and the phase adjuster 50. The controller 60 includes a storage unit that stores data, a calculation unit that perform arithmetic processing on data, and the like.

[0046] (Deposition method)

[0047] In this embodiment, profile curves of the voltage value V_{pp} and the capacitance value C_1 that corresponds to the phase difference θ are acquired in advance. A dummy substrate may be used as the substrate 121 at the stage of acquiring this profile curve.

[0048] First, the high-frequency power source 31 is caused to output the first high-frequency power to form discharge plasma between the electrode 11 and the electrode 12. As the discharge gas, for example, argon is applied. The output impedance of the high-frequency power source 31 and the load-side impedance (impedance on the side of the electrode 11) connected to the high-

frequency power source 31 are caused to match by the matching circuit 41.

[0049] Next, the high-frequency power source 32 is caused to output the second high-frequency power and the phase adjuster 50 is caused to operate so that the phase difference θ between the phase of the first high-frequency power and the phase of second high-frequency power is provided. Here, each of the first high-frequency power and the second high-frequency power is not changed, and is set to a fixed value. Further, the second high-frequency power is lower than the first high-frequency power and is set to, for example, 1/10 to 1/2 of the first high-frequency power.

[0050] Next, while the discharge plasma is formed between the electrode 11 and the electrode 12, the voltage value V_{pp} of the second high-frequency power and the capacitance value $C1$ of the variable capacitor 421 that correspond to the phase difference θ in a state where the output impedance of the high-frequency power source 32 and the load-side impedance (impedance on the side of the electrode 12) connected to the high-frequency power source 32 are caused to match by the matching circuit 42 are detected. Then, by changing the phase difference θ , a profile curve (Part (a) of Fig. 2) of the voltage value V_{pp} corresponding to the phase difference θ and a profile curve (Part (b) of Fig. 2)

of the capacitance value C1 corresponding to the phase difference θ in a state where the output impedance of the high-frequency power source 32 and the load-side impedance connected to the high-frequency power source 32 match are acquired.

[0051] Here, the phase difference θ is formed by delaying the phase of the second high-frequency power with respect to the phase of the first high-frequency power by the phase adjuster 50, and is changed as appropriate in the range of 0 degrees to 360 degrees.

For example, in the case of changing the phase difference θ from 0 degrees, it is changed from 0 degrees by a predetermined interval, e.g., every 10 degrees to 10 degrees, 20 degrees, ..., 360 degrees.

Then, a sputtering film is formed on the substrate 121 by selecting the voltage value Vpp and the capacitance value C1 in combination in a predetermined range of the changed phase difference θ . Here, forming a sputtering film on the substrate 121 means embedding a sputtering film in a recessed pattern (lines and spaces, through holes, and the like) formed on the substrate 121 and forming the sputtering film on the surface of the substrate 121 other than the recessed pattern. The sputtering film deposited on the surface of the substrate 121 other than the recessed pattern may be removed as an excess portion as necessary by a method

such as a chemical mechanical polishing (CMP) after forming the sputtering film.

[0052] As described above, Part (a) of Fig. 2 is a graph describing an example of the profile curve of the voltage value V_{pp} . Part (b) of Fig. 2 is a graph describing an example of the profile curve of the capacitance value C_1 . In Part (a) of Fig. 2, the horizontal axis represents the phase difference θ and the vertical axis represents the voltage value V_{pp} . In Part (b) of Fig. 2, the horizontal axis represents the phase difference θ and the vertical axis represents the capacitance value C_1 . The first high-frequency power output from the high-frequency power source 31 is 4000 W, and the second high-frequency power output from the high-frequency power source 32 is 400 W. Further, the reduced pressure atmosphere is 0.1 to 4.0 Pa using argon gas. The distance between the sputtering target/substrate is 50 to 90 mm. Note that the higher V_{dc} shown in the graph, the stronger the bias potential to be applied to the electrode 12 toward the negative bias side.

[0053] For example, Part (a) of Fig. 2 shows the profile curves of the voltage value V_{pp} in two tests, i.e., a test A and a test B. The test A shows a profile curve in the case of using, as the high-frequency power source 32, a high-frequency power source that outputs

the second high-frequency power whose phase is synchronized with the phase of the first high-frequency power output from the high-frequency power source 31.

[0054] Meanwhile, the test B shows a profile curve

5 in the case of using, as the high-frequency power source 32, a high-frequency power source that outputs the second high-frequency power whose phase is advance by 50 degrees with respect to the phase of the first high-frequency power output from the high-frequency
10 power source 31. This has the same meaning that the length of the cable between the high-frequency power source 32 and the matching circuit 42 has increased by the amount corresponding to 50 degrees due to the maintenance of the deposition apparatus 1 or the like.

15 Note that in the test B, profile curves of the voltage value V_{pp} and the capacitance value C_1 are acquired by a deposition chamber different from that in the test A.

[0055] In the test A, the voltage value V_{pp} is high when the phase difference θ is around 0 degrees, and
20 the voltage value V_{pp} tends to gradually decrease as the phase difference θ increases. Then, the voltage value V_{pp} reaches its lowest value when the phase difference θ is 60 degrees, and then, the voltage value V_{pp} tends to gradually increase as the phase difference
25 θ increases. Meanwhile, also in the test B, the voltage value V_{pp} is high when the phase difference θ is around

60 degrees, and the voltage value V_{pp} tends to gradually decrease as the phase difference θ increases. Then, the voltage value V_{pp} reaches its lowest value when the phase difference θ is 110 degrees, and then, the voltage value V_{pp} tends to gradually increase as the phase difference θ increases.

[0056] In this way, in each of the profile curves of the voltage value V_{pp} in the test A and the test B, a downward convex curve is drawn.

[0057] Further, Part (b) of Fig. 2 shows profile curves of the capacitance value C_1 in the test A and the test B. In the test A, the capacitance value C_1 is low when the phase difference θ is around 0 degrees, and then, the capacitance value C_1 tends to gradually increase as the phase difference θ increases.

Meanwhile, also in the test B, the capacitance value C_1 is low when the phase difference θ is around 60 degrees, and then, the capacitance value C_1 tends to gradually increase as the phase difference θ increases.

[0058] In this embodiment, a sputtering film is formed on the substrate 121 by using these profile curves and setting the phase difference θ in a first range, and, the first range being a range of + 30 degrees to +50 degrees from a phase difference θ_1 of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the lowest.

[0059] For example, in the test A, the phase difference θ_1 where the voltage value V_{pp} is the lowest is 50 degrees, and the first range is a range of 80 degrees to 100 degrees. Further, in the test B, the phase difference θ_1 where the voltage value V_{pp} is the lowest is 100 degrees, and the first range is a range of 130 degrees to 150 degrees. In this embodiment, the voltage value V_{pp} and the capacitance value C_1 that belong to such a first range are applied to form a sputtering film on the substrate 121.

[0060] (Evaluation)

[0061] A difference between the sputtering film in the case where the voltage value V_{pp} and the capacitance value C_1 that belong to the first range are applied and the sputtering film in the case where the voltage value V_{pp} and the capacitance value C_1 that do not belong to the first range are applied will be described.

[0062] Part (a) of Fig. 3 to Part (e) of Fig. 3 are each a cross-sectional SEM image. Part (a) of Fig. 3 is a cross-sectional SEM image of a recessed pattern before a sputtering film is formed. Part (a) of Fig. 3 shows a recessed pattern that is formed of silicon oxide and has a depth of 240 nm and an aspect ratio of 1.0. The portion indicated by an arrow A is an end portion where the bottom portion of the recessed

pattern and a side wall intersect at approximately 90 degrees, and the portion indicated by an arrow B is a top end of the side wall. Further, Part (b) of Fig. 3 to Part (e) of Fig. 3 are each a cross-sectional SEM
5 image of the sputtering film after a sputtering film is formed in the recessed pattern. Part (b) of Fig. 3 to Part (e) of Fig. 3 each show a state after an alumina film as a sputtering film is embedded in this recessed pattern.

10 [0063] For example, as a sputtering film in the case of applying the phase difference θ that does not belong to the first range, a SEM image of a phase difference of 60 degrees (with reference to the minimum value of the profile curve of the voltage value V_{pp} , the phase
15 difference θ on the left side of the minimum value) in the test B is shown in Part (b) of Fig. 3 and a SEM image of a phase difference 100 degrees (the minimum value of the profile curve of the voltage value V_{pp}) in the test B is shown in Part (c) of Fig. 3. In these
20 alumina films, the wraparound to the end portion indicated by the arrow A was not excellent and a phenomenon in which the alumina film was recessed at an acute angle at the end portion appeared. Such a
25 tendency was observed also in the test A. Further, it was confirmed that an opening indicated by an arrow C was narrower and the film would close at the upper part

when the deposition was continued, forming a hole.

[0064] Meanwhile, as a sputtering film in the case of applying the phase difference θ that belongs to the first range, a SEM image of a phase difference of 100 degrees in the test A is shown in Part (d) of Fig. 3 and a SEM image of a phase difference of 140 degrees in the test B is shown in part (e) of Fig. 3. In these alumina films, it was found that the alumina film was not recessed at an acute angle at the end portion and the alumina film with excellent step coverage was formed at the end portion. Further, even if the aspect ratio of the recessed pattern is 0.2 to 1.0, it was found that the wraparound to the end portion indicated by the arrow A was not excellent in the case of applying the phase difference θ that does not belong to the first range while an alumina film with excellent step coverage was formed by applying the phase difference θ that belongs to the first range.

[0065] In other words, since the profile curve of the voltage value V_{pp} is convex downward, the same voltage value as the voltage value V_{pp} that belongs to the first range is present outside the first range. Instead of selecting the voltage value V_{pp} outside the first range, the voltage value V_{pp} that belongs to the first range, of the same voltage values V_{pp} , and the capacitance value C_1 that is a relatively high

capacitance value are selected in combination, thereby forming an alumina film with excellent step coverage. Here, in the first range, the capacitance value C1 is set larger than the capacitance value C2.

5 [0066] Next, the results of further increasing the phase difference θ from 100 degrees will be described using the test A.

[0067] Fig. 4 shows the profile curves of the voltage value Vpp and the capacitance value C1 in the
10 test A. In Fig. 4, the horizontal axis represents the phase difference θ , and the left vertical axis indicates the voltage value Vdc in addition to the voltage value Vpp and the voltage value Vpp. Further, the right vertical axis indicates the capacitance value
15 C1. Further, Fig. 4 also shows the profile curve in the case where the phase difference θ is 0 degrees to 110 degrees described above.

[0068] When the phase difference θ exceeds 100 degrees and reaches 110 degrees to 240 degrees, the
20 capacitance value C1 shook off the maximum capacitance value of 1000 pF and a phenomenon in which the output impedance of the high-frequency power source 32 and the load-side impedance connected to the high-frequency power source 32 could not match occurred. In this non-
25 matching region (110 to 240 degrees), both the voltage value Vpp and the voltage value Vdc became unstable.

[0069] Meanwhile, when the phase difference θ exceeded 240 degrees and reached 250 degrees, the output impedance of the high-frequency power source 32 and the load-side impedance connected to the high-frequency power source 32 matched again. After that, the voltage value V_{pp} gradually increased as the phase difference θ increased, the voltage value V_{pp} reached its maximum value when the phase difference θ was 300 degrees, and then, the voltage value V_{pp} gradually decreased as the phase difference θ increased. Further, it was found that the capacitance value C_1 is high when the phase difference θ is around 250 degrees, and then, the capacitance value C_1 gradually decreases as the phase difference θ increases. It was found that the voltage value V_{dc} gradually decreases in the range of 240 degrees to 290 degrees where the voltage value V_{pp} increases.

[0070] As described above, it was found that the profile curve of the voltage value V_{pp} draws an upward convex curve when the phase difference θ is 250 degrees to 360 degrees.

[0071] As described above, it was confirmed that the voltage value V_{pp} is convex downward and the capacitance value C_1 rises to the right in a region of the phase difference θ (referred to as an in-phase region) in which the phase of the waveform of the high-

frequency voltage supplied to the electrode 11 and the phase of the waveform of the high-frequency voltage supplied to the electrode 12 match, and the voltage value V_{pp} is convex upward and the capacitance value $C1$ falls to the right in a region of the phase difference θ (referred to as an anti-phase region) in which the phase of the waveform of the high-frequency voltage supplied to the electrode 11 and the phase of the waveform of the high-frequency voltage supplied to the electrode 12 are deviated from each other.

[0072] In this embodiment, in a region where the phase difference θ is 250 degrees to 360 degrees, the phase difference θ is set in a second range and forms a sputtering film on the substrate 121, the second range being a range from +10 degrees to -10 degrees from a phase difference θ_2 of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the largest. For example, the phase difference θ_2 where the voltage value V_{pp} is the largest is 300 degrees, and the second range is a range from 290 degrees to 310 degrees. Here, in the second range, the capacitance value $C1$ is set larger than the capacitance value $C2$.

[0073] A difference between the sputtering film in the case of applying the voltage value V_{pp} and the capacitance value $C1$ that belong to the second range and the sputtering film in the case of applying the

voltage value V_{pp} and the capacitance value C_1 that do not belong to the second range will be described.

[0074] Parts (a) and (b) of Fig. 5 are each a cross-sectional SEM image of a sputtering film after the sputtering film is formed in the recessed pattern shown in Part (a) of Fig. 3.

[0075] For example, as an example of the sputtering film that does not belong to the first range and the second range, an example in which deposition is started on the empty recessed pattern under the condition of a phase difference of 260 degrees will be shown. Part (a) of Fig. 5 shows a SEM image of a phase difference of 260 degrees. In this case, it was confirmed that the voltage value V_{dc} becomes larger than 50 (V), the top end of recessed pattern indicated by an arrow B is etched, and the alumina film has a facet shape at this top end.

[0076] Meanwhile, as an example of the sputtering film that belongs to the second range, a SEM image of a phase difference of 300 degrees is shown in Part (b) of Fig. 5. In this alumina film, it was found that the wraparound to the end portion is improved, the alumina film is not recessed at an acute angle at the end portion, and an alumina film with excellent step coverage is formed at the end portion. It was confirmed that when the phase difference θ exceeds 310 degrees,

the alumina film is recessed at an acute angle at the end portion.

[0077] As described above, it was found that even if both the first high-frequency power output from the high-frequency power source 31 and the second high-frequency power output from the high-frequency power source 32 are fixed power, the embedding characteristics of the sputtering film with respect to the recessed pattern change by manipulating the phase difference θ . In particular, it was found that a sputtering film exhibiting excellent step coverage is formed by setting the phase difference θ in the first range of +30 degrees to +50 degrees from the phase difference θ_1 where the profile curve of the voltage value V_{pp} has the smallest value. Alternatively, it was found that a sputtering film exhibiting excellent step coverage is formed by setting the phase difference θ in the second range of +10 degrees to -10 degrees from the phase difference θ_2 where the profile curve of the voltage value V_{pp} has the largest value.

[0078] Note that when the waveform of the high-frequency power at a position 418 (Fig. 1) between the electrode 11 and the matching circuit 41 and directly above the electrode 11 and a position 428 between the electrode 12 and the matching circuit 42 and directly below the electrode 12 was observed with an

oscilloscope, it was confirmed that the phase of the waveform of the high-frequency voltage supplied to the electrode 11 and the phase of the waveform of the high-frequency voltage supplied to the electrode 12 match in the range from 0 degrees to 110 degrees, and the phase of the waveform of the high-frequency voltage supplied to the electrode 11 and the phase of the waveform of the high-frequency voltage supplied to the electrode 12 are displaced from each other in the range of 250 degrees to 360 degrees.

[0079] The controller 60 stores data of profile curves of the voltage value V_{pp} and the capacitance value $C1$ obtained in advance. The controller 60 selects the voltage value V_{pp} and the capacitance value $C1$ in combination in a predetermined range of the phase difference θ and form a sputtering film on the substrate 121.

[0080] For example, the controller 60 controls the phase adjuster 50 to set the phase difference θ in the first range (the voltage value V_{pp} : 80 to 130 (V)), the capacitance value $C1$: 600 pF or more) or the second range (the voltage value V_{pp} : 260 to 280 (V)), the capacitance value $C1$: 600 to 900 (pF), V_{dc} : 50 (V) or less) and form a sputtering film on the substrate 121 in a state where the output impedance of the high-frequency power source 32 and the load-side impedance

match, the first range being a range of +30 degrees to +50 degrees from the phase difference θ_1 of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the lowest, the second range being a range of +10 degrees to -10 degrees from the phase difference θ_2 of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the largest.

[0081] As a result, a sputtering film exhibiting excellent step coverage with respect to the recessed pattern is formed.

[0082] (Modified example 1)

[0083] In the first range or the second range, a sputtering film may be formed on the substrate 121 by changing the phase difference θ in a stepwise manner.

When changing the phase difference θ in a stepwise manner, the first high-frequency power output from the high-frequency power source 31 is maintained at the same level. For example, the voltage value V_{dc} tends to increase as the capacitance value C_1 increases. Then, as the voltage value V_{dc} increases, the recessed pattern underlying the sputtering film is more likely to be damaged by sputtering particles.

[0084] Therefore, a sputtering film may be formed in a recessed pattern by setting the phase difference θ such that the voltage value V_{dc} is low immediately after sputter-deposition, and the phase difference θ

may be changed, e.g., the phase difference θ may be set such that the deposition rate increases to perform the sputter-deposition after a sputtering film having a predetermined thickness is embedded in the recessed pattern.

[0085] (Modified example 2)

Fig. 6 shows profile curves of the voltage value V_{pp} and the capacitance value C_1 according to a modified example 2. In the modified example 2, a third range is used as a range of the phase difference θ in addition to the first and second ranges.

[0086] As in the example of Part (b) of Fig. 5, the top end of the recessed pattern is etched in the case of starting deposition on the empty recessed pattern under the condition of a phase difference of 260 degrees. However, in the case of adopting a process of changing the phase difference θ in a stepwise manner, excellent step coverage can be achieved by adopting deposition in the third range including a phase difference of 260 degrees as the phase difference θ in the latter of the stepwise Steps.

[0087] For example, a sputtering film is formed on the substrate 121 in the first range or the second range, and then, a sputtering film is formed on the substrate 121 in the third range. Here, the third range is a range in which the phase difference θ is smaller

than the second range and larger than the first range. For example, the third range is a range of -50 degrees to -30 degrees from the phase difference θ_2 . The capacitance value C1 in the third range is 875 pF to 1000 pF. Note that when switching from the deposition in the first range or the second range to the deposition in the third range, the first high-frequency power output from the high-frequency power source 31 is maintained at the same level.

10 [0088] Parts (a) and (b) of Fig. 7 are each a schematic cross section showing a deposition method according to the modified example 2. Further, Part (c) of Fig. 7 is a cross-sectional SEM image of a sputtering film after the sputtering film is formed in
15 a recessed pattern. The aspect ratio of a recessed pattern 122 shown in Part (C) of Fig. 7 is the same as the aspect ratio of the recessed pattern shown in Part (a) of Fig. 3.

[0089] For example, as shown in Part (a) of Fig. 7,
20 a sputtering film 125 such as an alumina film is formed in the recessed pattern 122 formed of silicon oxide as a first Step under the condition that the phase difference θ is in the first range or the second range. As a result, the sputtering film 125 is formed in the
25 recessed pattern 122. In the first Step, the sputtering film 125 is embedded while leaving an unfilled portion

in the recessed pattern 122 instead of filling the entire inside of the recessed pattern 122 with the sputtering film 125. For example, regarding the target of film thickness in the first Step, the film thickness of the sputtering film 125 deposited on the portion (field portion) where the recessed pattern 122 is not formed is set to 40% to 60% of the opening width of the recessed pattern 122. Here, in the case where the recessed pattern 122 is lines and spaces, the opening width is an opening width of the recessed pattern 122 at the top end in the case of cutting the recessed pattern 122 in the direction in which the lines and spaces are arranged side by side. In the case where the recessed pattern 122 is a through hole, the opening width means the maximum diameter of the through hole at the top end. Further, in the first Step, a top end 122c of the recessed pattern 122 is covered (protected) with the sputtering film 125.

[0090] Here, in the recessed pattern 122, the sputtering film 125 is deposited from the bottom portion of the recessed pattern 122 and the sputtering film 125 is deposited also from the side wall of the recessed pattern 122. Therefore, in the sputtering film 125 formed in the recessed pattern 122, a recessed portion 125b that is recessed in the vicinity of the center of the sputtering film 125 is formed.

[0091] In the case of adopting a process in which the phase difference θ is not changed in a stepwise manner, in other words, in the case of continuing the deposition while the phase difference θ is in the first range or the second range, it is necessary to deposit the sputtering film 125 having a thickness equal to or larger than the depth of the recessed pattern 122 on the substrate 121 in order to fill the recessed pattern 122 with the sputtering film 125 until the recessed portion 125b disappears. However, as the thickness of the sputtering film 125 to be deposited on the substrate 121 increases, the burden on the CMP processing in the post-process increases. Further, the recessed portion 125b is more likely to be formed as the aspect ratio of the recessed pattern increases, and a phenomenon in which the recessed portion 125b remains as a void in the sputtering film 125 can occur when continuing the deposition in the first range or the second range.

[0092] In this regard, in the modified example 2, the deposition in the first range or the second range is stopped in the state of Part (a) of Fig. 7 and sputter-deposition is performed with the phase difference θ in the third range as the next Step. For example, after forming the sputtering film 125, a sputtering film 126 is formed under the condition that

the phase difference θ is in the third range on the sputtering film 125. This state is shown in Part (b) of Fig. 7.

[0093] In the third range, the second high-frequency power is more preferentially supplied to the electrode 12 via the output terminal 426 as the capacitance value C1 increases, and the voltage value Vdc tends to increase more than in the first range and the second range. Therefore, simultaneously with the deposition of sputtering particles on the substrate 121, the bias potential applied to the substrate 121 attracts ion (e.g., positive ion) particles to the substrate 121, and physical etching of the sputtering film by the ion particles also occurs. Here, when the deposition of sputtering particles on the substrate 121 works better than the physical etching of the sputtering film by the ion particles, the sputtering film is formed on the substrate 121 while the sputtering film is physically etched.

[0094] As a result, in the sputter-deposition in the third range, the width of the recessed portion 125b is further widened by the etching effect. Further, in the sputtering film 125 covering the top end 122c of the recessed pattern 122, so-called film thinning (phenomenon in which the film thickness is reduced) occurs due the etching effect. Since the width of the

recessed portion 125b is further widened, it is easier to fill the recessed portion 125b with the sputtering film. Further, since the top end 122c of the recessed pattern 122 is protected by the sputtering film 125, the top end 122c maintains its original shape without being etched.

[0095] Therefore, even if the recessed pattern 122 has a high aspect ratio, after the sputtering film 126 is formed, a sputtering film 127 having no void inside is formed in the recessed pattern 122 by the sputtering film 125 and the sputtering film 126 covering the sputtering film 125. The fact that the recessed pattern 122 is favorably filled with the sputtering film 127 having no void inside is confirmed also by the cross-sectional SEM image shown in Part (c) of Fig. 7.

[0096] In the modified example 2, the deposition with the phase difference θ in the third range may be performed after the deposition with the phase difference θ in the first range, or the deposition with the phase difference θ in the third range may be performed after the deposition with the phase difference θ in the second range.

[0097] Here, in order to switch from the phase difference θ in the first range to the phase difference θ in the third range, the phase difference θ only needs to be increased from the first range to the third

range. However, in the case of shifting the phase difference θ from the first range to the third range, it is necessary to cause the phase difference θ to pass through the non-matching region before reaching the third range. For this reason, in this method, it is necessary to adopt deposition processing of temporarily stopping the plasma discharge after the deposition in the first range is performed and switching from the phase difference θ in the first range to the phase difference θ in the third range.

[0098] Meanwhile, in order to switch from the phase difference θ in the second range to the phase difference θ in the third range, the phase difference θ only needs to be decreased from the second range to the third range. In this case, even if the phase difference θ is shifted from the second range to the third range, the phase difference θ does not need to pass through a non-matching region because there is no non-matching region between the second range and the third range. For this reason, it is possible to switch, after the deposition in the second range is performed, to the third range by changing the phase difference θ in a continuous manner without stopping the plasma discharge.

[0099] Although embodiments of the present invention have been described above, the present invention is not

limited only to the above-mentioned embodiments and it goes without saying that various modifications can be made. The respective embodiments are not limited to the independent form and can be combined as much as

5 technologically possible.

Reference Signs List

	[0100]	1	deposition apparatus
		11	electrode
		111	sputtering target
10		112	back plate
		12	electrode
		121	substrate
		122c	top end
		122	recessed pattern
15		125, 126, 127	sputtering film
		125b	recessed portion
		21, 22	power supply source
		31, 32	high-frequency power source
		41, 42	matching circuit
20		411, 412, 421, 422	variable capacitor
		413, 423	inductance
		415, 425	input terminal
		416, 426	output terminal
		424	sensor
25		50	phase adjuster
		60	controller

Claims

[1] A deposition method, comprising:

by using a deposition apparatus including

5 a first electrode that includes a sputtering target,

a second electrode that faces the first electrode and is capable of supporting a substrate,

a first power supply source that includes a first high-frequency power source and a first matching circuit, the first high-frequency power source outputting first high-frequency power, the first matching circuit being connected between the first high-frequency power source and the first electrode,

15 a second power supply source that includes a second high-frequency power source and a second matching circuit, the second high-frequency power source outputting second high-frequency power that has the same period as the first high-frequency power and is lower than the first high-frequency power, the second matching circuit being connected between the second high-frequency power source and the second electrode and the second matching circuit including an input terminal, an output terminal, a first variable capacitor, and a second variable capacitor, the input terminal being connected to the second high-frequency

power source, the output terminal being connected to the second electrode, the first variable capacitor being connected between the input terminal and a ground potential, the second variable capacitor being
5 connected between the input terminal and the output terminal in series, and

a phase adjuster that adjusts a phase of the first high-frequency power that is output from the first high-frequency power source and input to the
10 first matching circuit and a phase of the second high-frequency power that is output from the second high-frequency power source and input to the second matching circuit,

causing the first high-frequency power source to
15 output the first high-frequency power to form discharge plasma between the first electrode and the second electrode;

causing the second high-frequency power source to output the second high-frequency power and causing the
20 phase adjuster to operate to provide a phase difference θ between the phase of the first high-frequency power and the phase of the second high-frequency power;

detecting a voltage value V_{pp} of the second high-frequency power and a capacitance value C_1 of the first
25 variable capacitor that correspond to the phase difference θ in a state where output impedance of the

second high-frequency power source and load-side impedance connected to the second high-frequency power source match; and

forming a sputtering film on the substrate by selecting the voltage value V_{pp} and the capacitance value $C1$ in combination in a predetermined range of the phase difference θ .

[2] The deposition method according to claim 1, further comprising:

forming the phase difference θ by delaying the phase of the second high-frequency power with respect to the phase of the first high-frequency power;

obtaining a profile curve of the voltage value V_{pp} and a profile curve of the capacitance value $C1$ that correspond to the phase difference θ by changing the phase difference θ ;

setting the phase difference θ in a first range of the profile curve of the voltage value V_{pp} or a second range and the first range being a range of +30 degrees to +50 degrees from a phase difference $\theta1$ of the profile curve of the voltage value V_{pp} where the voltage value V_{pp} is the lowest, the second range being a range of +10 degrees to -10 degrees from a phase difference $\theta2$ where the voltage value V_{pp} is the largest and forming the sputtering film on the substrate in a state where the output impedance and the

load-side impedance match.

[3] The deposition method according to claim 2,
further comprising

forming the sputtering film on the substrate by
5 changing the phase difference θ in a stepwise manner in
the first range or the second range.

[4] The deposition method according to claim 2 or 3,
further comprising

forming the sputtering film on the substrate in a
10 third range in which the phase difference θ is smaller
than the second range and larger than the first range
after forming the sputtering film on the substrate in
the first range or the second range.

[5] The deposition method according to claim 4,
15 wherein

the third range is a range of -50 degrees to -30
degrees from the phase difference θ_2 .

[6] A deposition apparatus, comprising:

a first electrode that includes a sputtering
20 target;

a second electrode that faces the first electrode
and is capable of supporting a substrate;

a first power supply source that includes a first
high-frequency power source and a first matching
25 circuit, the first high-frequency power source
outputting first high-frequency power, the first

matching circuit being connected between the first high-frequency power source and the first electrode;

a second power supply source that includes a second high-frequency power source and a second matching circuit, the second high-frequency power source outputting second high-frequency power that has the same period as the first high-frequency power and is lower than the first high-frequency power, the second matching circuit being connected between the second high-frequency power source and the second electrode and the second matching circuit including an input terminal, an output terminal, a first variable capacitor, and a second variable capacitor, the input terminal being connected to the second high-frequency power source, the output terminal being connected to the second electrode, the first variable capacitor being connected between the input terminal and a ground potential, the second variable capacitor being connected between the input terminal and the output terminal in series;

a phase adjuster that adjusts a phase of the first high-frequency power that is output from the first high-frequency power source and input to the first matching circuit and a phase of the second high-frequency power that is output from the second high-frequency power source and input to the second matching

circuit; and

a controller that controls the first power supply source, the second power supply source, and the phase adjuster,

5 the controller storing data obtained by

causing the first high-frequency power source to output the first high-frequency power to form discharge plasma between the first electrode and the second electrode,

10 causing the second high-frequency power source to output the second high-frequency power and causing the phase adjuster to operate to provide a phase difference θ between the phase of the first high-frequency power and the phase of the second high-frequency power, and

15 detecting a voltage value V_{pp} of the second high-frequency power and a capacitance value C_1 of the first variable capacitor that correspond to the phase difference θ in a state where output impedance of the second high-frequency power source and load-side impedance connected to the second high-frequency power source match,

20 the controller selecting the voltage value V_{pp} and the capacitance value C_1 in combination in a predetermined range of the phase difference θ to form a sputtering film on the substrate.

[7] The deposition apparatus according to claim 6,
wherein

the controller stores a profile curve of the
voltage value V_{pp} and a profile curve of the
5 capacitance value C_1 that correspond to the phase
difference θ obtained by forming the phase difference θ
by delaying the phase of the second high-frequency
power with respect to the phase of the first high-
frequency power and changing the phase difference θ ,
10 and

the controller sets the phase difference θ in a
first range or a second range, the first range being a
range of +30 degrees to +50 degrees from a phase
difference θ_1 of the profile curve of the voltage value
15 V_{pp} where the voltage value V_{pp} is the lowest, the
second range being a range of +10 degrees to -10
degrees from a phase difference θ_2 where the voltage
value V_{pp} is the largest to form the sputtering film on
the substrate in a state where the output impedance and
20 the load-side impedance match.

[8] The deposition apparatus according to claim 7,
further comprising

forming the sputtering film on the substrate by
changing the phase difference θ in a stepwise manner in
25 the first range or the second range.

[9] The deposition apparatus according to claim 7 or

8, further comprising

forming the sputtering film on the substrate in a third range in which the phase difference θ is smaller than the second range and larger than the first range

5 after forming the sputtering film on the substrate in the first range or the second range.

[10] The deposition apparatus according to claim 9, wherein

10 the third range is a range of -50 degrees to -30 degrees from the phase difference θ_2 .