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**METHOD AND CIRCUIT FOR DRIVING POWER TRANSISTORS
IN A HALF BRIDGE CONFIGURATION ALLOWING FOR
EXCESSIVE NEGATIVE SWING OF THE OUTPUT NODE AND
INTEGRATED CIRCUIT INCORPORATING THE CIRCUIT**

5 **BACKGROUND OF THE INVENTION**

The present invention is directed to a method and circuit for driving power transistors in a half bridge configuration allowing for excessive negative swing of the output node. It is also directed to an
10 integrated circuit incorporating the circuit, e.g., a circuit integrated on a single silicon chip.

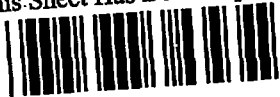
In driver circuits for power transistors, for example, power MOSFETs driving power equipment, the power transistors often switch a large current. The large
15 switching current, combined with forward recovery characteristics of diodes and stray inductance in the circuit, generates a negative spike at the output node of the half bridge. These spike signals can be destructive to the driver circuits and also create noise.

20 **SUMMARY OF THE INVENTION**

It is accordingly, an object of the present invention to provide a method and circuit for driving power transistors in a half bridge configuration allowing for excessive negative swing of the output node.

25 It is furthermore an object of the present invention to provide such a circuit which can be integrated on a single chip.

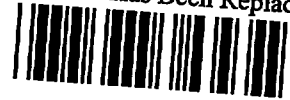
The above and other objects of the invention are achieved by a method for driving power transistors in



5 a half bridge configuration allowing for excessive
negative swing of an output node between the transistors
in the half bridge configuration comprising arranging
first and second power transistors in series in a half
bridge configuration with an output node between the
transistors; connecting the series transistors between a
first voltage source and a common potential; providing a
second voltage reference source; providing a terminal
connected to a common point coupled to anodes of
10 intrinsic diodes of driver circuits for the power
transistors; and connecting the second voltage source
between the common potential and the terminal so as to
shift the level of the common point such that the
intrinsic diodes will not forward bias due to negative
15 transients at the output node.

The above and other objects of the invention
are also achieved by a circuit for driving power
transistors arranged in series in a half bridge
configuration allowing for excessive negative swing of an
20 output node between the transistors in the half bridge
configuration, the series transistors being adapted to be
connected between a first voltage source and a common
potential, the circuit comprising: driver circuits for
each of the power transistors, a terminal connected to a
25 common point coupled to anodes of intrinsic diodes of the
driver circuits for the power transistors; and the
terminal being adapted to be connected to a second
voltage source provided between the common potential and
the terminal so as to shift the level of the common point
30 such that the intrinsic diodes will not forward bias due
to negative transients at the output node.

The above and other objects of the invention
are also claimed by a method of integrating on a single



integrated circuit chip a circuit for driving power transistors in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration comprising:

5 arranging first and second power transistors in series in a half bridge configuration with an output node between the transistors;

 connecting the series transistors between a first voltage source and a common potential;

10 providing a second voltage reference source;

 providing a terminal coupled to a common point coupled to anodes of intrinsic diodes of driver circuits for the power transistors; and

15 connecting the second voltage source between said common potential and said terminal so as to shift the level of said common point such that said intrinsic diodes will not forward bias due to negative transients at the output node.

20 The above and other objects of the invention are also achieved by a circuit integrated on a single integrated circuit chip for driving power transistors arranged in series in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration, the series transistors being adapted to be connected between a first voltage source and a common potential, the circuit comprising:

30 driver circuits for each of the power transistors;

 a terminal connected to a common point coupled to anodes of intrinsic diodes of the driver circuits for the power transistors; and



the terminal being adapted to be connected to a second voltage source provided between said common potential and said terminal so as to shift the level of said common point such that said intrinsic diodes will not forward bias due to negative transients at the output node.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1(a) shows power transistors, illustratively power mosfets, arranged in a half bridge configuration;

Figure 1(b) shows a typical output pulse at the common output node of the power transistors, including a negative spike, as encountered in the prior art circuits;

Figure 2 shows a typical half bridge configuration interfaced with a driver interface IC which provides the driver signals to drive the power transistors;

Figures 3(a) and 3(b) show two arrangements according to the invention which allow power transistors and the driver circuits to operate with negative output node spikes without damage;

Figure 4 shows an output pulse of the circuit of Figures 3(a) or 3(b), illustrating how the circuit of the invention prevents driver circuit intrinsic diode forward biasing, thereby allowing operation of the circuit without damage from negative output node spikes;

Figure 5 shows a conventional integrated circuit driver which can be modified in accordance with



the invention to incorporate the circuit of the invention;

Figure 6(a) shows how a portion of the circuit of Fig. 3(a) can be implemented in an integrated circuit; and

Figure 6(b) shows how a portion of the circuit of Fig. 3(b) can be implemented in an integrated circuit.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

With reference now to the drawings, Figure 1(a) shows power transistors, in particular, power mosfets, in a typical half bridge circuit. In the arrangement shown, two power transistors are configured in series in a totem pole arrangement. The high side transistor 10 has its drain connected to a voltage supply VL and the low side transistor 20 has its source connected to a common reference point. The output may be taken at the common node between the two transistors 10 and 20 and is coupled to the VS pin from the driver circuit coupled to the power transistors, and described in more detail with reference to Figure 2.

In a half bridge circuit, the output node typically swings below ground (COM) as shown in Figure 1(b). This negative spike is typically higher for high power circuits or highly inductive circuits and can reach tens of volts.

With reference to Figure 2, which shows the half bridge configuration being driven by an interface chip 25, for example, the IR 2110 available from International Rectifier Corp., in such a junction isolated integrated circuit 25, VS cannot fall below reference COM by more than the supply potential VB because the supply potential VB will also fall below COM



and the inherent diode 22 between VB and COM will forward bias. This inherent or parasitic diode 22 is typically present in driver circuits of the type shown in Figure 2. In some situations, the forward biasing of this diode can create significant currents which can damage the diode or other parts of the circuit. Therefore, it is preferable to prevent the parasitic diode 22 from forward biasing if possible, so as to prevent damage to the circuit. In addition to the parasitic diode 22, a parasitic diode 28 between VDD and COM and another parasitic diode 30 between VCC and COM are also present.

Figure 5 shows a conventional interface chip 25 in greater detail. In particular, Figure 5 shows the details of a conventional IR-2110 integrated circuit driver device. This device can be modified in accordance with the invention to incorporate the circuit of the invention which is shown in detail in Figures 3(a) and 3(b).

Figure 5 is a functional block diagram of the circuit contained within the integrated circuit 25 in Figure 2. Logic input pins 10, 11 and 12 are connected through Schmitt triggers 32X, 32Y and 32Z to the RS latches 32T and 32U and to logic circuits 32V and 32W. The outputs of logic circuits 32V and 32W are coupled, respectively, to level shift circuits 33A and 33B. As will be seen, the outputs of the level shift circuits 33A and 33B control the high side control output and low side control output at pins 7 and 1, respectively.

The output from level shift circuit 33B in the low voltage channel is applied through a delay circuit 26A and one input of gate circuit 26B. The output of gate 26B is connected to the gate electrodes of driver output MOSFET transistors 26C and 26D. As will be later



described, these transistors will produce a gate voltage at pin 1 (L OUT) when required by the logic input to pins 11 and 12.

5 The circuit of Figure 5 also contains an under-voltage detection circuit 27 which disables the output from gate 26B when an under voltage is detected at pin 3 (VCC) to prevent turn-on of the power MOSFET or IGBT operated from pin 1.

10 The level shift circuit 33A for the high voltage channel of the circuit has one input connected to the pulse generator 24A. Under-voltage detection circuit 27 is also connected to pulse generator 24A and will turn off the high voltage output channel responsive to the detection of an under-voltage condition at pin 3 (VCC).

15 Pulse generator 24A has two outputs, a set(s) output connected to the gate of MOSFET 24B and a reset (R) output connected to the gate of MOSFET 24C.

20 The sources of MOSFETs 24B and 24C are connected to a common connection rail and their drains are connected to resistors 24D and 24E, respectively.

25 During normal operation, the application of pulses to MOSFETs 24B and 24C from the pulse generator 24A will produce output voltage pulses Vset and Vrst at the nodes between MOSFETs 24B and 24C and their respective resistors 24D and 24E.

30 The pulses Vset and Vrst are then applied to a pulse filter 24F. The output channels of filter 24F are connected to the R and S inputs of latch 24G. A second under-voltage detection circuit 24H is provided as an input to the latch 24G to ensure that no signal is applied at pin 7 if an under-voltage is detected at pin 6.



5 The output of the RS latch 24G is then used to turn driver MOSFETs 24I and 24J on and off. Thus, if a high signal is applied to input R of the RS latch 24G, the output at pin 7 is turned off. If a high signal is applied to the S input of latch 24G, the output at pin 7 will turn on.

10 Figure 5 shows the intrinsic diode 22 present between VB and COM, shown also in Figure 2. In addition, intrinsic diodes are also found between VDD and COM and between VCC and COM. See diodes 28 and 30 in Figure 5.

15 Figures 3(a) and 3(b) show two examples of how transistors in a half bridge configuration can be operated in a safe manner and allowing for excessive negative swing of the output node without damage to the driver circuits. These figures show how the circuit of Figure 5 can be modified in accordance with the invention. The allowable negative spike at the output node between transistors 10 and 20 can be increased using either one of the two circuits shown in Figure 3(a) or Figure 3(b).

20 According to the invention, the common anodes of intrinsic diodes 22, 28 and 30, which are always present as shown in the drawing figures, are floated with respect to the reference COM of the low side driver circuit 26 by a voltage V_{sub} . As shown, the floating voltage supply V_{sub} is polarized such that the anodes of the intrinsic diodes 22, 28 and 30 are at a negative potential- V_{sub} with respect to COM. In this way, VS can fall below COM by up to the V_{sub} potential. This configuration allows for the custom setting of the allowable negative spike at the output node VS for a given application.



5 The two circuits of Figures 3(a) and 3(b)
differ only by the fact that the input logic circuits 32a
and 32b are referenced differently. In Figures 3(a) and
3(b), the details of the interface circuit 25, shown in
10 Figure 5, are not shown. In Figures 3(a) and 3(b),
suitable level shifting circuits are necessary to supply
the driver signals from input circuits 32a and 32b to the
driver circuits 24 and 26. Such level shifting circuits
can be of the type disclosed in copending application
15 Serial No. IR-1122, filed concurrently herewith and the
disclosure of which is incorporated by reference herein.

In Figure 3(a), the input circuit 32a floats
above the voltage $-V_{sub}$. Accordingly, in the circuit of
Fig. 3(a), a level shifting circuit 40 will be necessary
15 to shift the level of the output of input circuit 32a
first to the $-V_{sub}$ reference level. The output of the
level shifting circuit 40 is coupled to a buffer 41, and
the output of the buffer 41 is coupled to level shifting
circuits 44 and 42. The level shifting circuit 42 is
20 necessary to shift the level of the signals from the
 $-V_{sub}$ level to the level COM to drive the low side driver
circuit 26, and the level shifting circuit 44 is
necessary to shift the level of the signals from the
 $-V_{sub}$ level to the reference level VB to drive the high
25 side driver circuit 24.

In Figure 3(b), since the input circuit 32b is
already referenced to the $-V_{sub}$ level, only two level
shifting circuits are necessary, one (46) to shift the
level of the output of the input circuit 32b to the COM
30 reference level for driving the low side driver circuit
26 and another (48) to shift the reference level to the
reference level VB of the high side driver circuit 24.



Because the anode of the intrinsic diode 22 is now at the level $-V_{sub}$ with respect to the reference level COM in the circuits of Figures 3(a) and 3(b), this diode will not forward bias if V_S falls below COM by up to the V_{sub} potential. This is shown graphically in Fig. 4, which shows the negative spike at the output node V_S above the $-V_{sub}$ potential, thereby preventing intrinsic diode forward conduction. Accordingly, the high current conditions caused in the prior art circuit of Figure 2 due to the forward biasing of the intrinsic diodes cannot occur.

Figures 6(a) and 6(b) show how portions of the circuits of respective Figures 3(a) and 3(b) can be implemented in an integrated circuit. Figure 6(a) shows a portion of the circuit of Figure 3(a) and Figure 6(b) shows a portion of the circuit Figure 3(b). Two circuit structures are essentially identical. The only difference is that the various terminals are connected to points of different potential. These are shown in Figures 6(a) and 6(b). A description of Figure 6(a) will now be given. For brevity, a detailed description of Figure 6(b) will not be given. The reader can observe the differences in potentials by the comparing the two Figures.

When implementing the circuit of Figure 3(a) in a common chip, the high and low voltage circuits are laterally isolated from one another. Figure 6(a) shows a portion of such a chip in cross-section. Thus, in Figure 6(a), a silicon chip 120 consists of a P^- substrate 121 which has an epitaxially layer 122 of N^- silicon grown thereon. The N^- region 122 is separated into high voltage and low voltage regions by P^+ sinkers 130, 131 and 132. Thus, sinkers 130 and 131 define a high voltage



device region 140 in epitaxial layer 122, separated from low voltage region 141. Regions 140 and 141 can have any desired pathology. Moreover, any desired isolation technique can be used between regions 140 and 141.

5 Typically, MOSFET driver circuits, such as the circuit 24 in Figure 3(a), comprise P channel and N channel MOSFET transistors. This is described in co-
pending patent application Serial No. 08/274,012 (IR-
1131), assigned to the assignee of this application. The
10 disclosure of that application is incorporated by reference herein. The high voltage circuitry MOSFETs of the driver circuit 24 of the Figure 3(a) are shown as
formed within high voltage region 140. The P⁺ contact
regions 162 and 163, which are diffused in layers 122,
15 represent any of the source and drains of the P channel MOSFETs of the driver device 24. The P region 164 is
diffused in layer 122 to form the P-type well region.
The N⁺ contact regions 160 and 161, which are diffused in
the P-type region 64, represent any of the sources and
20 drains of the N channel MOSFETs of the driver device 24 of Figure 3(a).

 Typically, driver devices like circuit 24 of Figure 3(a) also have a low voltage portion having N-channel and P-channel MOSFETs. The low voltage control
25 circuitry MOSFETs of the driver circuit 24 of Fig. 3(a) are schematically shown as formed within area 141. N⁺
contact region 125 is diffused in region 141 and receives an electrode which is at the potential V₁. The low
voltage control region 124 would also contain diffusions,
30 not shown, identical to the diffusions 160 to 164 in the high voltage region 40 of the low voltage transistors.
However, all the N⁺ and P⁺ diffusions in the low voltage control region 124 would receive electrodes which are at



levels between $-V_{sub}$ and V_1 . These would represent the sources and drains of the low voltage MOSFETs of the driver circuit 24 of Figure 3(a).

5 N+ contact regions 126 and 127 are diffused into layer 122 and receive metallic electrodes which can be at potentials between V_B (615V) and V_1 (600v). The P+ sinkers 130, 131, and 132 receive electrodes which are at $-V_{sub}$ potential. P(-) resurf regions 150 and 151 may encircle the high voltage region 140 to provide isolation from low voltage region 141.

10 As is conventional, all devices within the silicon surfaces are overcoated by a dielectric, for example, a low temperature silicon dioxide (silox) layer 180 which may have a thickness of about 1.5 micrometers. 15 Contacts to all surface electrodes penetrate the dielectric layer 180 and are taken to suitable external pins, not shown.

The device of Fig. 6(a) is also conventionally housed in a plastic housing 181 which overlies and 20 contacts the upper surface of the completed chip as schematically shown in Fig. 6(a). Plastics used for the housing may be any suitable insulation material such as those sold under the tradenames Nitto MP-150SG, Nitto MP-180, and Hysol MG15-F.

25 Fig. 6(a) shows the circuit cross-section for the circuit connected to V_B and V_1 in Fig. 3(a). Similar circuit constructions would be made for the circuits coupled to $V_{DD}-V_{ss}$ and $V_{cc}-COM$ of Fig. 3(a). These circuits would be identical but be separate. The only 30 difference would be that, for the $V_{DD}-V_{ss}$ circuit of Fig. 3(a), the point of Fig. 6(a) marked V_B would be connected to V_{cc} or V_{DD} , depending on whether the $V_{cc}-COM$ or $V_{DD}-V_{ss}$



circuit is at issue, and the point marked V_i in Fig. 6(a) would be connected to COM or V_{ss} , respectively.

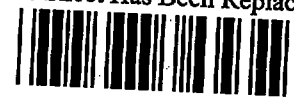
5 The circuit of Fig. 6(b), which shows the construction of a portion of the circuit of Fig. 3(b) is identical to that of Fig. 6(a), except that region 125 is coupled to V_{DD} . Regions 130, 131 and 132 remain connected to $-V_{sub}$. The V_B - V_i circuit is shown (driver 24 of Fig. 3(b)) is Fig. 3(b). A similar construction would be made for the V_{cc} -COM circuit (driver 26 of Fig. 3(b),
10 but the point of Fig. 6(b) marked V_B would be connected to V_{cc} and the point marked V_i would be coupled to COM.

Thus, there has been disclosed a method and circuit for driving power transistors in a half bridge configuration allowing excessive negative swing of the
15 output node without damage. Preferably, the circuit of the invention can be integrated on a single chip, e.g., a silicon chip. For example, the invention can be integrated in the design of conventional MOSFET driver chips, e.g., the IR2110 device.

20 Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore, the present invention should be limited not by the
25 specific disclosure herein, but only by the appended claims.



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WHAT IS CLAIMED IS:

1. A method for driving power transistors in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration comprising:
5 arranging first and second power transistors in series in a half bridge configuration with an output node between the transistors;
 connecting the series transistors between a first voltage source and a common potential;
10 providing a second voltage reference source;
 providing a terminal coupled to a common point coupled to anodes of intrinsic diodes of driver circuits for the power transistors; and
15 connecting the second voltage source between said common potential and said terminal so as to shift the level of said common point such that said intrinsic diodes will not forward bias due to negative transients at the output node.
2. The method recited in claim 1, further comprising coupling said second voltage reference source between the common potential and said common point coupled to the anodes of said intrinsic diodes such that
5 said common point is at a negative potential with respect to the common potential.
3. A circuit for driving power transistors arranged in series in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration,
5 the series transistors being adapted to be connected

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between a first voltage source and a common potential,
the circuit comprising:

driver circuits for each of the power
transistors;

10 a terminal connected to a common point
coupled to anodes of intrinsic diodes of the driver
circuits for the power transistors; and

the terminal being adapted to be connected
to a second voltage source provided between said common
15 potential and said terminal so as to shift the level of
said common point such that said intrinsic diodes will
not forward bias due to negative transients at the output
node.

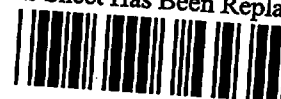
4. The circuit recited in claim 3, wherein
said second voltage reference source is adapted to be
coupled between said common potential and said common
point coupled to the anodes of said intrinsic diodes such
5 that said common point is at a negative potential with
respect to the common potential.

5. A method of integrating on a single
integrated circuit chip a circuit for driving power
transistors in a half bridge configuration allowing for
10 excessive negative swing of an output node between the
transistors in the half bridge configuration comprising:
arranging first and second power
transistors in series in a half bridge configuration with
an output node between the transistors;
15 connecting the series transistors between
a first voltage source and a common potential;
providing a second voltage reference
source;



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20 providing a terminal coupled to a common
point coupled to anodes of intrinsic diodes of driver
circuits for the power transistors; and
connecting the second voltage source
between said common potential and said terminal so as to
shift the level of said common point such that said
25 intrinsic diodes will not forward bias due to negative
transients at the output node.

6. The method recited in claim 5, further
comprising coupling said second voltage reference source
between the common potential and said common point
coupled to the anodes of said intrinsic diodes such that
said common point is at a negative potential with respect
to the common potential.

7. A circuit integrated on a single
integrated circuit chip for driving power transistors
arranged in series in a half bridge configuration
allowing for excessive negative swing of an output node
5 between the transistors in the half bridge configuration,
the series transistors being adapted to be connected
between a first voltage source and a common potential,
the circuit comprising:

10 driver circuits for each of the power
transistors;

a terminal connected to a common point
coupled to anodes of intrinsic diodes of the driver
circuits for the power transistors; and

15 the terminal being adapted to be connected
to a second voltage source provided between said common
potential and said terminal so as to shift the level of
said common point such that said intrinsic diodes will

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not forward bias due to negative transients at the output node.

- 5 8. The circuit recited in claim 7, wherein said second voltage reference source is adapted to be coupled between said common potential and said common point coupled to the anodes of said intrinsic diodes such that said common point is at a negative potential with respect to the common potential.



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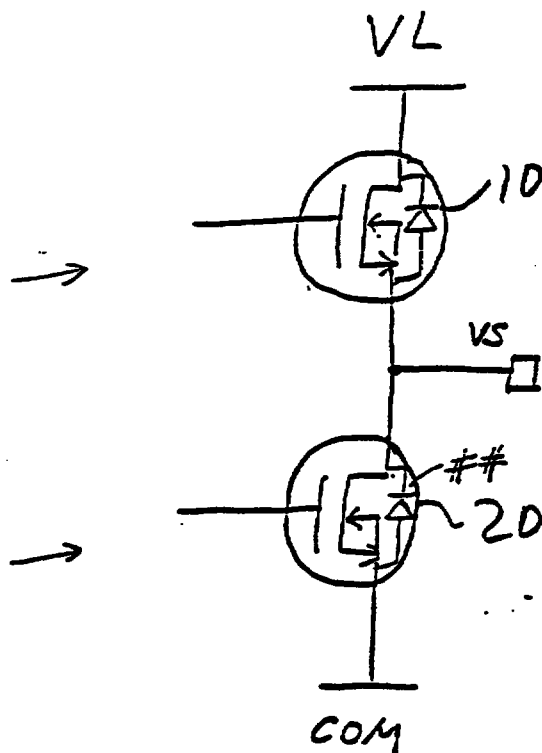
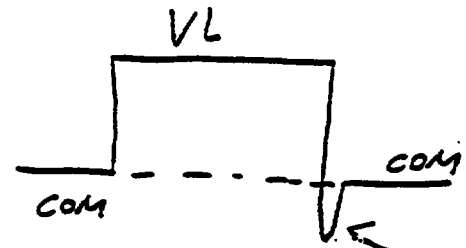


Fig 1(a)



NEGATIVE SPIKE AT V_S .

Fig.1(b)

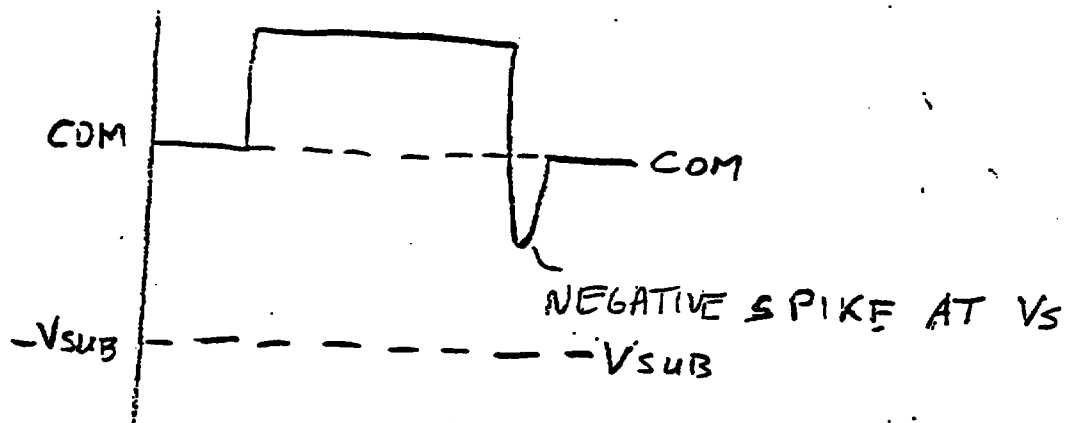


Fig 4

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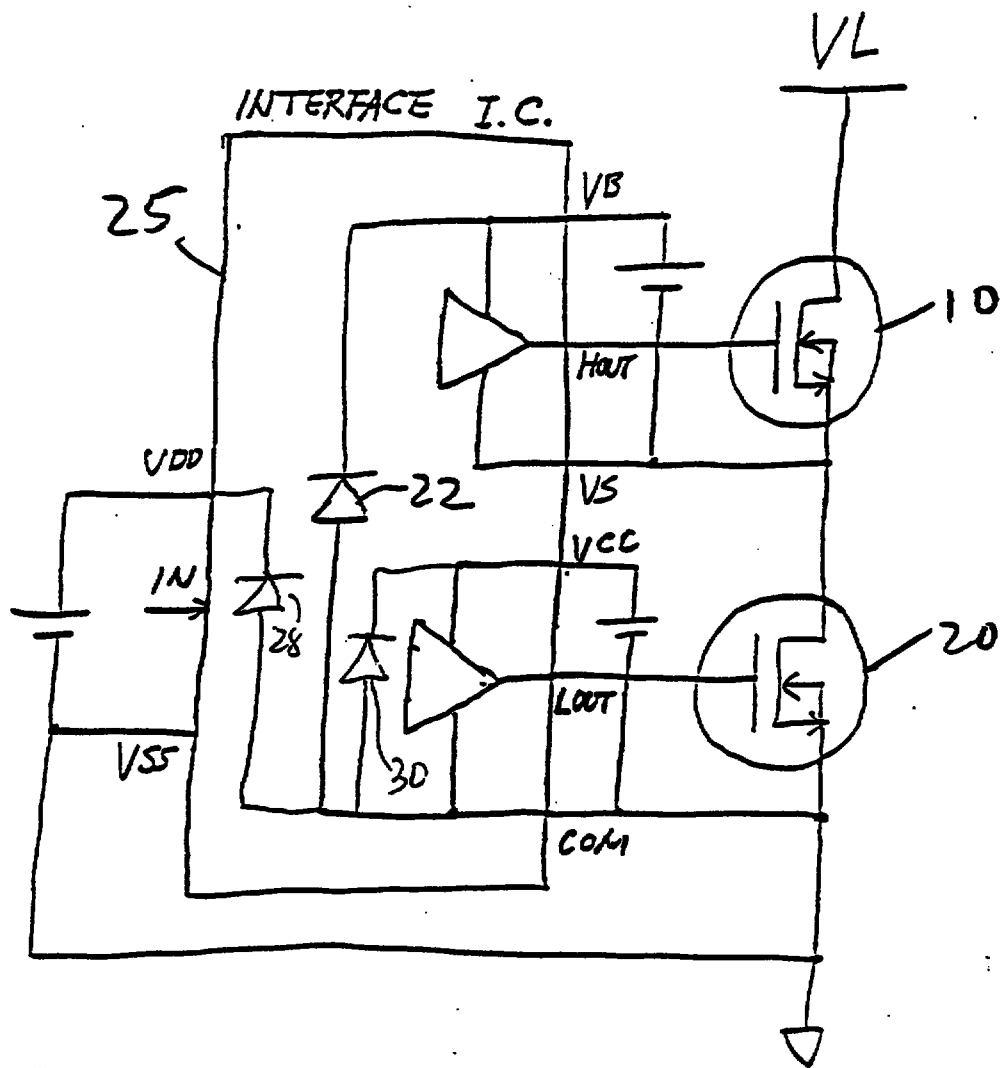


Fig. 2

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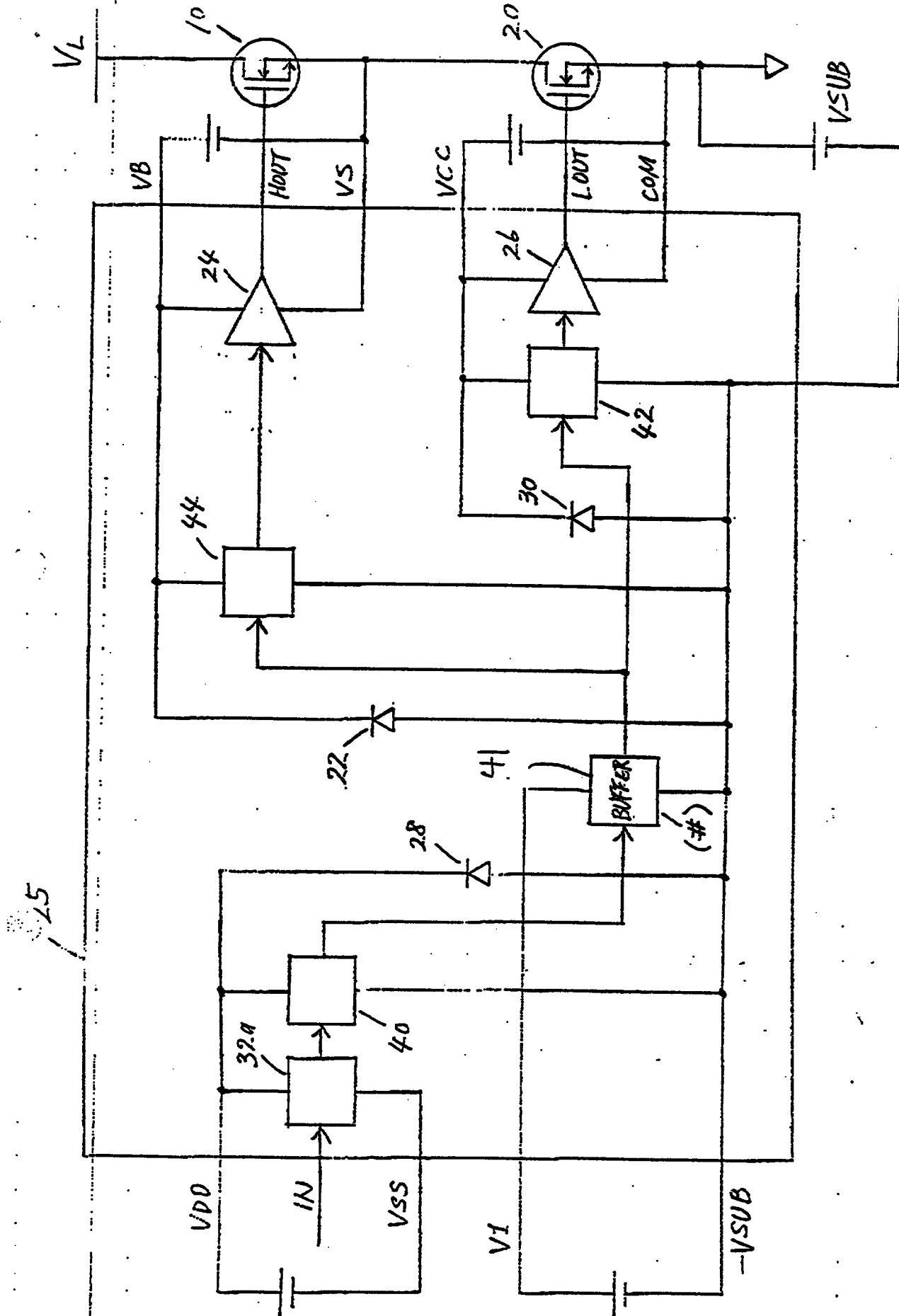


Fig. 3(a) (IR-1132)

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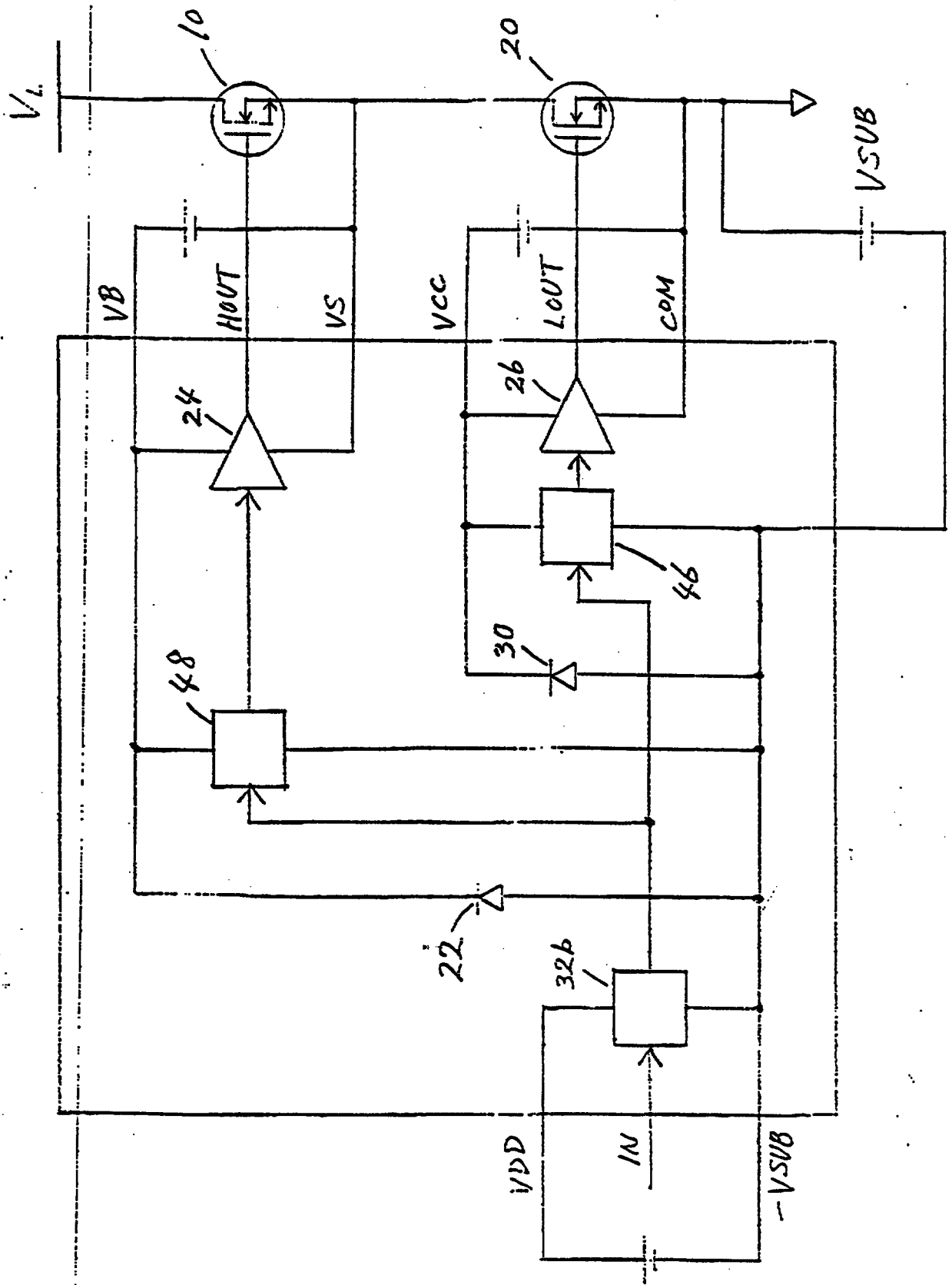


Fig. 3(b) (IR-1132)

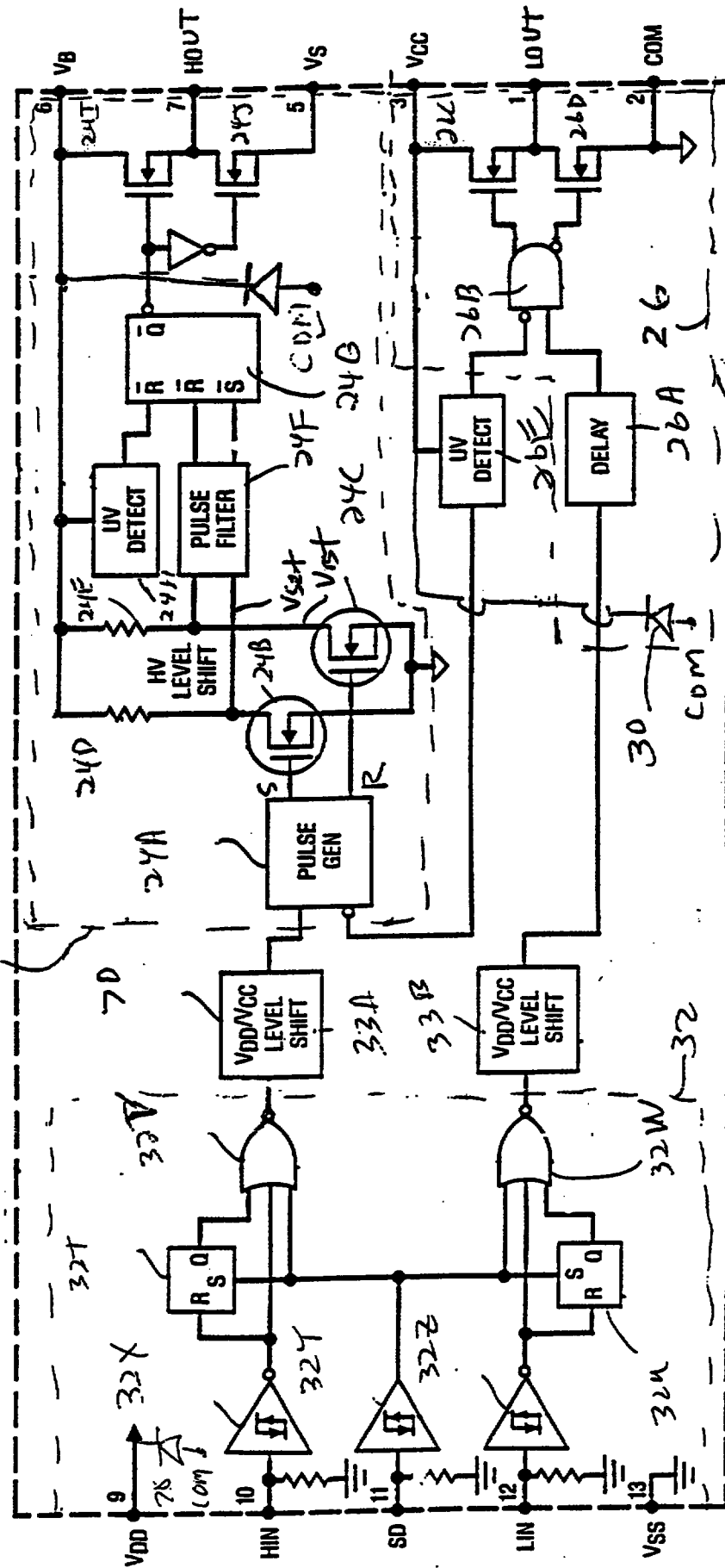
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FIG. 5

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PRIOR ART 26

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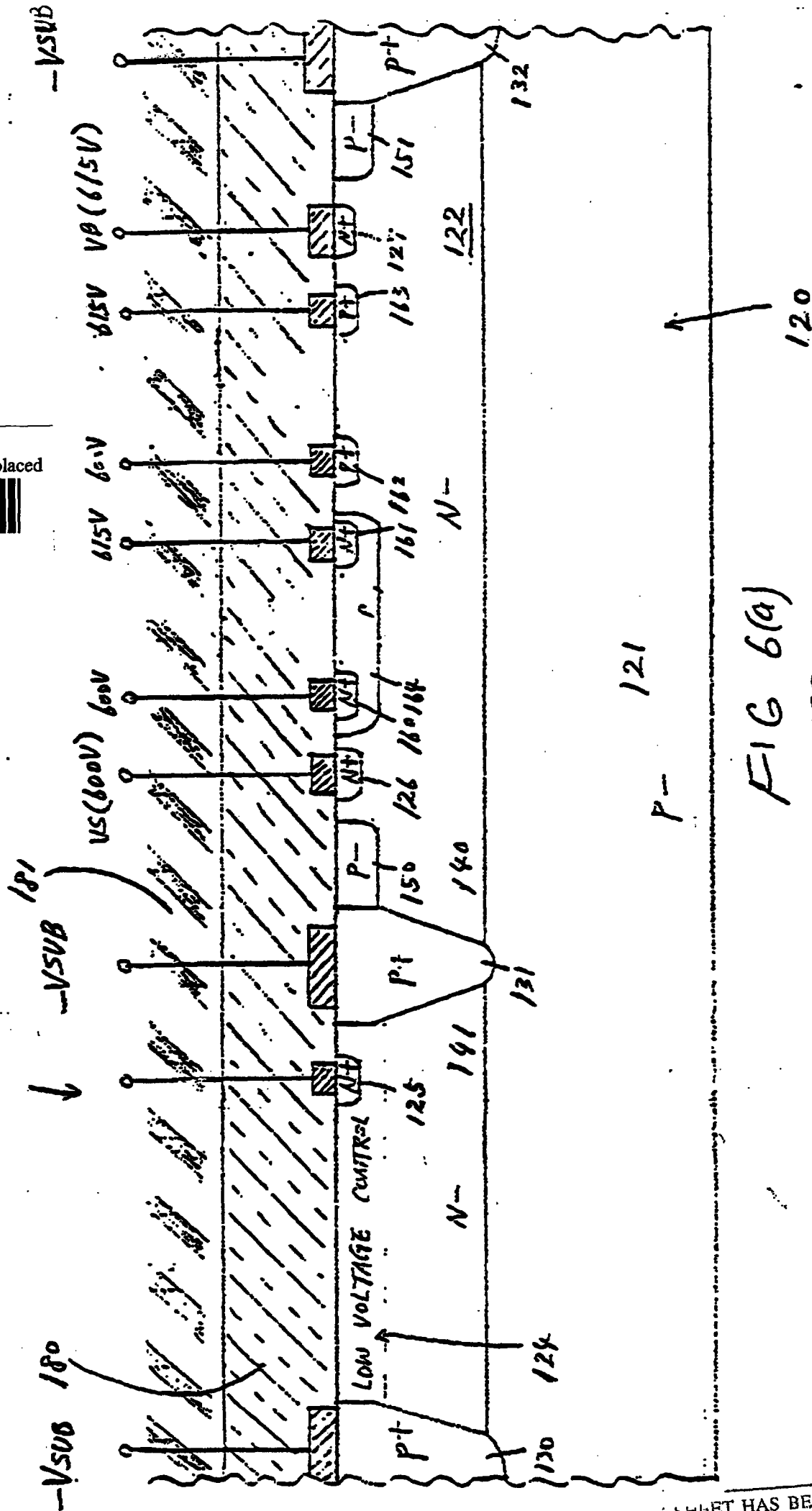


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FIG 6(a)
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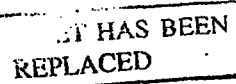


Fig 6(b)

**METHOD AND CIRCUIT FOR DRIVING POWER TRANSISTORS
IN A HALF BRIDGE CONFIGURATION ALLOWING FOR
EXCESSIVE NEGATIVE SWING OF THE OUTPUT NODE AND
INTEGRATED CIRCUIT INCORPORATING THE CIRCUIT**

ABSTRACT OF THE DISCLOSURE

A method and circuit for driving power transistors arranged in series in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration. The series transistors are connected between a first voltage source and a common potential. A second voltage reference source is also provided. A terminal is connected to a common point coupled to anodes of intrinsic diodes of driver circuits for the power transistors. The second voltage source is connected between the common potential and the terminal so as to shift the level of the common point such that the intrinsic diodes will not forward bias due to negative output node transients generated by diode forward recovery and stray inductances. The circuit of the invention can also be incorporated in an integrated circuit comprising a single chip, e.g., a silicon chip.

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METHOD AND INTEGRATED CIRCUIT FOR
DRIVING POWER TRANSISTORS

5 BACKGROUND OF THE INVENTION

The present invention is directed to a method and circuit for driving power transistors in a half bridge configuration allowing for excessive negative swing of the output node. It is also directed to an
10 integrated circuit incorporating the circuit, e.g., a circuit integrated on a single silicon chip.

In driver circuits for power transistors, for example, power MOSFETs driving power equipment, the power transistors often switch a large current. The large
15 switching current, combined with forward recovery characteristics of diodes and stray inductance in the circuit, generates a negative spike at the output node of the half bridge. These spike signals can be destructive to the driver circuits and also create noise.

20 SUMMARY OF THE INVENTION

It is accordingly, an object of the present invention to provide a method and circuit for driving power transistors in a half bridge configuration allowing for excessive negative swing of the output node.

25 It is furthermore an object of the present invention to provide such a circuit which can be integrated on a single chip.

The above and other objects of the invention are achieved by a method for driving power transistors in

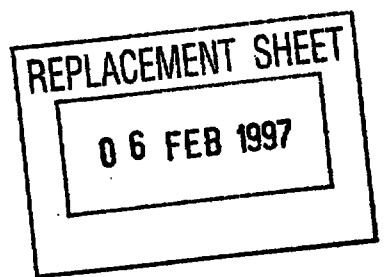
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a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration comprising arranging first and second power transistors in series in a half
5 bridge configuration with an output node between the transistors; connecting the series transistors between a first voltage source and a common potential; providing a second voltage reference source; providing a terminal connected to a common point coupled to anodes of
10 intrinsic diodes of driver circuits for the power transistors; and connecting the second voltage source between the common potential and the terminal so as to shift the level of the common point such that the intrinsic diodes will not forward bias due to negative
15 transients at the output node.

The above and other objects of the invention are also achieved by a circuit for driving power transistors arranged in series in a half bridge configuration allowing for excessive negative swing of an
20 output node between the transistors in the half bridge configuration, the series transistors being adapted to be connected between a first voltage source and a common potential, the circuit comprising: driver circuits for each of the power transistors, a terminal connected to a
25 common point coupled to anodes of intrinsic diodes of the driver circuits for the power transistors; and the terminal being adapted to be connected to a second voltage source provided between the common potential and the terminal so as to shift the level of the common point
30 such that the intrinsic diodes will not forward bias due to negative transients at the output node.

The above and other objects of the invention are also claimed by a method of integrating on a single



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integrated circuit chip a circuit for driving power transistors in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration comprising:

5 arranging first and second power transistors in series in a half bridge configuration with an output node between the transistors;

 connecting the series transistors between a first voltage source and a common potential;

10 providing a second voltage reference source;

 providing a terminal coupled to a common point coupled to anodes of intrinsic diodes of driver circuits for the power transistors; and

15 connecting the second voltage source between said common potential and said terminal so as to shift the level of said common point such that said intrinsic diodes will not forward bias due to negative transients at the output node.

20 The above and other objects of the invention are also achieved by a circuit integrated on a single integrated circuit chip for driving power transistors arranged in series in a half bridge configuration allowing for excessive negative swing of an output node
25 between the transistors in the half bridge configuration, the series transistors being adapted to be connected between a first voltage source and a common potential, the circuit comprising:

30 driver circuits for each of the power transistors;

 a terminal connected to a common point coupled to anodes of intrinsic diodes of the driver circuits for the power transistors; and

the terminal being adapted to be connected to a second voltage source provided between said common potential and said terminal so as to shift the level of said common point such that said intrinsic diodes will not forward bias due to negative transients at the output node.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1(a) shows power transistors, illustratively power mosfets, arranged in a half bridge configuration;

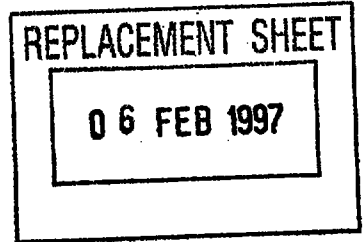
Figure 1(b) shows a typical output pulse at the common output node of the power transistors, including a negative spike, as encountered in the prior art circuits;

Figure 2 shows a typical half bridge configuration interfaced with a driver interface IC which provides the driver signals to drive the power transistors;

Figures 3(a) and 3(b) show two arrangements according to the invention which allow power transistors and the driver circuits to operate with negative output node spikes without damage;

Figure 4 shows an output pulse of the circuit of Figures 3(a) or 3(b), illustrating how the circuit of the invention prevents driver circuit intrinsic diode forward biasing, thereby allowing operation of the circuit without damage from negative output node spikes;

Figure 5 shows a conventional integrated circuit driver which can be modified in accordance with



the invention to incorporate the circuit of the invention;

5 Figure 6(a) shows how a portion of the circuit of Fig. 3(a) can be implemented in an integrated circuit; and

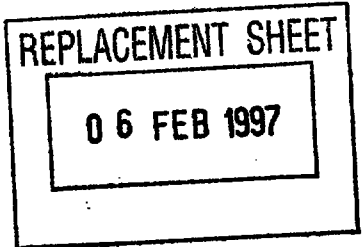
 Figure 6(b) shows how a portion of the circuit of Fig. 3(b) can be implemented in an integrated circuit.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

10 With reference now to the drawings, Figure 1(a) shows power transistors, in particular, power mosfets, in a typical half bridge circuit. In the arrangement shown, two power transistors are configured in series in a totem pole arrangement. The high side transistor 10 has its drain connected to a voltage supply VL and the low side
15 transistor 20 has its source connected to a common reference point. The output may be taken at the common node between the two transistors 10 and 20 and is coupled to the VS pin from the driver circuit coupled to the power transistors, and described in more detail with
20 reference to Figure 2.

 In a half bridge circuit, the output node typically swings below ground (COM) as shown in Figure 1(b). This negative spike is typically higher for high power circuits or highly inductive circuits and can reach
25 tens of volts.

 With reference to Figure 2, which shows the half bridge configuration being driven by an interface chip 25, for example, the IR 2110 available from International Rectifier Corp., in such a junction
30 isolated integrated circuit 25, VS cannot fall below reference COM by more than the supply potential VB because the supply potential VB will also fall below COM



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and the inherent diode 22 between VB and COM will forward bias. This inherent or parasitic diode 22 is typically present in driver circuits of the type shown in Figure 2. In some situations, the forward biasing of this diode can
5 create significant currents which can damage the diode or other parts of the circuit. Therefore, it is preferable to prevent the parasitic diode 22 from forward biasing if possible, so as to prevent damage to the circuit. In addition to the parasitic diode 22, a parasitic diode 28
10 between VDD and COM and another parasitic diode 30 between VCC and COM are also present.

Figure 5 shows a conventional interface chip 25 in greater detail. In particular, Figure 5 shows the details of a conventional IR-2110 integrated circuit
15 driver device. This device can be modified in accordance with the invention to incorporate the circuit of the invention which is shown in detail in Figures 3(a) and 3(b).

Figure 5 is a functional block diagram of the
20 circuit contained within the integrated circuit 25 in Figure 2. Logic input pins 10, 11 and 12 are connected through Schmitt triggers 32X, 32Y and 32Z to the RS latches 32T and 32U and to logic circuits 32V and 32W. The outputs of logic circuits 32V and 32W are coupled,
25 respectively, to level shift circuits 33A and 33B. As will be seen, the outputs of the level shift circuits 33A and 33B control the high side control output and low side control output at pins 7 and 1, respectively.

The output from level shift circuit 33B in the
30 low voltage channel is applied through a delay circuit 26A and one input of gate circuit 26B. The output of gate 26B is connected to the gate electrodes of driver output MOSFET transistors 26C and 26D. As will be later

described, these transistors will produce a gate voltage at pin 1 (L OUT) when required by the logic input to pins 11 and 12.

5 The circuit of Figure 5 also contains an under-voltage detection circuit 27 which disables the output from gate 26B when an under voltage is detected at pin 3 (VCC) to prevent turn-on of the power MOSFET or IGBT operated from pin 1.

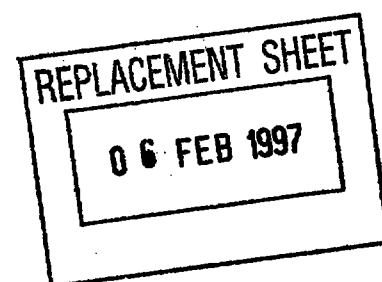
10 The level shift circuit 33A for the high voltage channel of the circuit has one input connected to the pulse generator 24A. Under-voltage detection circuit 27 is also connected to pulse generator 24A and will turn off the high voltage output channel responsive to the detection of an under-voltage condition at pin 3 (VCC).

15 Pulse generator 24A has two outputs, a set(s) output connected to the gate of MOSFET 24B and a reset (R) output connected to the gate of MOSFET 24C.

20 The sources of MOSFETs 24B and 24C are connected to a common connection rail and their drains are connected to resistors 24D and 24E, respectively.

25 During normal operation, the application of pulses to MOSFETs 24B and 24C from the pulse generator 24A will produce output voltage pulses Vset and Vrst at the nodes between MOSFETs 24B and 24C and their respective resistors 24D and 24E.

30 The pulses Vset and Vrst are then applied to a pulse filter 24F. The output channels of filter 24F are connected to the R and S inputs of latch 24G. A second under-voltage detection circuit 24H is provided as an input to the latch 24G to ensure that no signal is applied at pin 7 if an under-voltage is detected at pin 6.



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The output of the RS latch 24G is then used to turn driver MOSFETs 24I and 24J on and off. Thus, if a high signal is applied to input R of the RS latch 24G, the output at pin 7 is turned off. If a high signal is applied to the S input of latch 24G, the output at pin 7 will turn on.

Figure 5 shows the intrinsic diode 22 present between VB and COM, shown also in Figure 2. In addition, intrinsic diodes are also found between VDD and COM and between VCC and COM. See diodes 28 and 30 in Figure 5.

Figures 3(a) and 3(b) show two examples of how transistors in a half bridge configuration can be operated in a safe manner and allowing for excessive negative swing of the output node without damage to the driver circuits. These figures show how the circuit of Figure 5 can be modified in accordance with the invention. The allowable negative spike at the output node between transistors 10 and 20 can be increased using either one of the two circuits shown in Figure 3(a) or Figure 3(b).

According to the invention, the common anodes of intrinsic diodes 22, 28 and 30, which are always present as shown in the drawing figures, are floated with respect to the reference COM of the low side driver circuit 26 by a voltage V_{sub} . As shown, the floating voltage supply V_{sub} is polarized such that the anodes of the intrinsic diodes 22, 28 and 30 are at a negative potential- V_{sub} with respect to COM. In this way, VS can fall below COM by up to the V_{sub} potential. This configuration allows for the custom setting of the allowable negative spike at the output node VS for a given application.

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The two circuits of Figures 3(a) and 3(b) differ only by the fact that the input logic circuits 32a and 32b are referenced differently. In Figures 3(a) and 3(b), the details of the interface circuit 25, shown in Figure 5, are not shown. In Figures 3(a) and 3(b), suitable level shifting circuits are necessary to supply the driver signals from input circuits 32a and 32b to the driver circuits 24 and 26. Such level shifting circuits can be of the type disclosed in copending application Serial No. IR-1122, filed concurrently herewith and the disclosure of which is incorporated by reference herein.

In Figure 3(a), the input circuit 32a floats above the voltage $-V_{sub}$. Accordingly, in the circuit of Fig. 3(a), a level shifting circuit 40 will be necessary to shift the level of the output of input circuit 32a first to the $-V_{sub}$ reference level. The output of the level shifting circuit 40 is coupled to a buffer 41, and the output of the buffer 41 is coupled to level shifting circuits 44 and 42. The level shifting circuit 42 is necessary to shift the level of the signals from the $-V_{sub}$ level to the level COM to drive the low side driver circuit 26, and the level shifting circuit 44 is necessary to shift the level of the signals from the $-V_{sub}$ level to the reference level VB to drive the high side driver circuit 24.

In Figure 3(b), since the input circuit 32b is already referenced to the $-V_{sub}$ level, only two level shifting circuits are necessary, one (46) to shift the level of the output of the input circuit 32b to the COM reference level for driving the low side driver circuit 26 and another (48) to shift the reference level to the reference level VB of the high side driver circuit 24.

REPLACEMENT SHEET

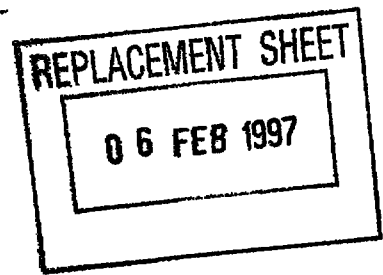
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Because the anode of the intrinsic diode 22 is now at the level $-V_{sub}$ with respect to the reference level COM in the circuits of Figures 3(a) and 3(b), this diode will not forward bias if V_S falls below COM by up to the V_{sub} potential. This is shown graphically in Fig. 4, which shows the negative spike at the output node V_S above the $-V_{sub}$ potential, thereby preventing intrinsic diode forward conduction. Accordingly, the high current conditions caused in the prior art circuit of Figure 2 due to the forward biasing of the intrinsic diodes cannot occur.

Figures 6(a) and 6(b) show how portions of the circuits of respective Figures 3(a) and 3(b) can be implemented in an integrated circuit. Figure 6(a) shows a portion of the circuit of Figure 3(a) and Figure 6(b) shows a portion of the circuit Figure 3(b). Two circuit structures are essentially identical. The only difference is that the various terminals are connected to points of different potential. These are shown in Figures 6(a) and 6(b). A description of Figure 6(a) will now be given. For brevity, a detailed description of Figure 6(b) will not be given. The reader can observe the differences in potentials by the comparing the two Figures.

When implementing the circuit of Figure 3(a) in a common chip, the high and low voltage circuits are laterally isolated from one another. Figure 6(a) shows a portion of such a chip in cross-section. Thus, in Figure 6(a), a silicon chip 120 consists of a P⁺ substrate 121 which has an epitaxially layer 122 of N⁻ silicon grown thereon. The N⁻ region 122 is separated into high voltage and low voltage regions by P⁺ sinkers 130, 131 and 132. Thus, sinkers 130 and 131 define a high voltage



device region 140 in epitaxial layer 122, separated from low voltage region 141. Regions 140 and 141 can have any desired pathology. Moreover, any desired isolation technique can be used between regions 140 and 141.

5 Typically, MOSFET driver circuits, such as the circuit 24 in Figure 3(a), comprise P channel and N channel MOSFET transistors. This is described in co-
10 pending patent application Serial No. 08/274,012 (IR-1131), assigned to the assignee of this application. The disclosure of that application is incorporated by
15 reference herein. The high voltage circuitry MOSFETs of the driver circuit 24 of the Figure 3(a) are shown as formed within high voltage region 140. The P⁺ contact regions 162 and 163, which are diffused in layers 122,
20 represent any of the source and drains of the P channel MOSFETs of the driver device 24. The P region 164 is diffused in layer 122 to form the P-type well region. The N⁺ contact regions 160 and 161, which are diffused in the P-type region 64, represent any of the sources and
25 drains of the N channel MOSFETs of the driver device 24 of Figure 3(a).

 Typically, driver devices like circuit 24 of Figure 3(a) also have a low voltage portion having N-channel and P-channel MOSFETS. The low voltage control
25 circuitry MOSFETs of the driver circuit 24 of Fig. 3(a) are schematically shown as formed within area 141. N⁺ contact region 125 is diffused in region 141 and receives an electrode which is at the potential V₁. The low voltage control region 124 would also contain diffusions,
30 not shown, identical to the diffusions 160 to 164 in the high voltage region 40 of the low voltage transistors. However, all the N⁺ and P⁺ diffusions in the low voltage control region 124 would receive electrodes which are at

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levels between $-V_{sub}$ and V_1 . These would represent the sources and drains of the low voltage MOSFETs of the driver circuit 24 of Figure 3(a).

5 N+ contact regions 126 and 127 are diffused into layer 122 and receive metallic electrodes which can be at potentials between V_B (615V) and V_1 (600v). The P+ sinkers 130, 131, and 132 receive electrodes which are at $-V_{sub}$ potential. P(-) resurf regions 150 and 151 may encircle the high voltage region 140 to provide isolation from low voltage region 141.

10 As is conventional, all devices within the silicon surfaces are overcoated by a dielectric, for example, a low temperature silicon dioxide (silox) layer 180 which may have a thickness of about 1.5 micrometers. 15 Contacts to all surface electrodes penetrate the dielectric layer 180 and are taken to suitable external pins, not shown.

The device of Fig. 6(a) is also conventionally housed in a plastic housing 181 which overlies and 20 contacts the upper surface of the completed chip as schematically shown in Fig. 6(a). Plastics used for the housing may be any suitable insulation material such as those sold under the tradenames Nitto MP-150SG, Nitto MP-180, and Hysol MG15-F.

25 Fig. 6(a) shows the circuit cross-section for the circuit connected to V_B and V_1 in Fig. 3(a). Similar circuit constructions would be made for the circuits coupled to $V_{DD}-V_{ss}$ and $V_{cc}-COM$ of Fig. 3(a). These circuits would be identical but be separate. The only 30 difference would be that, for the $V_{DD}-V_{ss}$ circuit of Fig. 3(a), the point of Fig. 6(a) marked V_B would be connected to V_{cc} or V_{DD} , depending on whether the $V_{cc}-COM$ or $V_{DD}-V_{ss}$

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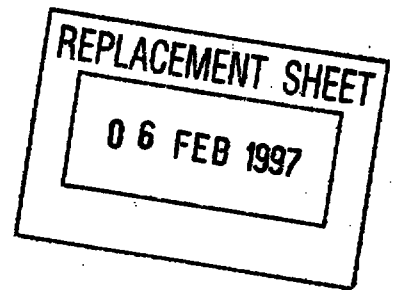
- 13 -

circuit is at issue, and the point marked V_i in Fig. 6(a) would be connected to COM or V_{ss} , respectively.

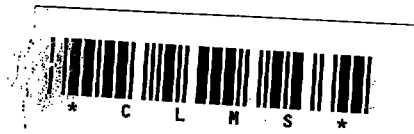
5 The circuit of Fig. 6(b), which shows the construction of a portion of the circuit of Fig. 3(b) is identical to that of Fig. 6(a), except that region 125 is coupled to V_{DD} . Regions 130, 131 and 132 remain connected to $-V_{sub}$. The V_B - V_i circuit is shown (driver 24 of Fig. 3(b)) is Fig. 3(b). A similar construction would be made for the V_{cc} -COM circuit (driver 26 of Fig. 3(b),
10 but the point of Fig. 6(b) marked V_B would be connected to V_{cc} and the point marked V_i would be coupled to COM.

Thus, there has been disclosed a method and circuit for driving power transistors in a half bridge configuration allowing excessive negative swing of the
15 output node without damage. Preferably, the circuit of the invention can be integrated on a single chip, e.g., a silicon chip. For example, the invention can be integrated in the design of conventional MOSFET driver chips, e.g., the IR2110 device.

20 Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore, the present invention should be limited not by the
25 specific disclosure herein, but only by the appended claims.



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WHAT IS CLAIMED IS:

1. A method for driving power transistors in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration comprising:

5 arranging first and second power transistors in series in a half bridge configuration with an output node between the transistors;

connecting the series transistors between a first voltage source and a common potential;

10 providing a second voltage reference source;

providing a terminal coupled to a common point coupled to anodes of intrinsic diodes of driver circuits for the power transistors; and

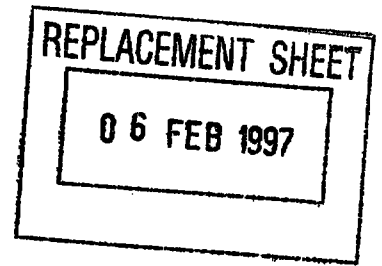
15 connecting the second voltage source between said common potential and said terminal so as to shift the level of said common point such that said intrinsic diodes will not forward bias due to negative transients at the output node.

2. The method recited in claim 1, further comprising coupling said second voltage reference source between the common potential and said common point coupled to the anodes of said intrinsic diodes such that
5 said common point is at a negative potential with respect to the common potential.

3. A circuit for driving power transistors arranged in series in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration,
5 the series transistors being adapted to be connected



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between a first voltage source and a common potential,
the circuit comprising:

driver circuits for each of the power
transistors;

10 a terminal connected to a common point
coupled to anodes of intrinsic diodes of the driver
circuits for the power transistors; and

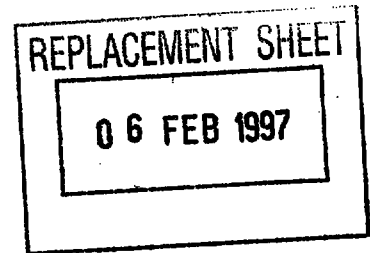
15 the terminal being adapted to be connected
to a second voltage source provided between said common
potential and said terminal so as to shift the level of
said common point such that said intrinsic diodes will
not forward bias due to negative transients at the output
node.

4. The circuit recited in claim 3, wherein
said second voltage reference source is adapted to be
coupled between said common potential and said common
point coupled to the anodes of said intrinsic diodes such
5 that said common point is at a negative potential with
respect to the common potential.

5. A method of integrating on a single
integrated circuit chip a circuit for driving power
transistors in a half bridge configuration allowing for
10 excessive negative swing of an output node between the
transistors in the half bridge configuration comprising:
 arranging first and second power
transistors in series in a half bridge configuration with
an output node between the transistors;
15 connecting the series transistors between
a first voltage source and a common potential;
 providing a second voltage reference
source;



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20 providing a terminal coupled to a common point coupled to anodes of intrinsic diodes of driver circuits for the power transistors; and

connecting the second voltage source between said common potential and said terminal so as to shift the level of said common point such that said
25 intrinsic diodes will not forward bias due to negative transients at the output node.

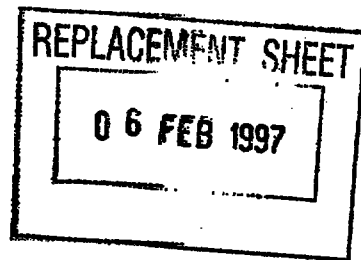
6. The method recited in claim 5, further comprising coupling said second voltage reference source between the common potential and said common point coupled to the anodes of said intrinsic diodes such that said common point is at a negative potential with respect to the common potential.

7. A circuit integrated on a single integrated circuit chip for driving power transistors arranged in series in a half bridge configuration allowing for excessive negative swing of an output node
5 between the transistors in the half bridge configuration, the series transistors being adapted to be connected between a first voltage source and a common potential, the circuit comprising:

10 driver circuits for each of the power transistors;

a terminal connected to a common point coupled to anodes of intrinsic diodes of the driver circuits for the power transistors; and

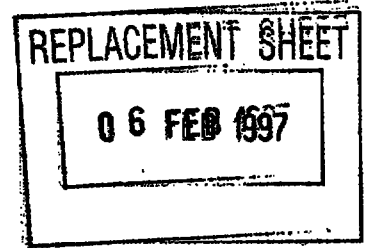
15 the terminal being adapted to be connected to a second voltage source provided between said common potential and said terminal so as to shift the level of said common point such that said intrinsic diodes will



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not forward bias due to negative transients at the output node.

8. The circuit recited in claim 7, wherein said second voltage reference source is adapted to be coupled between said common potential and said common point coupled to the anodes of said intrinsic diodes such that said common point is at a negative potential with respect to the common potential.



METHOD AND INTEGRATED CIRCUIT FOR
DRIVING POWER TRANSISTORS

ABSTRACT OF THE DISCLOSURE

A method and circuit for driving power transistors arranged in series in a half bridge configuration allowing for excessive negative swing of an output node between the transistors in the half bridge configuration. The series transistors are connected between a first voltage source and a common potential. A second voltage reference source is also provided. A terminal is connected to a common point coupled to anodes of intrinsic diodes of driver circuits for the power transistors. The second voltage source is connected between the common potential and the terminal so as to shift the level of the common point such that the intrinsic diodes will not forward bias due to negative output node transients generated by diode forward recovery and stray inductances. The circuit of the invention can also be incorporated in an integrated circuit comprising a single chip, e.g., a silicon chip.

Figure 3B

FIG. 1 a

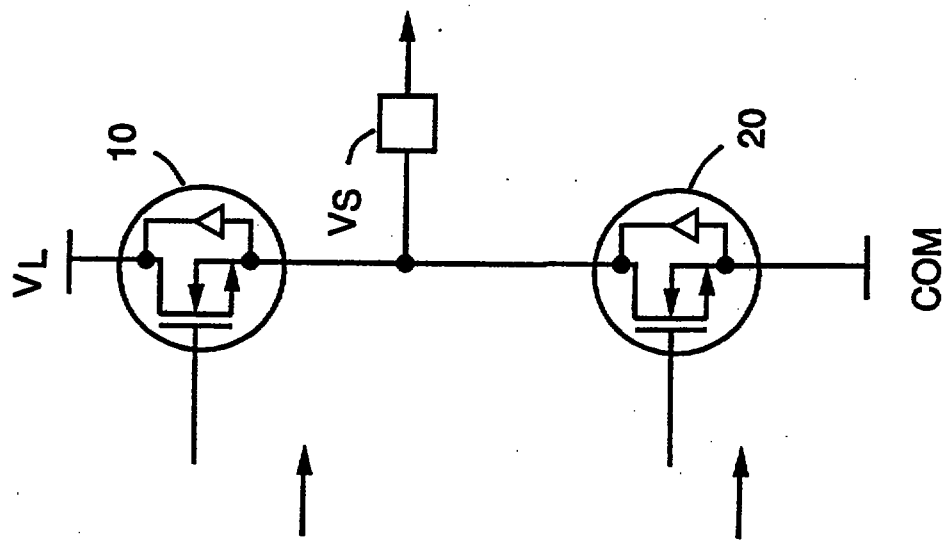


FIG. 1 b

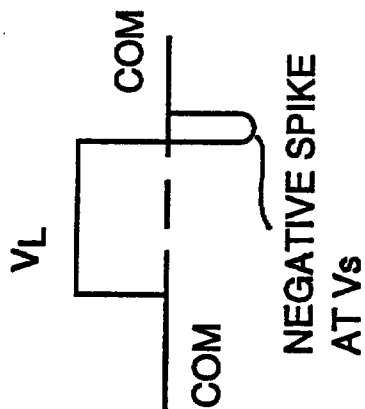
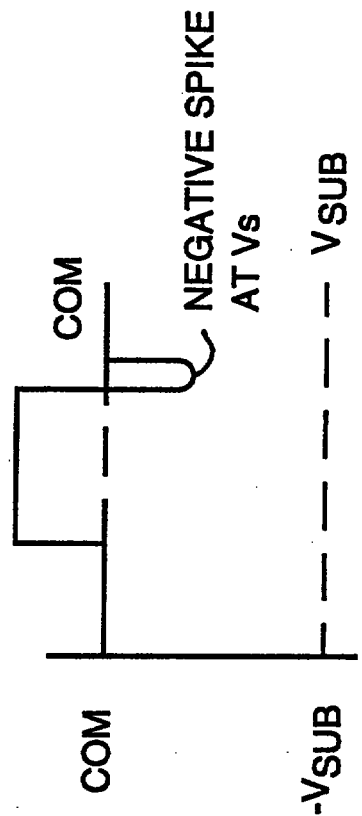


FIG. 4



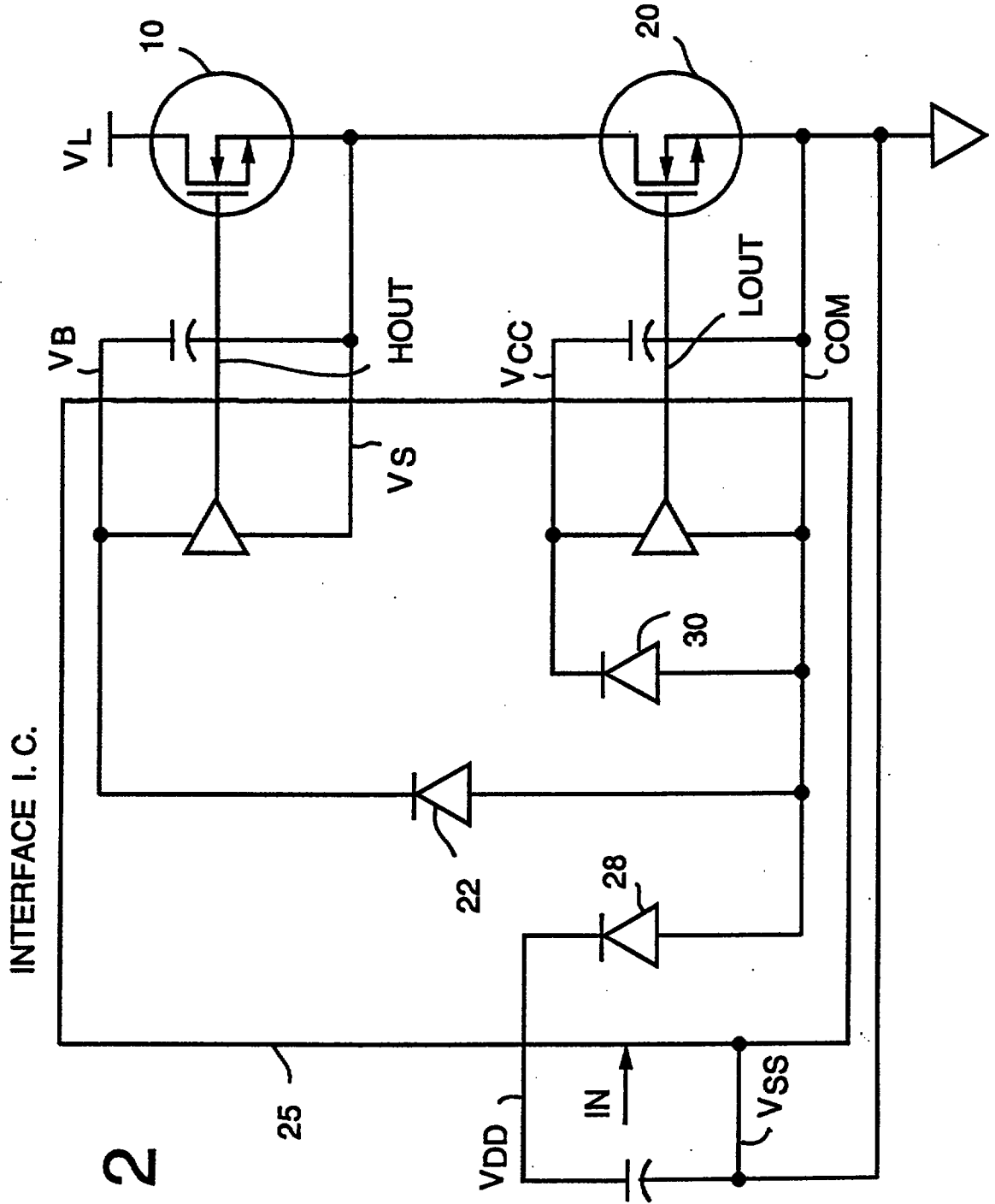


FIG. 2

25)

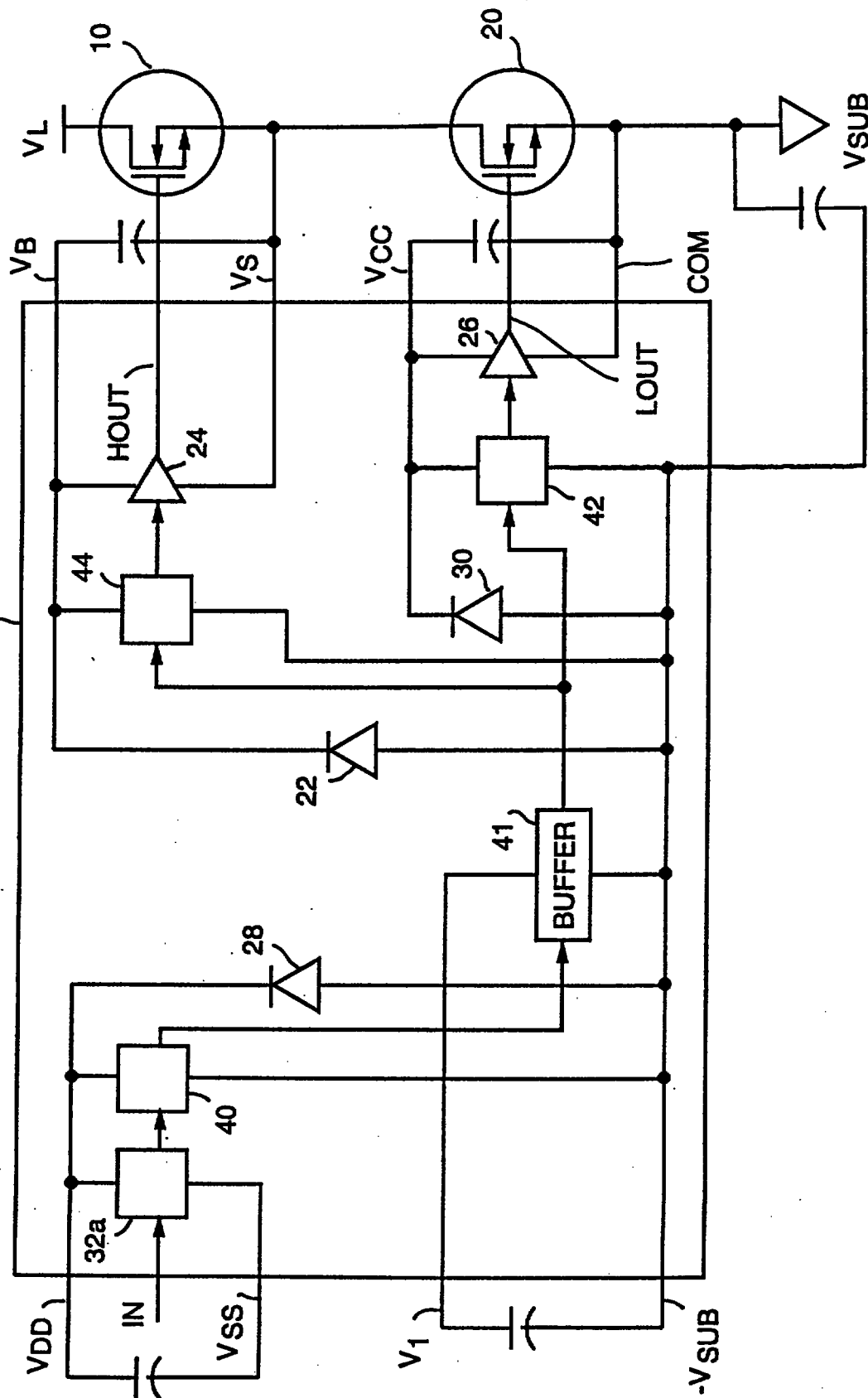
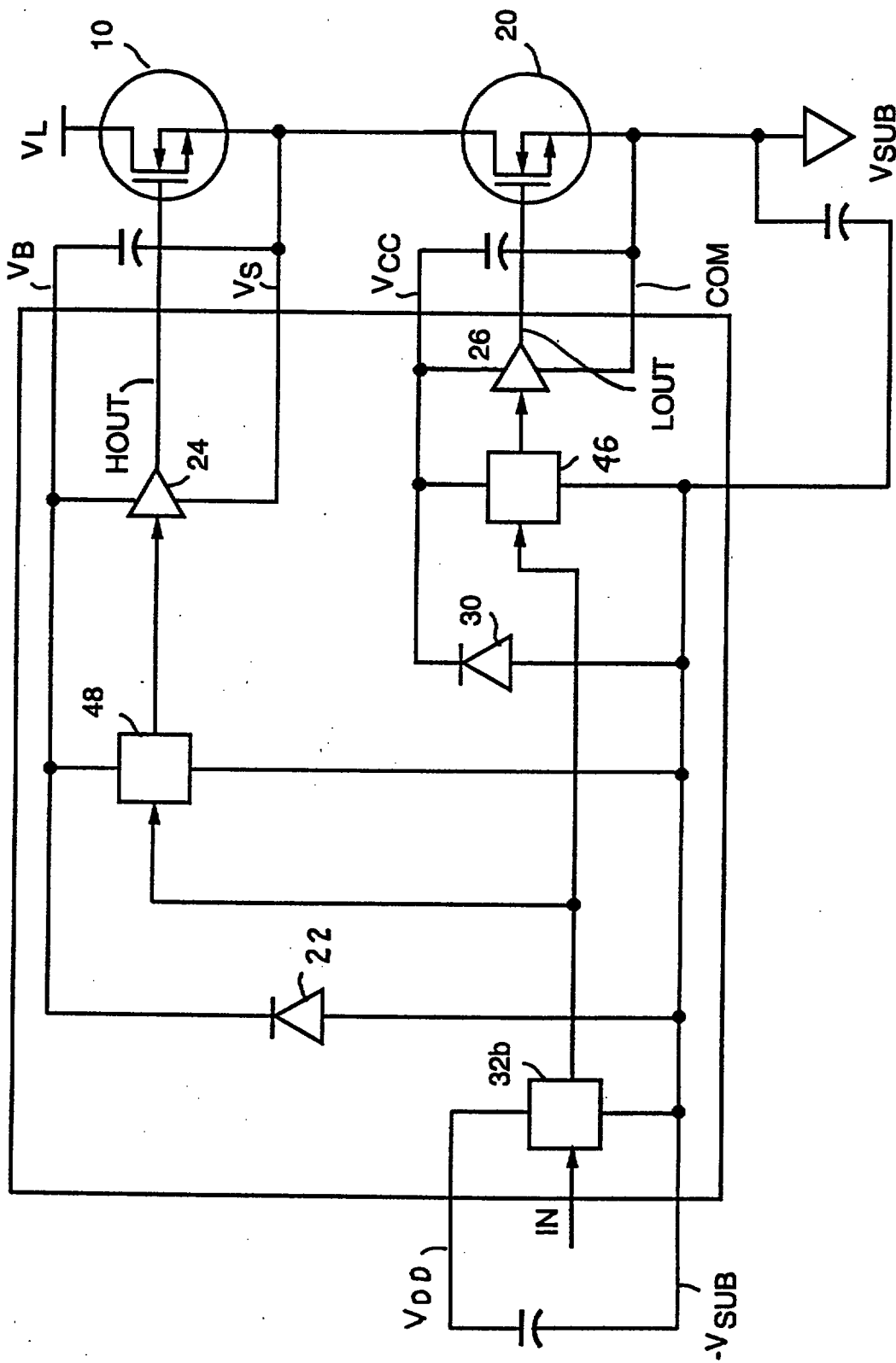


FIG. 3 b



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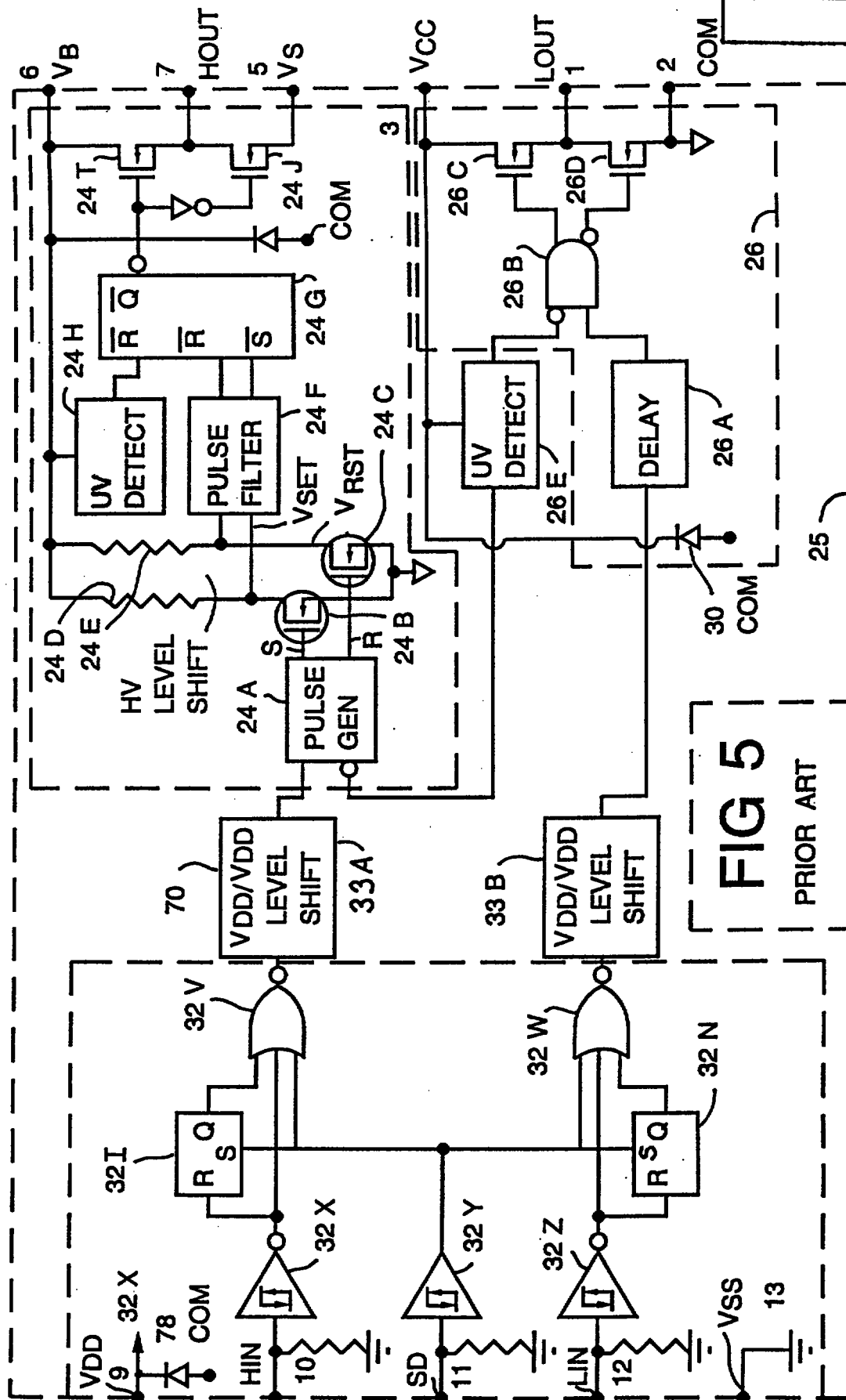


FIG 6 a

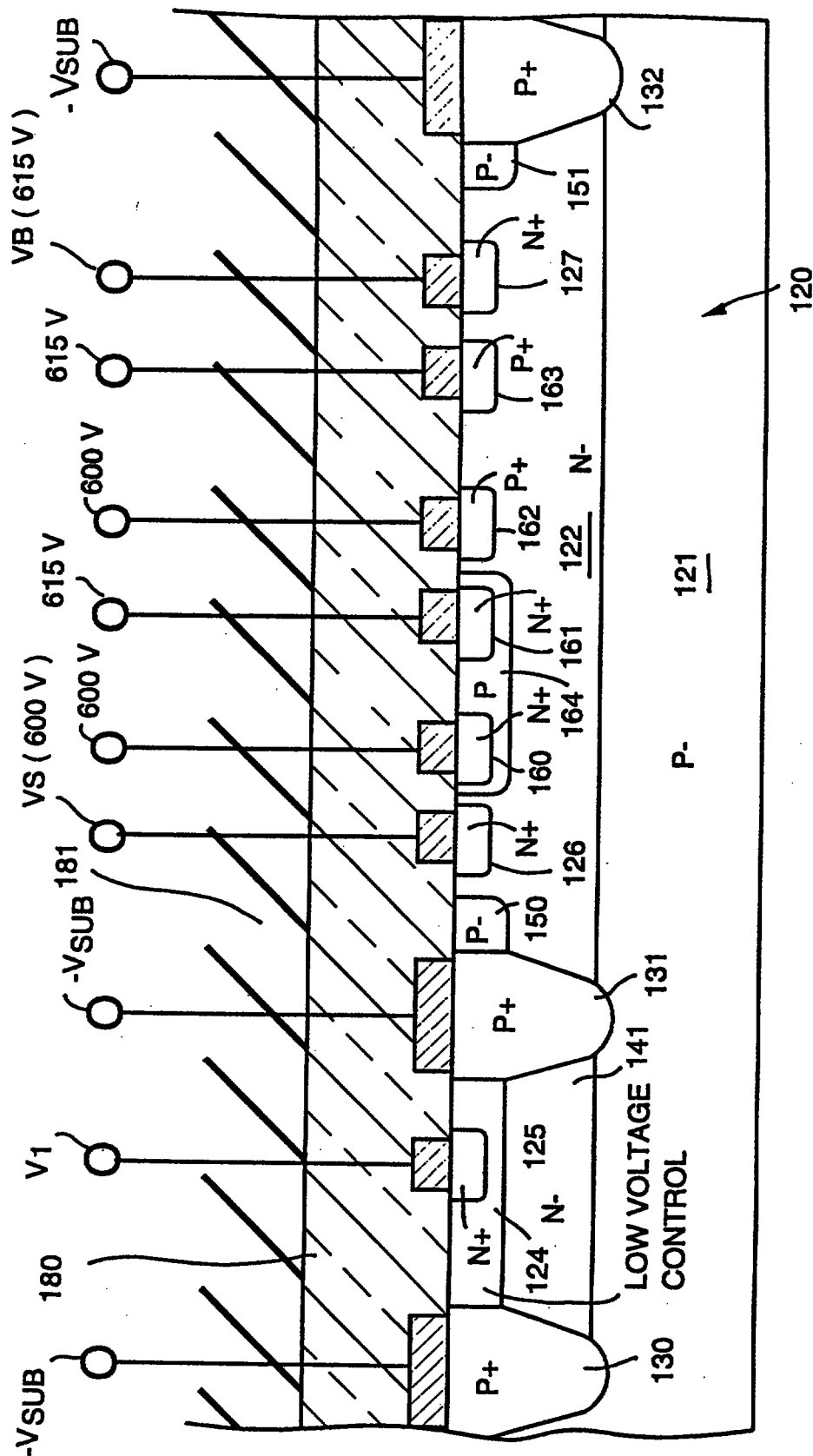


FIG 6 b

