

ABSTRACT

The present application relates to a write data signal delay control method. The method comprises: performing working mode configuration on a register circuit in a memory by means of a host, so as to obtain a training register, which supports reading and writing (202); sending a sample write data signal to the memory by means of the host (204); sampling the sample write data signal by means of the memory on the basis of a sampling signal, and caching a sampled write data signal, which is obtained by means of sampling, into the training register (206); if the sampled write data signal, which is read by the host from the training register, is inconsistent with the sample write data signal, performing, on the basis of the sample write data signal, delay adjustment training on a write data delay control circuit, which is provided on the host, so as to obtain a trained write data delay control circuit (208); and performing signal offset adjustment on the write data signals, which are input, by means of the trained write data delay control circuit, so as to obtain a target write data signal, which is aligned with a sampling edge of the sampling signal and is to be written to the memory (210).