Description

This invention relates to television apparatus and particularly to receivers intended for use with auxiliary signal sources of a type providing separated luminance and chrominance output signals and extended luminance signal bandwidth.

Video cassette recorders (VCRs) and combination camera-recorders (camcorders) have been proposed that provide a relatively wideband luminance signal response (e.g., 5 MHz) and which include an output connector (commonly called an "S-terminal") that provides separated luminance and chrominance output signals. An advantage of this new video interconnection format is that one may apply the separated luminance and chrominance signals to the display processing circuits of a television receiver directly without going through the receiver's internal comb filter. Advantageously, this signal format eliminates interference effects such as cross-color and cross-luminance which otherwise could occur if the luminance and chrominance signals were to be combined as a composite video signal for application to the receiver. See, generally, the article "Hitachi S-VHS Digital Hi-Fi Videotape Recorder VT-Z70" published in TV GIJUTSU, August, 1987, at pages 24-37. See also the article "Sony Introduces 8mm Hi-Band Products" published in TV DIGEST, Vol. 29, No. 7, Feb. 13, 1989.

It would be desirable to be able to add an auxiliary input connector to a conventional television receiver to facilitate the display of video signals of the proposed wideband Y-C format. The problem, to which the present invention is addressed, is to add Y-C input capability to a conventional receiver without the necessity of making major modifications to the existing receiver signal processing circuits. The present invention is particularly directed to providing peaking of the wideband luminance input signal.

The present invention provides television apparatus comprising a first luminance signal source comprising a source of composite video signals inclusive of luminance and chrominance signal components, and means for separating said luminance signal component from said composite video signals; a second luminance signal source providing a luminance signal exhibiting a bandwidth wider than the bandwidth of said separated lumiannce signal component provided by said first souce; a display processor having a luminance input coupled to said first luminance signal source via a first luminance peaking circuit and coupled to said second luminance signal source via a circuit path; characterized in that said second luminance signal source is coupled via said circuit path to an input of said first luminance peaking circuit to which said first luminance signal source is coupled; and said circuit path includes a second luminance peaking circuit for subjecting a luminance signal provided by said second luminance signal source to peaking by the combination of said first and second peaking circuits, wherein said second luminance peaking circuit exhibits peaking in a frequency region higher than that of said first luminance peaking circuit.

Television apparatus embodying the invention includes a display processor having an input coupled to a first video source via a first luminance peaking circuit and coupled to a second video source via a circuit path. A second video source is coupled via the circuit path to an input of the first luminance peaking circuit to which the first video source is coupled. The circuit path includes a second luminance peaking circuit for subjecting a luminance input signal provided by the second video source to peaking by the combination of the first and second peaking circuits.

In accordance with a further aspect of the invention the second luminance peaking circuit exhibits peaking in a frequency region higher than that characteristic of the first luminance peaking circuit.

The invention is illustrated in the accompanying drawing wherein like elements are denoted by like reference designators and in which:

FIGURE 1 is a block diagram of a television receiver embodying the invention;

FIGURE 2 is a spectrum diagram illustrating certain aspects of luminance signal processing in the receiver of FIGURE 1;

FIGURE 3 is a diagram illustrating certain aspects of chrominance signal processing in the receiver of FIGURE 1;

FIGURE 4 is a detailed block diagram of an auxiliary luminance peaking circuit used in the receiver of FIGURE 1;

FIGURE 5 is a detailed circuit diagram of the peaking circuit of FIGURE 4;

FIGURE 6 is a detailed block diagram of a chrominance signal de-peaking or pre-distortion circuit used in the receiver of FIGURE 1; and

FIGURE 7 is a detailed circuit diagram of the chrominance signal pre-distortion circuit of FIGURE 6.

The receiver of FIGURE 1 includes an RF and composite video input processor 10 having an antenna input terminal 12 for receiving a standard RF modulated video input signal S1 from sources such as an antenna or cable TV source or from TV accessories such as computers or television games. Signal S1 is applied to a tuner 14 which selects specific channels to be received. The tuner output signal S2 is applied to an intermediate frequency amplifier (IF) unit 16 which amplifies signal S2 and applies the amplified signal S3 to a sound trap 18. The sound trap 18 removes the sound carrier from signal S3 and provides the resultant video signal S4 to a video detector 20 which produces a baseband video output signal S5 which is of composite video form, that is, it comprises a baseband luminance component (Y) and a quadra-

ture modulated chrominance component (C). A video switch 22 selectively applies the composite video signal S5 or an auxiliary baseband composite video signal S6 to a luminance chrominance (Y-C) separation filter 24 (e.g., a comb filter). The auxiliary composite video signal S6 may be provided by an auxiliary input terminal 26 from a source such as a VCR, computer or other suitable device. Filter 24 separates the selected video input signal (S5 or S6) into its luminance (Y1) and chrominance (C1) components which are applied to respective output terminals 28 and 30 of input processor 10.

With the exception of video switch 22, the elements of processor 10 may all be of conventional design. Switch 22 is of unconventional design, however, in that it preferably includes a "null" or disabled condition in which neither of the composite video signals S5 and S6 are applied to Y-C separator filter 24. This feature prevents interference with wideband auxiliary video input signals Y2 and C2 when the wideband signals are selected for display as will be explained.

One may select various alternatives for video switch 22 for disabling or interrupting output signals Y1 and C1 from processor 10. As a first example, one may interpose a switch between the output of switch 22 and the input of filter 24 for interrupting or disabling the switch 22 output signal S7. As another example, switches may be interposed between the outputs of filter 24 and output terminals 28 and 30 of prcessor 10. Still another alternative would be to interpose switches in the conductors carrying the composite video signals S5 and S6. In any case, what is of importance to the present invention is that suitable means be provided for disabling the luminance Y1 and chrominance C1 signals produced by input processor 10 when it is desired to display a wideband video input signal S8 of the separated Y-C format.

The selected luminance (Y1) and chrominance (C1) output signals of input processor 10 at output terminals 28 and 30 are coupled to respective inputs 32 and 34 of a display processor 40 by means of respective conductors 36 and 38. Processor 40 is of conventional design and includes a luminance-chrominance (Y-C) processing unit 42 having an output 44 coupled to supply a processed video signal S9 to a display 46 (e.g., a kinescope). The luminance input terminal 32 is coupled to a luminance input (48) of processor 42 via a luminance signal delay and equalization circuit 50 and a luminance signal peaking circuit 52. A sharpness control 54 is coupled to luminance peaking circuit 52 for controlling the luminance signal peaking amplitude. The chrominance signal input 34 of processor 40 is coupled to the chrominance signal input 56 of Y-C processor 42 via a chrominance signal peaking circuit 58. Processing unit 42 is of conventional design and includes, illustratively, a chrominance signal demodulator (for demodulating the chrominance signal provided by peaking circuit 58), hue and saturation controls and a suitable matrix circuit for combining the luminance input signal with the demodulated color difference components (e.g., R-Y, B-Y) to provide an output color signal S9 in a form (e.g., RGB) suitable for display by display 46.

The remaining elements of FIGURE 1 facilitate the display of an auxiliary video input signal S8 of the recently proposed Y-C format in which the luminance Y2 and chrominance C2 components thereof are provided in separate form to the receiver and in which the luminance component Y2 exhibits a relatively wide bandwidth (e.g., 5MHz or so) as compared with broadcast standard video signals. As previously explained, this new wideband Y-C video signal format provides improved resolution (about 400 horizontal lines). Also, since the components Y2 and C2 are of separated form (rather than composite form) undesirable effects such as cross-color and cross-luma are eliminated. It is herein recognized as being desirable to be able to display the Y-C format video signal S8 without requiring extensive modifications to the receiver and to avoid unnecessary duplication of existing receiver circuits.

In detail, the wideband Y-C format video input signal S8 is applied to a Y-C format video input connector 60 having a first terminal 62 to which the luminance component Y2 of signal S8 is applied and a second terminal 64 to which the chrominance component of signal S8 is applied. The luminance component Y2 at terminal 62 is coupled to the input of luminance peaking circuit 52 in processor 40 by means of a circuit path which includes an auxiliary luminance peaking circuit 70. Specifically, the auxiliary peaking circuit 70 is connected at its input 72 to terminal 62 of connector 60 and at its output terminal 74 to conductor 36 at circuit node 76. By this means the wideband luminance signal Y2 is subjected to peaking by the combination of peaking circuits 52 and 70. The conventional peaking circuit 52 applies peaking over a lower portion of the bandwidth of signal Y2 and peaking circuit 70 applies supplementory peaking to an upper portion of the bandwidth of signal Y2. Accordingly, the wideband luma signal Y2 receives peaking over essentially its full bandwidth without requiring a separate full bandwidth peaking circuit in the receiver.

Advantageously, this feature of the invention avoids costly and complex circuit duplication in the receiver because peaking circuit 70 only needs to supplement the peaking provided by the conventional receiver peaking circuit 52. FIGURE 2 illustrates the effect of this feature. Response curve 202 (solid line) illustrates the amplitude response of the receiver when displaying the standard bandwidth video signal Y1. For this case maximum peaking occurs at a frequency of about 2.5 MHz and the upper band edge is around 4.0 MHz. Curve 204 illustrates the supplementary peaking provided by peaking circuit 70. As shown, about 3dB of peaking is added at a frequency

of about 4 MHz. The effect of doubly peaking the wideband luma signal Y2 is illustrated by the resultant curve 206 (dashed line). As shown, the Y2 signal response is extended to a frequency of about 5 MHz. Advantageously, a relatively small amount of additional peaking at the upper end of the peaking range of the conventional peaking circuit is needed to obtain full bandwidth peaking of the wideband luma signal Y2 and since the standard peaking circuit is used for both the standard bandwith signal Y1 and the wideband signal Y2 a desirable savings in peaking circuitry is achieved.

An advantage of applying the output of auxiliary peaking circuit 70 to node 76 rather than directly to peaking circuit 52 is that the doubly peaked luma signal Y2 is thereby also delayed by delay and equalization circuit 50. This delay (e.g., a few hundred nanoseconds) compensates for the difference in luminance and chrominance delays due to their different bandwidths so as to achieve proper luminance/chrominance registration on display 46. It has been found that the delay compensation for the standard bandwidth luma signal Y1 is adequate to achieve good registration of luminance and chrominance for the wideband signal and thus needless duplication of circuit elements is avoided by the connection to node 76 to facilitate the sharing of circuit 50.

The chrominance component C2 of Y-C format signal S8 is processed by coupling input terminal 64 to the input 82 of a chrominance signal pre-distortion or "de-peaking" circuit 80 having an output 84 coupled to a circuit node 86 on conductor 38. An important function of circuit 80 is to unbalance the relative amplitudes of the upper and lower sidebands of the chrominance signal C2. Specifically, the upper sideband is reduced relative to the lower sideband by suitable filtering. The amount of the reduction is selected to be complementary to the reduction of the lower sideband relative to the upper sideband which occurs in chroma peaking circuit 58 in display processor 40 so that after peaking in circuit 58 and de-peaking in circuit 80 the resultant C2 chroma signal at the input of Y-C processor 42 exhibits substantially equal amplitude sidebands. It is important that the chroma sidebands do not become unbalanced because as previously explained processor 42 demodulates them to baseband (R-Y, B-Y) for matrixing with the luma signal and these sideband amplitude errors will cause hue and saturation errors in the matrixed (RGB) output signal.

The foregoing is illustrated in FIGURE 3 in which curve 302 illustrates the chroma de-peaker 80 response, curve 304 illustrates the chroma peaker 58 response and curve 306 illustrates the combined resultant response. As shown, curve 302 peaks at about 700 KHz below the subcarrier frequency (3.58 MHz) and curve 304 peaks at about 700 KHz above the subcarrier frequency. The resultant response 306 peaks at the color subcarrier frequency and is symmetrical thereby ensuring that the relative amplitudes of the upper and lower sidebands of the quadrature modulated color subcarrier signal are not distorted.

It is instructive to note that one reason chroma peaking circuit 58 is present in processor 40 is to correct for sideband distortion of chroma signal C1 which occurs due to the limited IF bandwidth of the input processor 10 or the limited bandwidth of the source coupled to input 26. Since chroma signal C2 in the new Y-C signal format should have equal sidebands one might consider just skipping the peaking circuit 58 when displaying signal C2. This could be done, for example, by connecting chroma input terminal 64 directly to the chroma input 56 of processor 40 and thus eliminating the need for circuit 80. Such an approach would solve the sideband amplitude problem but could create another problem, namely, Y-C mis-registration. Recall that delay 50 corrects for Y-C delay differences due to the different bandwidths involved. For the embodiment of the invention shown, the relative Y-C delay for Y1 and C1 is about the same as for Y2 and C2. Accordingly, the same compensating delay is suitable for both signals. If, however, de-peaker 80 were eliminated and C2 were applied directly to input 56 of processor 42, the C2 delay will be different. This may be corrected, illustratively, by switching the luma signal delay or, alternatively, by adding delay to signal C2. Such complications may be completely avoided by passing both chroma signals through peaking circuit 58 and correcting the chroma signal C2 sideband amplitudes by de-peaking in circuit 80 as described.

Selection of signals for display is provided for by a user activated control unit 90 which has an output 92 coupled to a control input 23 of video switch 22 and another output 94 coupled to respective control inputs 88 and 78 of the chrominance and luminance circuits 80 and 70. To display the broadcast or cable antenna input signal S1, the user activates control 90 to send a disabling signal to the control inputs of circuits 80 and 70. This causes these units to open respective series connected output switches thus disconnecting them from conductors 36 and 38. At the same time unit 92 sends an enabling signal to switch 22 for selecting signal S5. This action is the same when auxiliary composite video signal S6 is selected for display except that switch 22 selects signal S6 rather than S5. When displaying the wideband Y-C format signal S8 for display, control unit 90 sends a disabling signal to switch 22 so that neither S5 nor S6 is selected. Simultaneously, an enabling signal is produced at output 94 of unit 90 thereby enabling the internal series switches in circuits 70 and 80 to couple the processed Y2 and C2 signals to conductors 36 and 38 for display by display unit 46.

FIGURE 4 is a detailed block diagram of a preferred embodiment of auxiliary luminance peaking circuit 70 illustrating further features of luminance sig-

nal processing. The input terminal 72 is coupled to the output terminal 74 via a cascade connection, in the order named, of a termination network 71, an AC coupling network 73, a peaking filter 75 and a switched amplifier 77 to which there is also connected a supply input terminal 79 and the control input terminal 78. FIGURE 5 is exemplary of a specific circuit implementation of FIGURE 4 and includes exemplary circuit values.

The termination network 71 of FIGURE 4 serves to terminate the luma input cable for signal Y2 in its characteristic impedance to thereby prevent cable reflections which would otherwise appear as double images or "ghosts" when Y2 is displayed. In FIGURE 5 this function is provided by resistor RT coupled between input 72 and ground.

The AC coupling network 73 it will be noted is placed before the peaking filter 75 in the cascade connection (71-73-75-77). Advantageously, this prevents the low impedance terminating resistor (75 Ohms) and any DC component if signal Y2 from upsetting the DC bias of amplifier 77 since, as will be explained, peaking filter 75 forms part of the bias network for amplifier 77 thus advantageously reducing the number of components needed to implement the amplifier. Network 73 is implemented, in the example of FIGURE 5, by a series coupled capacitor (33 micro-Farads).

The peaking filter 75, as shown and described in connection with FIGURE 2, provides a small boost of about 3 dB near the upper end of the video band (around 4 MHz). Any suitable filter may be used for this purpose but the preferred example of FIGURE 5 provides a DC path to ground through a resistor R2 and thus is useful in establishing bias for amplifier 77. Specifically, in FIGURE 5 filter 75 comprises an input series resistor R1 coupled by a parallel resonant (L-C) circuit and a shunt resistor R2 to ground. The values of the input series resistor R1 and the shunt resistor R2 are the main factors that determine the signal change. At frequencies far below or above resonance, the filter attentuation is approximately R2/(R1 + R2) or about 3 dB and at resonance it is about zero dB as shown in FIGURE 2.

Advantageously, bias voltage for amplifier 77 is developed in filter 75 by passing a current through the filter inductor and resistor R2. This current is provided by resistor R3 connected to supply terminal 79. The bias so developed is coupled via resistor R4 to amplifier transistor Q1 having collector and emitter resistors (R5 and R6) coupled respectively to supply terminal 79 and ground. The gain of the amplifier is primarily determined by the ratio of resistor R6 and R5 and for the values shown is about times three or 10 dB. Thus, the overall gain change of peaking circuit 70 varies from a minimum of +7 dB to a maximum of +10 dB over the luminance frequency range.

Output signals for amplifier 77 are provided by an emitter follower transistor Q2 connected at the base thereof to the collector of transistor Q1 and at the emitter and collector electrodes thereof to terminals 74 and 79. Switching of the output signal is provided by means of diode D1 connected at the anode and cathode thereof to the base of transistor Q2 and to control terminal 78. A high level voltage at terminal 78 reverse biases diode D1 whereby the amplifier is enabled and Y2 (peaked) is coupled to node 76 on conductor 36 for display by display 46. Conversely, a low level voltage on terminal 78 forward biases diode D1 thereby disabling emitter follower transistor Q2 and thus decoupling the luminance peaking filter 70 from conductor 36. In this mode, as previously explained, video switch 22 selects one of signals S5 or S6 for display by display 46 in processor 40.

FIGURE 6 is a detailed block diagram of a preferred embodiment of auxiliary chrominance pre-distortion or "de-peaking" circuit 80 illustrating further features of the chrominance signal processing of the receiver of FIGURE 1. The input terminal 82 is coupled to the output terminal 84 by a cascade connection, in the order named, of a termination network 81, a filter 83, an AC coupling network 85 and a switched amplifier 87 to which there is also connected a supply terminal 89 and the control input terminal 88. FIGURE 7 is exemplary of a specific circuit implementation of FIGURE 6 and includes exemplary circuit values.

The termination network 81 serves to terminate the chrominance signal input cable for signal C2 in its characteristic impedance to thereby prevent cable reflections which would otherwise appear as color distortions when C2 is displayed. In FIGURE 7 this function is provided by resistor R6 coupled between terminal 82 and ground.

The filter 83, as discussed with regard to FIGURE 3, distorts the relative amplitudes of the chroma signal sidebands by attenuating the upper sideband more than the lower sideband. The degree of attenuation, as shown in FIGURE 3, is complementary to the response of the peaking filter 58 so that the resultant sidebands are symmetrical as shown by curve 306. For this purpose, one could implement filter 83 with a low-pass or a bandpass filter. In order to provide a good match (i.e., complement) for the chrominance filter 58, it has been found advantageous to include resistors in filter 83 for controlling its response shape (slope) in the chrominance signal band (i.e., plus or minus about 700 KHz from the subcarrier frequency). To this end, the filter 83 includes a series branch comprising inductor L1 and shaping resistor R7 and a shunt branch including capacitor C'1 and shaping resistor R8. The inductor and capacitor considered alone provide a low-pass characteristic which, by itself, would exhibit a maximum slope of -12 dB/octove. This is modified by selective resistors R7 and R8 for filter 83 to match the slope of filter 58 in the region from about 2.8 MHz to about 4.2 MHz.

AC coupling in the chrominance filter 80 is done differently than in the luminance filter 70 in that it follows (rather than precedes) filter 83 in the cascade connection 81-83-85-87. In this case, however, the AC coupling (e.g., capacitor C'2) could be placed before the filter since there is no DC path to ground through the shunt path R8-C'1. However, if a filter is used for filter 83 which does have a shunt path to ground then one may wish to use this path for biasing amplifier 87 as was done with amplifier 77 in which case the AC coupling would be placed before filter 83.

Amplifier 87 is a switched amplifier which couples and decouples the pre-distorted chrominance signal C2 to conductor 38. As was the case with amplifier 77, the selective coupling could be provided by means of a series switch at the amplifier output. It is preferred, however, to use a switched amplifier to avoid increased output resistance which would result from using a series output switch. By this means, circuit output signal levels are little influenced by the impedance of the conductors 38 and 36 and associated elements connected to them. A specific example of amplifier 87 (FIGURE 7) includes a pair of resistors R9, R10 coupled between the output of the coupling capacitor and the supply terminal 89 and ground, respectively. The DC bias so developed and the chrominance signal are coupled via a resistor R11 to the base of an emitter follower transistor Q3 having collector and emitter electrodes connected to respective ones of supply and output terminals 89 and 84. Switching of amplifier 87 is provided by diode D2 connected at the anode and cathode thereof to the base of transistor Q3 and the control terminal 88, respectively. In operation a low level voltage at terminal 88 forward biases diode D2 thereby disabling transistor Q3 and isolating amplifier 87 from conductor 38. Conversely, a high level voltage at terminal 88 reverse biases diode D2 and enables transitor Q3 to supply the pre-distorted chrominance signal C2 to conductor 38.

The principles of luminance peaking and chrominance depeaking herein shown and described may be used either separately or in combination in a specific television receiver application. It has been previously explained in detail, for example, that the chrominance pre-distortion circuit 80 may be eliminated in a given receiver application by coupling C2 input 64 to the chrominance input 56 of display processor 40 by a switch thereby bypassing chroma peaking circuit 58. As explained, the changes in relative delays of the signals C2 and Y2 could be corrected by use of switchable delay circuits for luma signal Y2 or by adding delay in the C2 signal path. In certain applications it may be desired to display the signal Y2 without peaking or to provide a Y2 with a completely separate full bandwidth peaking circuit thus eliminating the need for circuit 70. For example, luminance peaking circuit 70 could be replaced with a switch for selecting Y2 and peaking circuit 52 could be disabled when displaying signal Y2. This would provide "flat" (unpeaked) luminance response but the benefits of chroma de-peaking would still be obtained since it facilitates proper Y2-C2 registration as previously explained. Yet another alternative would be to replace circuit 70 with a full bandwidth peaker and switch and to disable peaker 52 when displaying Y2 thereby giving independent peaking control of Y1 and Y2. Again, the Y2-C2 registration advantages are still obtained in this example of dispensing with circuit 70. The advantages of employing the combination of luminance supplementary peaking (70) and chrominance predistortion (80) have been previously discussed.

Claims

1. Television apparatus comprising:

   a first luminance signal source comprising a source of composite video signals inclusive of luminance and chrominance signal components, and means for separating said luminance signal component from said composite video signals;

   a second luminance signal source providing a luminance signal exhibiting a bandwidth wider than the bandwidth of said separated luminance signal component provided by said first source;

   a display processor having a luminance input coupled to said first luminance signal source via a first luminance peaking circuit and coupled to said second luminance signal source via a circuit path; characterized in that:

   said second luminance signal source (62) is coupled via said circuit path to an input of said first luminance peaking circuit (52) to which said first luminance signal source (10) is coupled; and

   said circuit path includes a second luminance peaking circuit (70) for subjecting a luminance signal provided by said second luminance signal source (62) to peaking by the combination of said first (52) and second(70) peaking circuits, wherein said second luminance peaking circuit (70) exhibits peaking in a frequency region higher (204) than that (202) of said first luminance peaking circuit (52).

2. Apparatus as recited in Claim 1 wherein:

   said circuit path includes a switch (77) serially coupled in said path between said second luminance peaking circuit (70) and said input of said first luminance peaking circuit (52).

3. Apparatus as recited in Claim 1 wherein said second luminance peaking circuit (70) is AC coupled (73) to said second luminance signal source (62) and DC coupled to said input of said first lumi-

AC coupling in the chrominance filter 80 is done differently than in the luminance filter 70 in that it follows (rather than precedes) filter 83 in the cascade connection 81-83-85-87. In this case, however, the AC coupling (e.g., capacitor C'2) could be placed before the filter since there is no DC path to ground through the shunt path R8-C'1. However, if a filter is used for filter 83 which does have a shunt path to ground then one may wish to use this path for biasing amplifier 87 as was done with amplifier 77 in which case the AC coupling would be placed before filter 83.

Amplifier 87 is a switched amplifier which couples and decouples the pre-distorted chrominance signal C2 to conductor 38. As was the case with amplifier 77, the selective coupling could be provided by means of a series switch at the amplifier output. It is preferred, however, to use a switched amplifier to avoid increased output resistance which would result from using a series output switch. By this means, circuit output signal levels are little influenced by the impedance of the conductors 38 and 36 and associated elements connected to them. A specific example of amplifier 87 (FIGURE 7) includes a pair of resistors R9, R10 coupled between the output of the coupling capacitor and the supply terminal 89 and ground, respectively. The DC bias so developed and the chrominance signal are coupled via a resistor R11 to the base of an emitter follower transistor Q3 having collector and emitter electrodes connected to respective ones of supply and output terminals 89 and 84. Switching of amplifier 87 is provided by diode D2 connected at the anode and cathode thereof to the base of transistor Q3 and the control terminal 88, respectively. In operation a low level voltage at terminal 88 forward biases diode D2 thereby disabling transistor Q3 and isolating amplifier 87 from conductor 38. Conversely, a high level voltage at terminal 88 reverse biases diode D2 and enables transitor Q3 to supply the pre-distorted chrominance signal C2 to conductor 38.

The principles of luminance peaking and chrominance depeaking herein shown and described may be used either separately or in combination in a specific television receiver application. It has been previously explained in detail, for example, that the chrominance pre-distortion circuit 80 may be eliminated in a given receiver application by coupling C2 input 64 to the chrominance input 56 of display processor 40 by a switch thereby bypassing chroma peaking circuit 58. As explained, the changes in relative delays of the signals C2 and Y2 could be corrected by use of switchable delay circuits for luma signal Y2 or by adding delay in the C2 signal path. In certain applications it may be desired to display the signal Y2 without peaking or to provide a Y2 with a completely separate full bandwidth peaking circuit thus eliminating the need for circuit 70. For example, luminance peaking circuit 70 could be replaced with a switch for selecting Y2 and peaking circuit 52 could be disabled when displaying signal Y2. This would provide "flat" (unpeaked) luminance response but the benefits of chroma de-peaking would still be obtained since it facilitates proper Y2-C2 registration as previously explained. Yet another alternative would be to replace circuit 70 with a full bandwidth peaker and switch and to disable peaker 52 when displaying Y2 thereby giving independent peaking control of Y1 and Y2. Again, the Y2-C2 registration advantages are still obtained in this example of dispensing with circuit 70. The advantages of employing the combination of luminance supplementary peaking (70) and chrominance predistortion (80) have been previously discussed.

Claims

1. Television apparatus comprising:

   a first luminance signal source comprising a source of composite video signals inclusive of luminance and chrominance signal components, and means for separating said luminance signal component from said composite video signals;

   a second luminance signal source providing a luminance signal exhibiting a bandwidth wider than the bandwidth of said separated luminance signal component provided by said first source;

   a display processor having a luminance input coupled to said first luminance signal source via a first luminance peaking circuit and coupled to said second luminance signal source via a circuit path; characterized in that:

   said second luminance signal source (62) is coupled via said circuit path to an input of said first luminance peaking circuit (52) to which said first luminance signal source (10) is coupled; and

   said circuit path includes a second luminance peaking circuit (70) for subjecting a luminance signal provided by said second luminance signal source (62) to peaking by the combination of said first (52) and second(70) peaking circuits, wherein said second luminance peaking circuit (70) exhibits peaking in a frequency region higher (204) than that (202) of said first luminance peaking circuit (52).

2. Apparatus as recited in Claim 1 wherein:

   said circuit path includes a switch (77) serially coupled in said path between said second luminance peaking circuit (70) and said input of said first luminance peaking circuit (52).

3. Apparatus as recited in Claim 1 wherein said second luminance peaking circuit (70) is AC coupled (73) to said second luminance signal source (62) and DC coupled to said input of said first lumi-

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nance peaking circuit (52).

4. Apparatus as recited in Claim 1 wherein
said first luminance signal source (10) includes an input switch (22) for selectively enabling and disabling said first luminance signal; and
said circuit path includes a switch (77) interposed between said second luminance peaking circuit (70) and said input of said first luminance peaking circuit (52) for selectively enabling and disabling said second luminance signal.

5. Apparatus as recited in Claim 1 further comprising:
a delay circuit (50) having an input coupled to said first source (10) and to said second source (62) and having an output coupled to said input of said first luminance peaking circuit (52) for imparting equal delays to luminance signals provided by said sources.

Patentansprüche

1. Fernsehgerät, enthaltend:
- eine erste Luminanzsignal-Quelle, enthaltend eine Quelle eines Composit-Videosignals mit Luminanz- und Chrominanz-Signalkomponenten und ein Mittel zum Trennen der Luminanzsignal-Komponente von den Composit-Videosignalen;
- eine zweite Luminanzsignal-Quelle, die ein Luminanzsignal bereitstellt, das eine größere Bandbreite zeigt als die Bandbreite der abgetrennten Luminanzsignal-Komponente, die von der ersten Quelle zur Verfügung gestellt wird;
- ein Darstellungsprozessor mit einem Luminanz-Eingang, der mit der ersten Luminanzsignal-Quelle über eine erste Luminanz-Anhebungsschaltung gekoppelt ist und mit der zweiten Luminanzsignal-Quelle über einen Schaltungspfad gekoppelt ist;
dadurch gekennzeichnet, daß
- die zweite Luminanzsignal-Quelle (62) über den Schaltungspfad mit einem Eingang der ersten Luminanz-Anhebungsschaltung (52) gekoppelt ist, an die die erste Luminanzsignal-Quelle (10) gekoppelt ist; und
- der Schaltungspfad eine zweite Luminanz-Anhebungsschaltung (70) beinhaltet zum Anheben oder Verändern eines Luminanzsignals, das von der zweiten Luminanzsignal-Quelle (62) zugeführt wird, durch die Kombination der ersten (52) und zweiten (70) Anhebungsschaltung ("peaking circuits"), wobei die zweite Luminanz-Anhebungsschaltung (70) eine Anhebung in einer Frequenzregion zeigt, die höher (204) als die (202) der ersten Luminanz-Anhebungsschaltung (52) ist.

2. Gerät nach Anspruch 1, bei dem
- der Schaltungspfad einen Schalter (77) beinhaltet, der seriell in den Pfad zwischen der zweiten Luminanz-Anhebungsschaltung (70) und den Eingang der ersten Luminanz-Anhebungsschaltung (52) gekoppelt ist.

3. Gerät nach Anspruch 1, bei dem
- die zweite Luminanz-Anhebungsschaltung (70) mit der zweiten Luminanzsignal-Quelle (62) AC-gekoppelt (73) und mit dem Eingang der ersten Luminanz-Anhebungsschaltung (52) DC-gekoppelt ist.

4. Gerät nach Anspruch 1, bei dem
- die erste Luminanzsignal-Quelle (10) einen Eingangsschalter (22) zum wahlweisen Aktivieren und Deaktivieren (Einschalten oder Sperren) des ersten Luminanzsignals beinhaltet; und
- der Schaltungspfad einen Schalter (77) beinhaltet, der zwischen die zweite Luminanz-Anhebungsschaltung (70) und den Eingang der ersten Luminanz-Anhebungsschaltung (52) zum selektiven Freigeben und Sperren des zweiten Luminanzsignals eingefügt ist.

5. Gerät nach Anspruch 1, weiter enthaltend
- eine Verzögerungsschaltung (50) mit einem Eingang, der mit der ersten Quelle (10) und der zweiten Quelle (62) gekoppelt ist, und mit einem Ausgang, der mit dem Eingang der ersten Luminanz-Anhebungsschaltung (52) gekoppelt ist, zum Einbringen gleicher Verzögerungen für die Luminanzsignale, die von den Quellen bereitgestellt werden.

Revendications

1. Appareil de télévision comprenant :
une première source de signal de luminance comprenant une source de signaux vidéo composites incluant les composantes des signaux de luminance et de chrominance et des moyens pour séparer ladite composante de signal de luminance desdits signaux vidéo composites;
une seconde source de signal de luminance fournissant un signal de luminance présentant une largeur de bande plus étendue que la largeur de bande de ladite composante de signal de lu-

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minance séparée fourni par ladite première source ;

un processeur d'affichage possédant une entrée de luminance couplée à ladite première source de signal de luminance par l'intermédiaire d'un premier circuit de correction de luminance et couplé à ladite seconde source de signal de luminance par l'intermédiaire d'une branche de circuit, caractérisé en ce que :

ladite seconde source de signal de luminance (62) est couplée par l'intermédiaire de ladite branche de circuit à une entrée dudit premier circuit de correction de luminance (52) auquel ladite source de signal de luminance (10) est couplée ; et

ladite branche de circuit comprend un second circuit de correction de luminance (70) pour soumettre un signal de luminance fourni par ladite seconde source de signal de luminance (62) à une correction en combinant lesdits premier (52) et second (70) circuits de correction, dans lequel ledit second circuit de correction de luminance (70) présente une correction dans une zone de fréquence plus élevée (204) que celle (202) dudit premier circuit de correction de luminance (52).

2. Appareil selon la revendication 1 dans lequel :

ladite branche de circuit comprend un commutateur (77) couplé en série dans ladite branche entre ledit second circuit de correction de luminance (70) et ladite entrée dudit premier circuit de correction de luminance (52).

3. Appareil selon la revendication 1 dans lequel ledit second circuit de correction de luminance (70) présente un couplage alternatif (73) avec ladite seconde source de signal de luminance (62) et un couplage continu avec ladite entrée dudit premier circuit de correction de luminance (52).

4. Appareil selon la revendication 1 dans lequel :

ladite première source de signal de luminance (10) comprend un commutateur d'entrée (22) pour valider et invalider de façon sélective ledit premier signal de luminance ; et

ladite branche de circuit comprend un commutateur (77) interposé entre ledit second circuit de correction de luminance (70) et ladite entrée dudit premier de correction de luminance (52) pour valider et invalider de façon sélective ledit second signal de luminance .

5. Appareil selon la revendication 1 comprenant de plus :

un circuit à retard (50) possédant une entrée couplée à ladite première source (10) et à ladite seconde source (62) et possédant une sortie couplée à ladite entrée dudit premier circuit de correction de luminance (52) pour communiquer des retards égaux aux signaux de luminance fournis par ladite source.