CLAIMS

What is claimed is:

1. An apparatus for evaluating communication signals, comprising:

a detector circuit to receive a time-varying differential communication signal, and including switched capacitors and an inverter to provide an indication of whether a level of the received communication signal is above or below a threshold value.

2. The apparatus of claim 1, wherein the time-varying differential communication signal comprises a first signal and a second signal, and wherein a peak-to-peak amplitude difference between the first and second signals provides the level of the communication signal that is compared with the threshold value.

3. The apparatus of claim 1, wherein the capacitors comprises a first capacitor coupled to receive the communication signal and a second capacitor coupled to the inverter, the detector circuit further including:

a first set of switches, responsive to a first phase of a clock, to close to enable the first capacitor to store a voltage corresponding to the level of the communication signal and to enable the second capacitor to store a voltage corresponding to a difference between the threshold value and a trip level of the inverter; and

a second set of switches, responsive to a second phase of the clock and that is an inverse to the first phase, to close to couple the first capacitor to the second capacitor to enable a difference between the stored voltages to be provided to the inverter,

wherein the first set of switches is closed while the second set of switches is open and vice versa.

4. The apparatus of claim 3, wherein the inverter is coupled to provide an output signal having a first state if the level of the communication

signal is greater than the threshold value to indicate activity on a communication channel that carries the communication signal, and

wherein the inverter is coupled to provide the output signal having a second state, opposite to the first state, if the level of the communication signal is less than the threshold value to indicate insufficient activity on the communication channel.

5. The apparatus of claim 3 or 4, wherein the first capacitor has a larger capacitance than a capacitance of the second capacitor.

6. The apparatus of claim 5, wherein the capacitance of the first capacitor is five times or more greater than the capacitance of the second capacitor.

7. The apparatus of claim 3, wherein the first set of switches comprises:

a first switch coupled between a first terminal of the first capacitor and a first pad that receives the first signal;

a second switch coupled between a second terminal of the first capacitor and a second pad that receives the second signal;

a third switch coupled between a first terminal of the second capacitor and a third pad that receives a voltage having the threshold value; and

a fourth switch coupled between an output terminal of the inverter and a second terminal of the second capacitor at an input terminal of the inverter.

8. The apparatus of claim 7, wherein the second set of switches comprises:

a fifth switch coupled between ground and the first terminal of the first capacitor; and

a sixth switch coupled between the second terminal of the first capacitor and the first terminal of the second capacitor.

9. The apparatus of any of claims 3-4 and claims 7-8, further comprising at least another inverter, coupled to the inverter, to provide an inverted version of an output of the detector circuit and to increase a gain of the detector circuit.

10. The apparatus of claim 9, further comprising a latch circuit coupled to the inverter.

11. The apparatus of any of claims 1-4 and claims 7-8, further comprising a clock circuit, coupled to the detector circuit, to receive input quadrature signals and to generate the clock signal to have a frequency that is at least double a frequency of each of the quadrature signals.

12. A method for evaluating communication signals, comprising:

receiving, by a detector, a time-varying differential communication signal;

operating a first set of switches, in response to a first phase of a clock signal, to store in a first capacitor a first voltage level corresponding to the communication signal and to store in a second capacitor a second voltage level corresponding to a threshold level;

operating a second set of switches, in response to a second phase of the clock signal, to provide to an inverter a third voltage level corresponding to a difference between the stored first and voltage levels; and

generating, by the inverter in response to the provided third voltage level, an output signal to indicate whether an amplitude level the communication signal exceeds the threshold level.

13. The method of claim 12, wherein the generating the output signal by the inverter in response to the provided third voltage level comprises:

determining whether the provided third voltage level is greater than a trip level of the inverter;

if the third voltage level is determined to be greater than the trip level, generating the output signal to have a first state to indicate that the amplitude level of the communication signal exceeds the threshold level; and

if the third voltage level is determined to be less than the trip level, generating the output signal to have a second state, opposite from the first state, to indicate that the amplitude level of the communication signal is below the threshold level.

14. The method of claim 13, further comprising powering down a component of a computer system in response to the output signal having the second state.

15. The method of claim 12, further comprising:

receiving input quadrature signals each having an operating frequency; and

generating, from the received quadrature signals, the clock signal to have a clock frequency of at least twice the operating frequency.

16. The method of claim 12, wherein:

the time-varying differential communication signal comprises a first signal and a second signal;

the operating the first set of switches to store the first voltage level corresponding to the communication signal comprises operating the first set of switches to store in the first capacitor a peak-to-peak amplitude difference between the first and second signals; and

the operating the first set of switches to store the second voltage level corresponding to the threshold level comprises operating the first set of switches to store in the second capacitor a voltage corresponding to a difference between the threshold level and a trip level of the inverter.

17. The method of any one of claims 12-16, wherein the first and second phases of the clock signal have opposite polarities to enable the first

set of switches to be closed while the second set of switches are open and vice versa.

18. A system for evaluating communication signals, comprising:

a communication interface to support a communication channel that carries a time-varying differential communication signal;

an inverter-and-switched-capacitor-based detector circuit, coupled to the communication interface, to detect activity by the communication signal in the communication channel and to generate an output signal to indicate whether the activity is detected; and

a component, coupled to the detector, to receive the generated output signal and to power down at least a portion of the communication interface if the output signal indicates insufficient activity by the communication signal in the communication channel.

19. The system of claim 18, wherein the component comprises a processor.

20. The system of claim 18 or 19, wherein the detector circuit comprises:

an inverter to provide the output signal and having a trip level;

a first capacitor coupled to receive the communication signal and a second capacitor coupled to the inverter;

a first set of switches, responsive to a first phase of a clock, to close to enable the first capacitor to store a voltage corresponding to a level of the communication signal and to enable the second capacitor to store a voltage corresponding to a difference between a threshold value and the trip level of the inverter; and

a second set of switches, responsive to a second phase of the clock and that is an inverse to the first phase, to close to couple the first capacitor to the second capacitor to enable a difference between the stored voltages to be provided to the inverter,

wherein the output signal indicates that there is activity the communication signal in the communication channel if the difference between the stored voltages provided to the inverter is above the trip level of the inverter.

21. The system of claim 20, further comprising a clock circuit, coupled to the detector circuit, to receive input quadrature signals and to generate the clock signal to have a frequency that is at least double a frequency of each of the quadrature signals.

CLAIMS

What is claimed is:

1. An apparatus, comprising:
a detector circuit to receive a time-varying differential communication signal, and including switched capacitors and an inverter to provide an indication of whether a level of the received communication signal is above or below a threshold value,

wherein the capacitors comprises a first capacitor coupled to receive the communication signal and a second capacitor coupled to the inverter, the detector circuit further including:

a first set of switches, responsive to a first phase of a clock, to enable the first capacitor to store a voltage corresponding to the level of the communication signal and to enable the second capacitor to store a voltage corresponding to a difference between the threshold value and a trip level of the inverter; and

a second set of switches, responsive to a second phase of the clock and that is an inverse to the first phase, to couple the first capacitor to the second capacitor to enable a difference between the stored voltages to be provided to the inverter,

wherein the first set of switches is closed while the second set of switches is open and vice versa.

2. The apparatus of claim 1, wherein the time-varying differential communication signal comprises a first signal and a second signal, and wherein a peak-to-peak amplitude difference between the first and second signals provides the level of the communication signal that is compared with the threshold value.

3. The apparatus of claim 1, wherein the inverter is coupled to provide an output signal having a first state if the level of the communication signal is greater than the threshold value to indicate activity on a communication channel that carries the communication signal, and

wherein the inverter is coupled to provide the output signal having a second state, opposite to the first state, if the level of the communication signal is less than the threshold value to indicate insufficient activity on the communication channel.

4. The apparatus of claim 1, wherein the first capacitor has a larger capacitance than a capacitance of the second capacitor.

5. The apparatus of claim 4, wherein the capacitance of the first capacitor is five times or more greater than the capacitance of the second capacitor.

6. The apparatus of claim 1, wherein the first set of switches comprises
a first switch coupled between a first terminal of the first capacitor and a first pad that receives the first signal;

a second switch coupled between a second terminal of the first capacitor and a second pad that receives the second signal;

a third switch coupled between a first terminal of the second capacitor and a third pad that receives a voltage having the threshold value; and

a fourth switch coupled between an output terminal of the inverter and a second terminal of the second capacitor at an input terminal of the inverter.

7. The apparatus of claim 6, wherein the second set of switches comprises
a fifth switch coupled between ground and the first terminal of the first capacitor; and

a sixth switch coupled between the second terminal of the first capacitor and the first terminal of the second capacitor.

8. The apparatus of claim 1, further comprising:
at least another inverter, coupled to the inverter, to provide an inverted version of an output of the detector circuit and to increase a gain of the detector circuit.

9. The apparatus of claim 8, further comprising:
a latch circuit coupled to the inverter.

10. An apparatus comprising:
a detector circuit to receive a time-varying differential communication signal, and including switched capacitors and an inverter to provide an indication of whether a level of the received communication signal is above or below a threshold value; and

a clock circuit, coupled to the detector circuit, to receive input quadrature signals and to generate the clock signal to have a frequency that is at least double a frequency of each of the quadrature signals.

11. A method, comprising:
receiving, by a detector, a time-varying differential communication signal;

operating a first set of switches, in response to a first phase of a clock signal, to store in a first capacitor a first voltage level corresponding to the communication signal and to store in a second capacitor a second voltage level corresponding to a threshold level;

operating a second set of switches, in response to a second phase of the clock signal, to provide to an inverter a third voltage level corresponding to a difference between the stored first and voltage levels; and

generating, by the inverter in response to the provided third voltage level, an output signal to indicate whether an amplitude level the communication signal exceeds the threshold level.

12. The method of claim 11, wherein the generating the output signal by the inverter in response to the provided third voltage level comprises
determining whether the provided third voltage level is greater than a trip level of the inverter;

if the third voltage level is determined to be greater than the trip level, generating the output signal to have a first state to indicate that the amplitude level of the communication signal exceeds the threshold level; and

if the third voltage level is determined to be less than the trip level, generating the output signal to have a second state, opposite from the first state, to indicate that the amplitude level of the communication signal is below the threshold level.

13. The method of claim 12, further comprising:
powering down a component of a computer system in response to the output signal having the second state.

14. The method of claim 11, further comprising:
receiving input quadrature signals each having an operating frequency; and

generating, from the received quadrature signals, the clock signal to have a clock frequency of at least twice the operating frequency.

15. The method of claim 11, wherein the time-varying differential communication signal comprises a first signal and a second signal;
the operating the first set of switches to store the first voltage level corresponding to the communication signal comprises operating the first set of switches to store in the first capacitor a peak-to-peak amplitude difference between the first and second signals; and

the operating the first set of switches to store the second voltage level corresponding to the threshold level comprises operating the first set of switches to store in the second capacitor a voltage corresponding to a difference between the threshold level and a trip level of the inverter.

16. The method of claim 11, wherein the first and second phases of the clock signal have opposite polarities to enable the first set of switches to be closed while the second set of switches are open and vice versa.

17. A system, comprising:
a communication interface to support a communication channel that carries a time-varying differential communication signal;

an inverter-and-switched-capacitor-based detector circuit, coupled to the communication interface, to detect activity by the communication signal in the communication channel and to generate an output signal to indicate whether the activity is detected; and

a component, coupled to the detector, to receive the generated output signal and to power down at least a portion of the communication interface if the output signal indicates insufficient activity by the communication signal in the communication channel,

wherein the detector circuit comprises an inverter to provide the output signal and having a trip level;

a first capacitor coupled to receive the communication signal and a second capacitor coupled to the inverter;

a first set of switches, responsive to a first phase of a clock, to enable the first capacitor to store a voltage corresponding to a level of the communication signal and to enable the second capacitor to store a voltage corresponding to a difference between a threshold value and the trip level of the inverter; and

a second set of switches, responsive to a second phase of the clock and that is an inverse to the first phase, to couple the first capacitor to the second capacitor to enable a difference between the stored voltages to be provided to the inverter,

wherein the output signal indicates that there is activity the communication signal in the communication channel if the difference between the stored voltages provided to the inverter is above the trip level of the inverter.

18. The system of claim 17, wherein the component comprises a processor.

19. The system of claim 17, further comprising:
a clock circuit, coupled to the detector circuit, to receive input quadrature signals and to generate the clock signal to have a frequency that is at least double a frequency of each of the quadrature signals.