

BT CASE NO:23448

WP NO: 0648P

SEMICONDUCTOR STRUCTURES AND A METHOD OF
MANUFACTURING SEMICONDUCTOR STRUCTURES

The present invention relates to semiconductor structures. It finds particular application in the field of opto-electronic devices such as semiconductor lasers, and their manufacture.

A known family of opto-electronic devices, buried heterostructure (BH) semiconductor lasers, is based on the following general structure : a substrate of semiconductor material having a mesa thereon, with confinement layers on either side of the mesa. Such a device is described by O Mikami et al in "1.5 μ m GaInAsP/InP Buried Heterostructure Lasers Fabricated by Hybrid Combination of Liquid - and Vapour-Phase Epitaxy", Electronics Letters, 18 (5) (4.3.82) pages 237-239. (The word "mesa" in this context is used to describe an upstanding stripe having a flat top.)

The devices of the family include a planar p-n junction across which current flows (the conventional current from p to n) and a waveguide region adjacent to the junction to which light is confined. The waveguide region may comprise an "active layer" in which electrons and holes combine with the production of photons by radiative recombination. Such an active layer has to relate suitably in band gap and refractive index to the other semiconductor regions of the structure in order to achieve a suitable degree of "confinement" of these processes to the active layer. The layers of material to either side of the waveguide region and in contact with

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the opposite faces of the waveguide region are known as "confinement layers".

5 A major field of application of semiconductor optical devices is in optical fibre communications systems. In general, the devices are constructed out of materials whose elemental components are selected from Groups III and V of the Periodic Table. Silica optical fibres as produced in recent years have loss minima at 1.3 μm and 1.55 μm approximately, the latter minimum being the lower. Accordingly, there is an especial need for devices 10 operating in the range from 1.1 to 1.65 μm , especially from 1.3 to 1.6 μm . (These wavelengths, like all the wavelengths herein except where the context indicates otherwise, are in vacuo wavelengths). Semiconductor 15 lasers operating in this region of the infrared usually comprise regions of indium phosphide, InP, and of quaternary materials indium gallium arsenide phosphides, $\text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$. By suitable choices of x and y it is possible to lattice-match the various regions while 20 varying the band gaps of the materials. (Band gaps can be determined experimentally by, for example, photoluminescence). Additionally, both indium phosphide and the quaternary materials can be doped to be p - or n-type as desired.

25 Describing a selected BH semiconductor laser, with its mesa uppermost, it has an active layer within the mesa. Electrical contacts are provided to the mesa and on the furthestmost face of the substrate from the mesa. The "confinement" required is provided optically in a vertical 30 direction, by changes in refractive index of the



semiconductor material, and both optically and electrically in a horizontal direction by the confinement layers. The confinement layers act to cause any current flowing between the contacts to flow preferentially through the mesa and therefore through the active layer. In one form, the confinement layers may present non-conducting semiconductor junctions to current flow between the contacts in use of the device.

Good electrical confinement is provided if the semiconductor layers between the contacts constitute a p-n junction and the confinement layers in combination with the substrate constitute an n-p-n junction when taken in the same direction. In use the confinement layers and substrate then comprise a reverse biased semiconductor junction in both directions. Alternatively the confinement layers and substrate could present multiple reverse biased semiconductor junctions in one or both directions.

In another form, the confinement layers may comprise "semi-insulating" materials such as Fe doped InP. These materials have a relatively high resistivity compared to for instance undoped InP. Confinement layers in this form have advantages in that they substantially completely oppose current flow and show low capacitance effects. Low capacitance effects tend to increase device speed.

In the past devices of this type have been fabricated by means of liquid phase epitaxy (LPE). However there are problems associated with these techniques such as solutal convection within the melts, inaccurate thickness control of the confinement layers and meltback of the mesas during fabrication. These have lead in particular to lack of uniformity over large areas and the techniques do not lend themselves easily to large scale production.



In an attempt to solve the problem of meltback of the mesas during fabrication an LPE-VPE (vapour phase epitaxy) hybrid technique has been used. However there are still disadvantages. It retains an LPE growth step and therefore does not lend itself to large scale production, a significant leakage current has been observed in the confinement layers, and narrow mesas are difficult or impossible to achieve.

An alternative growth technique, metal organic vapour phase epitaxy (MOVPE), has been found promising for large scale device production. It offers a highly desirable combination of features : atomic scale interface abruptness, precise compositional control, and uniformity of thickness and composition over a large area.

Additional alternative growth techniques which have also been found advantageous in epitaxial fabrication processes are molecular beam epitaxy (MBE) and metal organic molecular beam epitaxy (MOMBE).

A method of fabricating buried mesa structure lasers using only low pressure "metalorganic chemical vapour deposition" (LP-MOCVD) epitaxial growth steps is outlined in the following paper : "Very Low Threshold Buried Ridge Structure Lasers Emitting at 1.3 μ m Grown by Low Pressure Metalorganic Chemical Vapour Deposition" by M Razeghi et al, Applied Physics Letters, 46 (2) (15.1.85) pages 131-133. (MOCVD is an alternative term for MOVPE.) The method comprises the steps of growing onto an InP substrate, an n-doped InP buffer layer, an undoped GaInAsP active layer, and a p-doped InP layer for avoiding the formation of defects near the active layer during etching. Etching using a mask, the active layer is reduced to a mesa. After removing the mask, the mesa is covered by a p-doped InP layer and a p-doped GaInAs cap layer.



5 All the growth steps of the above method are performed
by low pressure MOVPE and hence large scale production
should be facilitated. Further it is particularly
convenient since only one growth technique must be
employed. However, the devices produced rely on a
built-in potential difference between the large area p-n
homo-junctions to each side of the active region and the
p-n heterojunction through the relatively small area
active region itself. Although a lowest measured
10 threshold current of 11 mA using continuous wave operation
has been quoted, the values given for measurements
relating to 269 devices were variable in the range from
17.9 mA to 50.0 mA inclusive. 44⁰/o of these devices
had a threshold current of more than 45 mA. An optical
15 power emission of only up to 15 mW is quoted, and current
blocking on either side of the mesa had to be improved by
proton bombardment to the depth of the p-n junction and
beyond. Such bombardment is not easy to carry out with
satisfactory results.

20 It is an object of the present invention to provide an
improved semiconductor structure and a method of
manufacture therefor.

25 Hereinafter, structures and devices may be described
in terms, such as "uppermost", which imply a specific
orientation of the structure or device. The use of such
terms is for convenience of description only and should
not be taken to limit any structure or device to a
specific orientation.

30 According to a first aspect of the present invention
there is provided a semiconductor structure, comprising a
substrate having epitaxial layers deposited thereon, there
being an interface which extends in a generally transverse
direction with respect to the face of the substrate,



between first and second regions of the layers, wherein at least a major portion of the interface corresponds at least substantially to a (111) B crystallographic plane of the material or materials of the first region, the layers of the first and second regions being at least substantially flat right up to the interface.

It has been found that, surprisingly, it is possible to grow layers in the second region, against such an interface, which tend to show no significant change in depth even immediately adjacent the interface. This means that relatively good control may be exercised over the positions of, for instance, transitions from one layer to the next in the first and second regions, even at the interface. Hence the relative positions of semiconductor junctions can be better controlled at the interface if layers of each region are appropriately doped.

Particularly advantageously, it has been found that such semiconductor structures can be fabricated using MOVPE growth techniques, having the advantages described above.

It has been thought that the layers referred to grow so flat against the interface because of the phosphorous-rich nature of (111) B crystallographic planes of InP. However it has further been found, surprisingly, that the major portion of the interface may correspond to modified (111) B crystallographic planes without significantly affecting the flat characteristic of the layers in the second region. This can be particularly advantageous in the fabrication of some semiconductor structures where for instance an improved device can be made by a technique incorporating a heating step which causes material transport at the interface before the layers of the second region are grown. An example of such



a device can be a buried heterostructure laser. A technique incorporating a heating step, and a semiconductor structure made by the use of the technique, is described below. (The heating step acts to "clean up" the sides of a mesa so that improved growth of confinement layers against the mesa occurs, in spite of the treatment history of the mesa before growth.)

The term "modified (111) B crystallographic plane" means that the major portion of the interface has been fabricated by exposing a (111) B crystallographic plane in the material of the first region, then subsequently modifying the plane, for instance by heat treatment causing material transport, so that it no longer accurately represents a (111) B crystallographic plane. However, the interface will retain general characteristics of the (111) B crystallographic plane, for instance the overall direction of slope and the characteristic interaction with certain growth techniques, particularly MOVPE, which allows the layers in the second region to grow relatively evenly, right up to the interface.

Preferably the major portion of the interface comprises of the order of 60⁰%, or more preferably of the order of 80⁰%, of that interface. Also preferably, said major portion should comprise parts of the interface both adjacent to, and furthest from the substrate. Both these preferred features tend to encourage a generally flat characteristic of the layers grown against the interface.

According to a second aspect of the present invention there is provided a semiconductor structure, comprising a substrate having a mesa supported by a face thereof, the mesa comprising a p-n junction which extends parallel to the face of the substrate, the lateral surfaces of the mesa being buried by one or more confinement layers,



wherein at least a major proportion of the lateral surfaces of the mesa correspond at least substantially to (111) B crystallographic planes of the material or materials of the corresponding part or parts of the mesa.

5 Semiconductor structures according to the second aspect of the present invention are particularly useful in buried heterostructure lasers.

10 Because semiconductor material such as InP can be used to grow surprisingly flat confinement layers against the lateral surfaces of such a mesa, for instance by means of MOVPE, the depth and positional relationship of the layers to a mesa can be relatively closely controlled. This is particularly important where the mesa contains a p-n junction and the confinement layers present an n-p
15 junction to block current flow in use of a device. It can also be advantageous for subsequent steps in fabrication of a device.

20 As before, the (111) B crystallographic planes may be modified, for instance by heat treatment causing material transport.

25 It has been found that, as mentioned above, if the mesa incorporates an active layer of a device, the device may be improved by heating the structure, before growth of confinement layers against the lateral surfaces, so as to cause material transport onto the sides of the active layer. This is preferable to growing the confinement layers against the sides of the active layer directly after etching those sides, producing for instance a device with more reliable performance characteristics.

30 According to a third aspect of the present invention there is provided a method of making a semiconductor structure according to the first aspect of the present invention which comprises the stages of:

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i) etching a wafer of semiconductor material to create a step having a rising surface, corresponding to the interface, at least a major portion of which surface comprises (111) B crystallographic planes of the material, and

ii) growing semiconductor material by means of any one of a MOVPE, a MBE or a MOMBE technique to create the layer or layers of the second region.

The method may further comprise a stage in which the (111) B crystallographic planes are modified, for instance by heating to cause material transport at the interface, before the growth of the semiconductor material. To prevent growth on the layer or layers of the first region, an epitaxial growth suppressing material may be deposited on that layer or layers prior to stage ii) above.

According to a fourth aspect of the present invention there is provided a method of making a semiconductor structure according to the second aspect of the present invention which comprises the steps of:

- i. forming a stripe of an epitaxial growth suppressing material on a heterostructure wafer;
- ii. using the stripe as a mask, etching a mesa with an etchant or a selection of etchants such that at least a major proportion of the lateral surfaces of the mesa comprise (111) B crystallographic planes of the material of the mesa;
- iii. using epitaxial growth to grow the confinement layers against the lateral surfaces of the mesa; and
- iv. removing the stripe.

An important application of the present invention is in the production of lasers, particularly those which will operate in a single transverse mode. These lasers are of major importance in optical communication systems. Such



lasers can be produced from semiconductor structures made by the method of the present invention in which the uppermost surface of the mesa is restricted to being not more than 5 μm wide.

5 Step iii. above may advantageously be preceded by a step in which the lateral surfaces of the mesa are modified by heat treatment which causes material transport at those surfaces.

10 MOVPE can be used as the epitaxial growth technique of step iv. above. This has the particular advantages already described.

15 Single transverse mode semiconductor lasers, and a waveguide, according to embodiments of the present invention will now be described, by way of example only, with reference to the accompanying Figures in which:

Figure 1 shows a vertical cross section of a laser according to a first embodiment of the present invention;

20 Figure 2 shows a cross section of part of a double heterostructure wafer for use in making the laser of Figure 1;

Figures 3a to 3f show stages in production of the laser of Figure 1;

25 Figure 4 shows a scanning electron microscope image of a cross section of a semiconductor structure according to an embodiment of the present invention;

Figures 5 and 7 show cross sections of semiconductor lasers according to second and third embodiments of the present invention;

30 Figure 6 shows a stage in the production of a laser according to an embodiment of the present invention, following an optional additional treatment step;



Figure 8 shows a plot of the dimensions of a plurality of mesas fabricated from a common wafer according to embodiments of the present invention;

Figure 9 shows a longitudinal mode spectrum of a laser structure as shown in Figure 5;

Figures 10a and 10b show the far field patterns parallel and perpendicular respectively to the plane of the p-n junction of the mesa;

Figure 11 shows a histogram of active layer widths in mesas produced using methods according to the present invention, sampled from five different wafers; and Figure 12 shows a waveguide according to an embodiment of the present invention.

Figures 1 to 7, and 12, are not drawn to scale and cross hatching is omitted for the purposes of clarity.

As is the usual practice, although only one laser is shown in Figures 3a to 3f, several lasers will generally in fact be fabricated from the same wafer.

Referring to Figure 1, a laser structure 1 according to an embodiment of the present invention comprises a layered mesa 2, 3, 4 buried by three confinement layers 5, 6, 7, a capping layer 8 and a contact layer 9. The lateral surfaces 10 of the mesa 2, 3, 4, against which the confinement layers 5, 6, 7 have been grown, are defined by (111) planes of the materials of the mesa 2, 3, 4. The resultant cross section of the mesa has a distinctive concertinalike appearance as a result.

In more detail, the laser structure 1 comprises a substrate 12 of (100) orientated S doped InP, doping level n approximately equal to $8 \times 10^{18} \text{ cm}^{-3}$, about 250 μm thick. Covering the upper surface of the substrate 12 is a quaternary layer 11 of S doped GaInAsP (quaternary material), doping level n of the order of 1 to 2×10^{18}



cm^{-3} , up to about $0.2 \mu\text{m}$ thick and of a band gap lying in the range from 1.0 to $1.3 \mu\text{m}$. The layered mesa 2, 3, 4 is mounted on the quaternary material and has the following layers, starting with the lowermost:

- 5 i) an S-doped buffer layer 2 of InP, doping level n approximately equal to $2 \times 10^{18} \text{ cm}^{-3}$, $0.4 \mu\text{m}$ thick;
- ii) an undoped active layer 3 of GaInAsP of band gap $1.5 \mu\text{m}$ and $0.1 \mu\text{m}$ thick; and
- 10 iii) a Cd-doped layer 4 of InP, doping level p approximately equal to $5 \times 10^{17} \text{ cm}^{-3}$, $0.2 \mu\text{m}$ thick.

On each side of the mesa is a series of three confinement layers 5, 6, 7 as follows, again starting with the lower most:

- 15 iv) an S-doped layer 5 of InP, doping level n of the order of 1 to $2 \times 10^{18} \text{ cm}^{-3}$, of thickness $0.1 \mu\text{m}$;
- v) a Cd-doped layer 6 of InP, doping level p approximately equal to $5 \times 10^{17} \text{ cm}^{-3}$, of approximate thickness $0.4 \mu\text{m}$; and
- 20 vi) an S-doped layer 7 of InP, doping level n approximately equal to $1 \times 10^{18} \text{ cm}^{-3}$, of approximate thickness $0.4 \mu\text{m}$.

Extending across the uppermost surfaces of both the mesa and the confinement layers 5, 6, 7 is a capping
25 layer 8 of Cd-doped InP, doping level p approximately equal to $2 \times 10^{18} \text{ cm}^{-3}$, of thickness lying in the range 1 to $2 \mu\text{m}$. The capping layer 8 in turn is covered by a ternary contact layer 9 of Zn-doped GaInAs, doping level p approximately equal to $4 \times 10^{19} \text{ cm}^{-3}$, of thickness
30 lying in the range 0.05 to $0.3 \mu\text{m}$.

Contacts, for providing driving current to the laser structure, are provided through a window 13 in a silica layer 14 over the contact layer 9, and to the lowermost



surface of the substrate 12. The contacts 15, 16 and 17
comprise Ti Au tunnelling Schottky contacts applied by
radio frequency sputtering and annealing. Pt may
advantageously be included as a diffusion barrier between
the Ti and the Au in the contact 15, 16 through the window
13. This contact configuration is known and further
details are not therefore provided herein.

Referring to Figures 2 and 3a to 3f, in a method of
fabricating a laser structure according to Figure 1,
firstly a double heterostructure wafer is produced. The
wafer (shown in Figure 2) comprises the substrate 12, the
quaternary layer 11, and the layers 2, 3, 4 which are
present in the mesa of the finished laser structure.

The layers 11, 2, 3, 4 are all lattice-matched to the
respective layer below, being grown by MOVPE under normal
growth conditions.

A silox stripe 18, $1.8\text{ }\mu\text{m}$ wide and $0.2\text{ }\mu\text{m}$ thick (shown
in Figures 3a to 3e), is then produced extending in the
(110) direction with respect to the crystalline structure
of the substrate 12. The stripe 18 is produced by the use
of the known combination of a positive photoresist mask
and buffered HF as an etchant.

Etching the wafer, which comprises layers of different
semi-conductor materials which must each be etched to
produce the layered mesa 2, 3, 4, must be carried out
using different selective etchants. The uppermost, InP
layer 4 is etched using hydrobromic acid. The active
layer 3 is etched using a mix of sulphuric acid, hydrogen
peroxide and water. The InP buffer layer 2 is etched by
again using hydrobromic acid. The actions of these
etchants in this crystallographic orientation are well
documented.

Alternatively the active layer 3 may be etched using a



mixture of potassium dichromate (1/6 molar), sulphuric acid, and hydrochloric acid in the ratio 3 : 1 : 1. The action of this etchant is further discussed below.

5 The hydrobromic acid etches through the uppermost InP layer 4 at a rate of about 6 μm per minute of InP at 20°C, or 2.5 μm per minute at 5°C, being stopped by the quaternary active layer 3. When the active layer 3 is reached, the etch rate drops significantly for instance by a factor of 3 or 4. Referring to Figure 3b, the
10 characteristic result at this stage is a shallow mesa profile with sides formed largely, or entirely, by (111) B planes. If the silox stripe 18 is well adhered to the InP layer 4, the planes exposed by the etchant are (111) A immediately below the silox stripe 18, then (111) B down
15 to the active layer 3. The ratio of A to B planes (in terms of the depth of the mesa showing each type of plane at this stage) has been observed to be about 1 : 4. If the silox stripe 18 is not well adhered, then the only plane exposed is generally the (111) B plane. Figure 3b
20 shows a mesa profile where the silox stripe 18 was not well adhered. In the latter case, as shown, there is a slight undercut, generally of up to 0.2 μm , of the silox stripe 18.

25 It was noted that in some cases the hydrobromic acid contained colloidal particles. These were removed by filtration.

30 Using the acid/peroxide mixed etchant, the active layer 3 is then etched. The mixed etchant etches at a rate of 0.4 μm per minute and is stopped by the InP buffer layer 2. Referring to Figure 3c, the sidewalls of the active layer 3 are characteristically etched to expose (111) A planes by this process. Hence at this stage a mesa has been formed which has an angular "bulge" in its sidewalls.



As mentioned above, the active layer 3 can alternatively be etched using a dichromate acid etchant. This etchant has the advantages of etching all wavelengths of quaternary material between InGaAs and InP, and of etching the active layer 3 only relatively slowly in a lateral direction once the (111) A plane has been exposed. Because of the latter feature, over etching of the active layer 3 does not cause deep undercutting of the uppermost InP layer 4. It has been found that the dichromate/acid etchant etches quaternary material of emission wavelength $1.5 \mu\text{m}$ at a rate of about $0.8 \mu\text{m}$ per minute in a downwards direction at 5°C . However the etch time for the active layer 3 in the present case has been found to tend to be variable where there is lattice mismatch in the double heterostructure wafer. An etch time of 60 secs is used to ensure complete clearance of the active layer 3. (If the active layer 3 comprises a quaternary material having a band gap of $1.3 \mu\text{m}$, then an etch time of 10 mins has been found suitable).

Reverting to hydrobromic acid as the etchant, the InP buffer layer 2 is then etched until the quaternary layer 11 which covers the substrate 12 stops the action of the etchant. Referring to Figure 3d, the resultant layered mesa 2, 3, 4 has the characteristic concertinalike appearance referred to above. If the active layer 3 has been overetched, this final etching step has been found to cut the uppermost InP layer 4 back rapidly, but only as far as the top corner of the (111) A plane in the active layer 3. Hence the same mesa 2, 3, 4 profile is achieved, though the degree of overetching will affect the mesa width.

It has been noted that during the final etching step, the active layer 3 appears to act as a strongly adherent



mask and the InP buffer layer 2 is at first etched along (111) A planes before the (111) B plane reasserts itself. This means that the angle produced in the mesa sidewall by the transition from A back to B planes does not coincide with the interface between the active and buffer layers 3, 2. This can be seen for instance in figure 3d.

After etching of the layered mesa 2, 3, 4, the three confinement layers 5, 6, 7 are grown in. The action of the silox stripe 18 during this stage is to suppress growth of InP. Referring to Figure 3e, the result is that the confinement layers 5, 6, 7 grow either side of the mesa leaving the silox stripe 18 exposed.

Growth conditions for the confinement layers are generally as are normal for MOVPE growth but before growth starts, the sample is heated to 700°C for 20 minutes in the presence of PH_3 . This treatment has been found to enhance the action of the silox as a MOVPE growth-suppressing material even when the silox stripe is reduced in width for instance to values as low as about 1 μm . Further, the heating involved appears to allow surface reconstruction to occur which improves the morphology of subsequently grown epitaxial layers. This surface reconstruction can be significant, modifying the lateral surfaces of the mesa by means of material transport particularly at the base of the mesa, and onto the exposed surfaces of the active layer. The concentration of PH_3 should be high enough to prevent incongruous evaporation of the InP. The period for which the sample must be heated in the presence of PH_3 will vary according to the conditions applied. For instance, if the concentration of PH_3 is increased, the period may be reduced.

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Where the uppermost InP layer 4 had been etched so as to undercut the silox stripe 18, it was noted that high device yields were achieved. This was because the silica overhang forces the confinement layers to "wing", or flare away, from the bottom surface of the silox stripe 18. Consequently few overgrowth bridges occur, where the confinement layers meet above the silox stripe 18. Such winging occurs even in the absence of an overhang but it is enhanced where an overhang is present.

Referring to Figure 3f, when the confinement layers 5, 6, 7 are complete, the silox stripe is removed in a 40% aqueous solution of HF and the capping and contact layers 8, 9 are grown, again by MOVPE.

Referring to Figure 4, it is possible to see, using a scanning electron microscope, that significant mass transport may take place onto the sides of the active layer 3 in a mesa during the heating step prior to growing the confinement layers.

To complete the laser as shown in Figure 1, the contacts 15, 16, 17 are applied by conventional techniques. It can then be conveniently mounted on a heat sink (not shown) by soldering the heat sink to the Au layer of the contact 15, 16.

The laser described above with reference to Figures 1 to 3f has a number of advantageous features. Firstly, the confinement layers 5, 6, 7 tend to grow in substantially planar, particularly at a distance down the lateral surfaces of the mesa 2, 3, 4 of more than 0.5 μm from the silox stripe 18. Further, as mentioned above, the uppermost confinement layer 7 tends to "wing" away from the silox stripe 18, leaving a wide opening which gives good access for subsequent removal of the stripe 18. The capping and contact layers 8, 9 tend to grow with a planar



characteristic which facilitates heat sinking and, also, at least two semiconductor junctions are grown by consecutive growth steps into the confinement layers 5, 6, 7. This avoids having junctions coincident with layer interfaces which have been chemically degraded for instance by the use of etchants.

Particularly advantageous is the novel use of a first quaternary layer 11, independent of the active layer 3, on the substrate 12. This acts as a stopping layer to the etchant used to etch the lowermost mesa layer 2. It also acts to prevent breakdown, even at large gate currents, of the p-n-p-n thyristor-like structure of the confinement layers 5, 6, 7 in combination with the capping layer 8. As a result leakage currents are blocked which would otherwise bypass the active region of the laser in use. By using a first quaternary layer 11 which is independent of the active layer 3, its characteristics such as band gap are not tied to those of the active layer 3. By reducing the bandgap, for instance to values in the range 1.0 to 1.3 μm as described above, the effectiveness of the first quaternary layer 11 in preventing leakage currents may then be improved.

The first quaternary layer 11 has even a third function, as part of the waveguiding structure of the laser. As long as the buffer layer 2 of the mesa is sufficiently thin, the first quaternary layer 11 can "dilute" the lateral refractive index step at the sides of the mesa, allowing wider mesas with the same mode cut-off properties. This is desirable for processing, device resistance and radiation beam width reasons. In addition the first quaternary layer 11 could have distributed feedback (DFB) gratings etched into it, planar growth being resumed to deposit the layers 2, 3 and 4 of the



mesa. (Again the buffer layer 2 should be relatively thin, say from 0.1 to 0.5 μm thick, to allow the desired degree of optical interaction).

5 The use of a first quaternary layer in a semiconductor laser structure, independent of the active layer, lying above the substrate and extending below the mesa, may be found advantageous more generally than in structures of the type described in the present specification.

10 Referring to Figure 5, variations may be made in the layers of the laser structure. For instance the first quaternary layer 11 may be left out and a deeper buffer layer 2 used, the layered mesa 2, 3, 4 extending only partially down into the buffer layer 2. The final etching step, in which the buffer layer 2 is etched, will then
15 have to be controlled by timing rather than by relying on the action of the first quaternary layer 11 as a stopping layer.

Referring to figure 6, it has been found advantageous to "notch" the active layer 3 immediately before heating
20 and growth of the confinement layers. An etchant which attacks only the active layer 3, and which selectively exposes the (111) A planes, is used to narrow the active layer 3 preferentially. A suitable etchant comprises sulphuric acid, hydrogen peroxide, and water in the ratio
25 3:1:1. This "notching" of the active layer 3 is believed to provide a clean, fresh surface on the side of the active layer 3, which benefits the subsequent process steps.

30 Other variations may be that the unetched thickness of the buffer layer 2 may conveniently range up to 4 μm , and the height of the layered mesa 2, 3, 4 may be as much as 1.4 μm . Different dopants and doping levels may be used, such as Zn instead of Cd in the uppermost layer 4 of the mesa, doped to a level of $2 \times 10^{18} \text{ cm}^{-3}$ instead of $5 \times 10^{17} \text{ cm}^{-3}$.



The second of the confinement layers 6 may comprise a "semi-insulating" material such as Fe doped InP instead of the p-doped InP referred to above. Such a material tends to have a relatively high resistivity.

5 The silox stripe 18 might be replaced by a stripe of different material, such as a different form of silica, or another dielectric material such as Si_3N_4 or alumina.

Referring to Figure 7, an additional p-doped layer 19 of InP may be grown onto the confinement layers 5, 6, 7. This avoids coincidence between the uppermost p-n junction provided by the confinement layers 5, 6, 7 and a chemically treated interface such as the interface between the confinement layers and the capping layer 8, which may be degraded during removal of the silox stripe 18.

15 The detailed growth of InP confinement layers by MOVPE against a layered mesa 2, 3, 4 of the type shown in Figure 5 has been investigated by growing alternating layers of p- and n-doped InP and using a scanning electron microscope (SEM) to obtain images of the layers. It was noted that there were no voids on the sides of the mesa, or under the overhang of the silox stripe 18 at least for an overhang of up to $0.2 \mu\text{m}$. The most interesting feature was the growth of the confinement layers parallel to the (100) plane. Only when the confinement layers were approaching within $0.2 \mu\text{m}$ of the silox stripe 18 did they begin to thicken preferentially at the points of contact with the mesa sidewalls.

Referring to Figure 8, the uniformity of a plurality of mesas produced on a single wafer was investigated by taking a cleave from one end of the wafer and examining mesa dimensions using an SEM. The approximate size of the wafer was $10\text{mm} \times 12\text{mm}$. All of the mesa dimensions were found to have been controllable to within $0.1 \mu\text{m}$. The



wafer was subsequently overgrown with confinement layers and only an insignificant number of bridges of the silox stripes could be visually observed.

5 Lasers fabricated according to embodiments of the present invention have produced up to 50 mW under direct current (dc) operation. The electrical characteristics have shown no appreciable conduction of current through the confinement layers due to mesa or overgrowth defects.

10 Referring to Figure 9, a longitudinal mode spectrum of a laser of the type shown in Figure 5, using n-, p- and n-doped confinement layers 5, 6, 7, has been found to show a smooth envelope of modes and no evidence of higher order transverse modes.

15 Referring to Figures 10a and 10b, far field spectra from such a laser have been found to show a full width at half maximum (fwhm) of 24° for the parallel direction and 30° for the perpendicular direction, with reference to the plane of the active layer. The far field spectra were also relatively smooth. It is considered that the smooth condition of the mesa sidewalls led to the smoothness of the far field spectra.

20 Referring to figure 11, the width of the active layer was measured in 80 different mesas, produced over five different wafers. Using silox stripes of $2.0\ \mu\text{m}$ and $1.85\ \mu\text{m}$ width, the active layer widths ranged from $1.4\ \mu\text{m}$ to $1.9\ \mu\text{m}$, with one active layer width lying in the range from $1.9\ \mu\text{m}$ to $2.0\ \mu\text{m}$. The active layer widths achieved on each wafer are shown as a histogram on Figure 11, differentiated as indicated by the markings within the columns of the histogram.

30 Although the embodiments of the present invention described above are fabricated using MOVPE, this could be replaced by MBE or MOMBE, although some changes in process conditions might then be necessary.



Referring to Figure 12, semiconductor structures other than lasers can be fabricated as embodiments of the present invention. As shown in the Figure, instead of a mesa, a channel might be created, the sides 20 of the channel being provided by (111) B crystallographic planes. If material is subsequently grown into the channel in layers having a substantially flat characteristic almost right up to the sides 20 of the channel, then a particularly useful waveguiding structure can be created.

The material grown into the channel may comprise a quaternary, InGaAsP, and the material into which the channel is created may comprise InP.

Other semiconductor structures which could beneficially be made according to embodiments of the present invention are optical detectors and opto-electronic integrated circuits (OEICS).





CLAIMS

1. A semiconductor structure, comprising a substrate having epitaxial layers deposited on a face thereof, there being an interface which extends in a generally transverse direction with respect to the substrate, between first and second regions of the layers, wherein at least a major portion of the interface corresponds at least substantially to (111) B crystallographic planes of the material or materials of the first region, the layer or layers of the first and second regions being at least substantially flat right up to the interface.
2. A semiconductor structure according to claim 1, wherein the major portion of the interface corresponds to modified (111) B crystallographic planes of the material or materials of the first region.
3. A semiconductor structure according to either one of claims 1 or 2, wherein the major portion of the interface is at least of the order of 60⁰/o of the area of the interface.
4. A semiconductor structure according to either one of claims 1 or 2 wherein the major portion of the interface is at least of the order of 80⁰/o of the area of the interface.
5. A semiconductor structure according to any one of the preceding claims, wherein the major portion of the interface comprises parts of the interface adjacent to and furthest from the substrate.
6. A semiconductor structure comprising a substrate having a mesa supported by a face thereof, the mesa comprising a p-n junction which extends parallel to the face of the substrate, the lateral surfaces of the mesa being buried by one or more confinement layers, wherein at

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least a major proportion of the lateral surfaces of the mesa is provided by (111) crystallographic planes of the material or materials of the corresponding part or parts of the mesa.

- 5 7. A semiconductor structure according to claim 6, wherein the crystallographic planes comprise a (111) B crystallographic plane.
8. A semiconductor structure according to claim 6, wherein the major proportion of the lateral surfaces of
- 10 the mesa is provided by modified (111) B crystallographic planes of the material or materials of the corresponding part or parts of the mesa.
9. A semiconductor structure according to any one of claims 6 to 8, wherein the material of the corresponding
- 15 part or parts of the mesa is InP.
10. A semiconductor structure according to any one of claims 6 to 9, wherein the material of the confinement layer or layers comprises InP.
11. A semiconductor structure according to any one of
- 20 claims 6 to 10, wherein the confinement layer or layers are grown by MOVPE.
12. A semiconductor structure according to any one of claims 6 to 11, wherein the p-n junction lies in or adjacent to an active layer in the mesa.
- 25 13. A semiconductor structure substantially as described hereinbefore with reference to any one of Figures 1 to 7 of the accompanying drawings.
14. A semiconductor laser comprising a semiconductor structure according to any one of the preceding claims.
- 30 15. A semiconductor laser structure comprising a substrate having a mesa supported by a face thereof, the mesa incorporating an active layer of quaternary material, the lateral surfaces of the mesa being buried by confinement

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layers which provide to each side of the mesa at least one current blocking semiconductor junction, wherein a second layer of quaternary material extends over the face of the substrate beneath the mesa and the confinement layers.

5 16. A semiconductor laser structure according to claim 15, wherein the band gap of the second layer of quaternary material is lower than the band gap of the active layer.

17. A semiconductor laser structure substantially as described hereinbefore with reference to Figures 1 to 3 of the accompanying drawings.

10 18. A method of making a semiconductor structure which comprises the stages of:

i) etching a wafer of semiconductor material to create a step having a rising surface, at least a major portion of which rising surface comprises a (111) B crystallographic plane of the material of the wafer; and

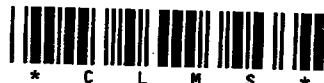
15 ii) preferentially growing semiconductor material by means of any one of a MOVPE, a MBE or a MOMBE technique onto the etched surface of the wafer, to meet the rising surface of the step.

19. A method according to claim 18, wherein stage i) is carried out using a mask of an epitaxial growth suppressing material to create the step, the mask being subsequently used to achieve the preferential growth of stage ii).

20 20. A method according to either one of claims 18 or 19 which further comprises a stage in which the (111) B crystallographic plane is modified prior to stage ii).

30 21. A method of making a semiconductor structure which comprises the steps of:





- 5
- 10
- 15
- 20
- 25
- 30
- i forming a stripe of an epitaxial growth suppressing material on a heterostructure wafer;
 - ii using the stripe as a mask, etching a mesa with an etchant or a selection of etchants so as to expose (111) B crystallographic planes over at least a major portion of the lateral surfaces of the mesa;
 - iii using epitaxial growth to grow confinement layers against the lateral surfaces of the mesa; and
 - iv removing the stripe.
22. A method according to claim 21 which further comprises the step of modifying the exposed (111) B crystallographic planes by heat treatment sufficient to cause material transport at the lateral surfaces of the mesa, prior to step iii.
23. A method according to either one of claims 21 or 22, wherein the stripe comprises a MOVPE growth suppressing material and the confinement layers are grown by MOVPE.
24. A method according to claim 23, wherein the semiconductor structure comprises a structure according to any one of claims 1 to 13.
25. A method of making a semiconductor structure substantially as described hereinbefore with reference to any one of figures 1 to 7 of the accompanying drawings.

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ABSTRACT

SEMICONDUCTOR STRUCTURES AND A METHOD OF
MANUFACTURING SEMICONDUCTOR STRUCTURES

5 In a semiconductor buried heterostructure laser, having a
mesa 2, 3, 4 and confinement layers 5, 6, 7 on a substrate
12, at least the lowermost of the confinement layers 5, 6,
7 is substantially planar up to the mesa. This is
achieved by MOVPE growth of InP against lateral surfaces
of the mesa 2, 3, 4 which are defined by distinct
10 crystallographic planes of the material of the mesa. In
particular (111) B InP planes are used. The laser is
particularly for use in the field of optical
communications.

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Fig. 1.

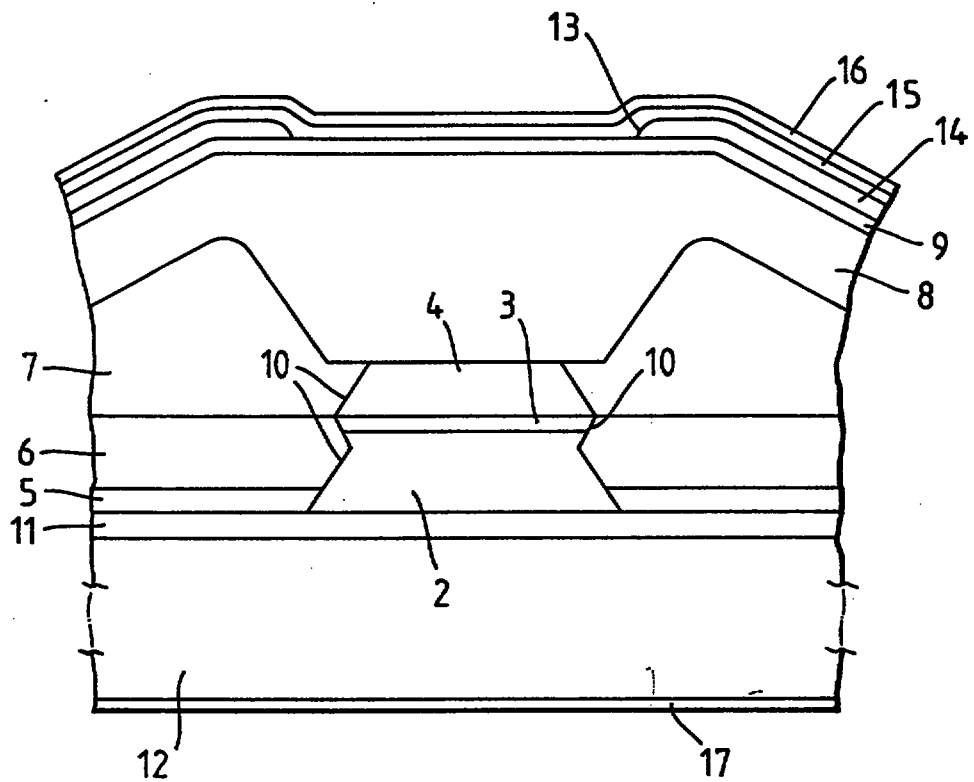
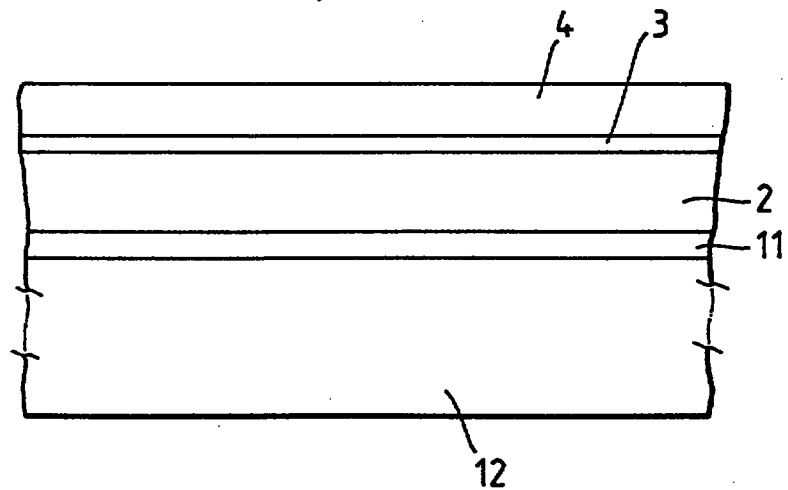


Fig. 2.



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Fig. 3a.

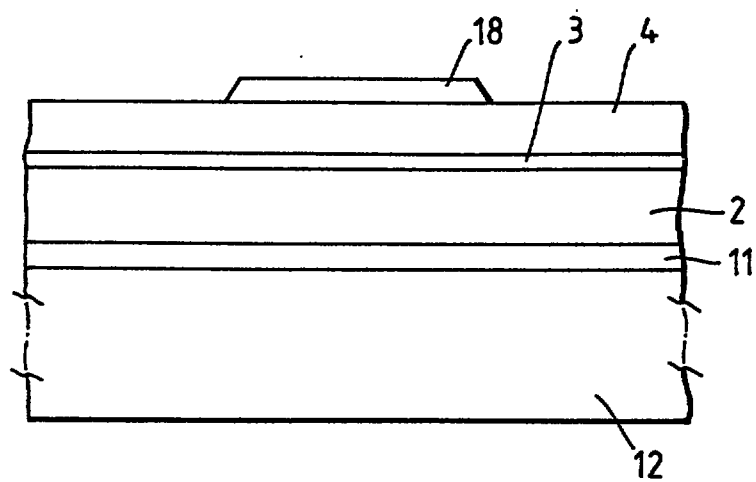


Fig. 3b.

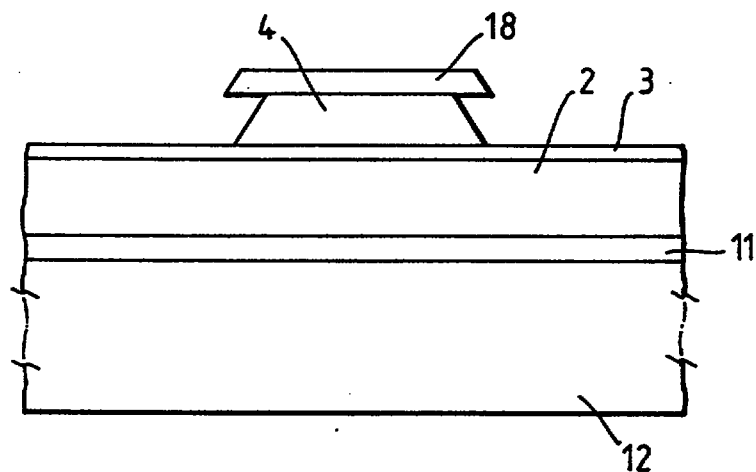
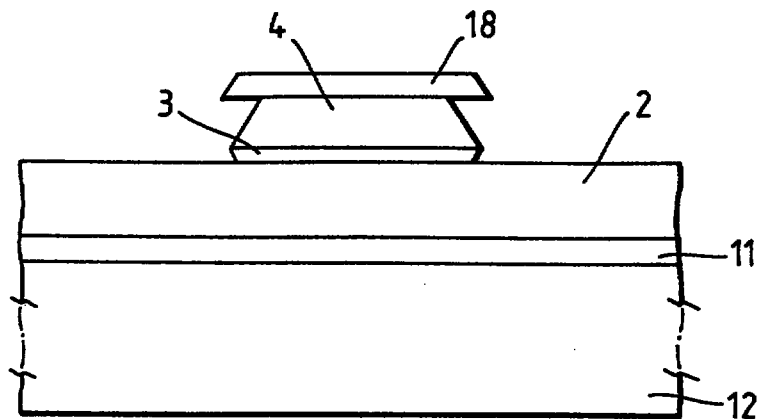


Fig. 3c.



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Fig. 3d.

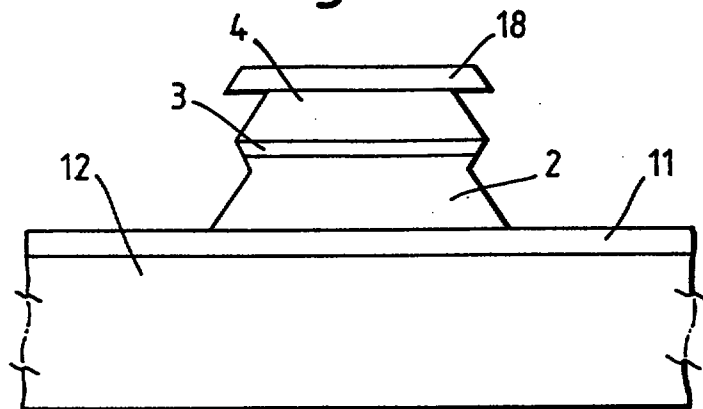


Fig. 3e.

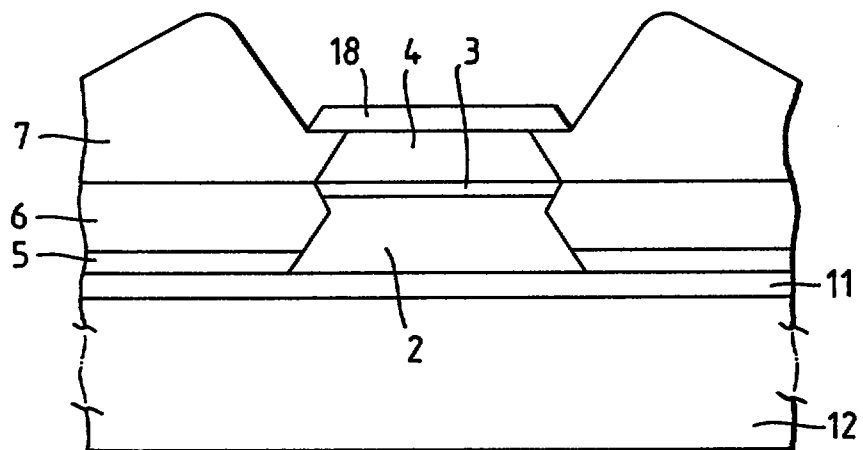
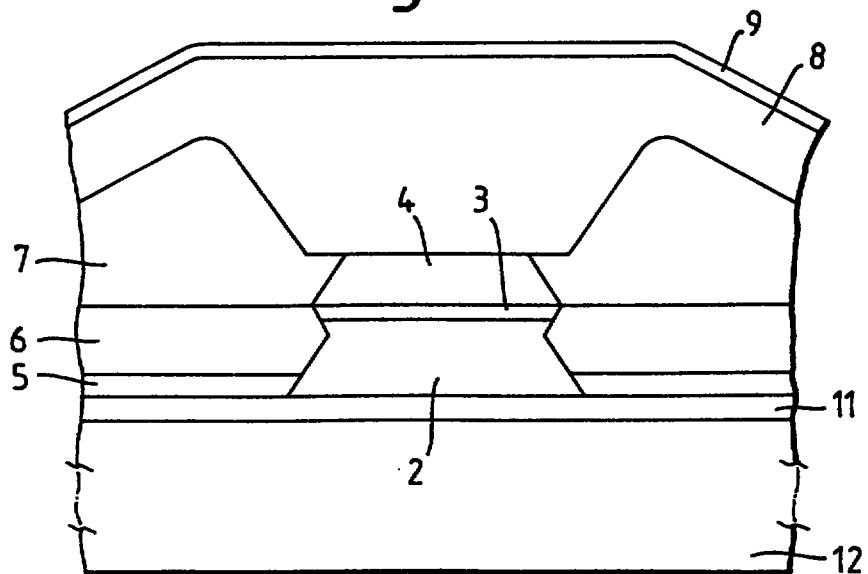


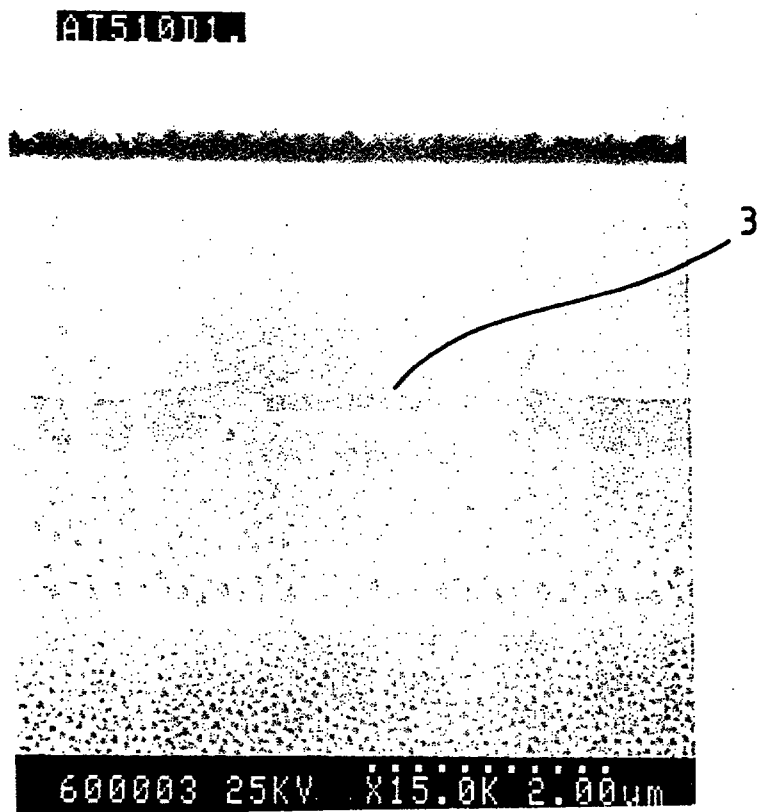
Fig. 3f.



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Fig. 4.



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Fig.5.

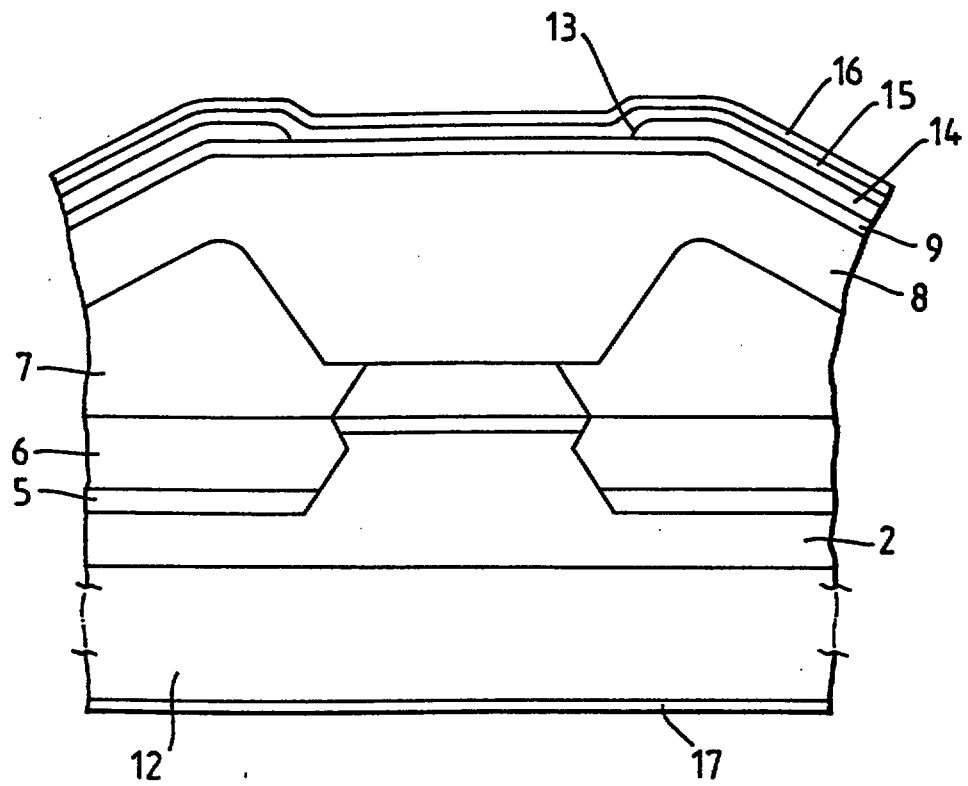
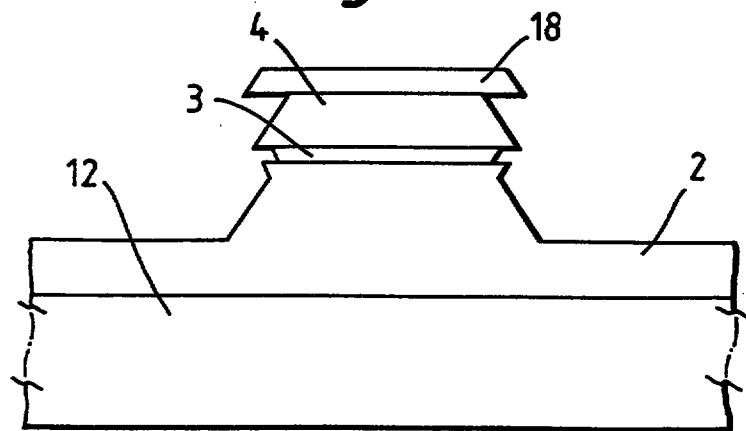


Fig.6.



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Fig. 7.

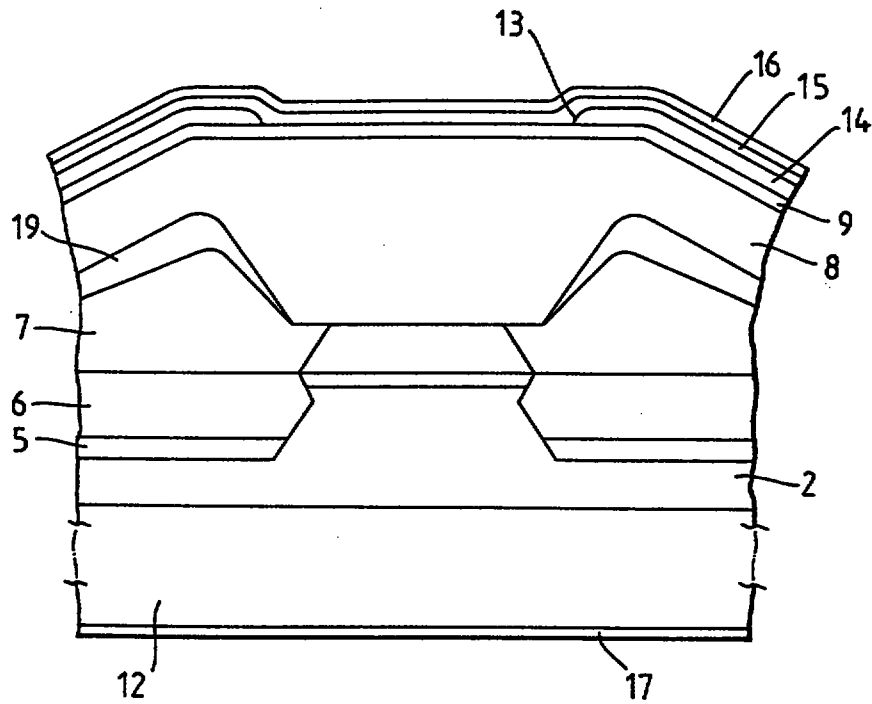
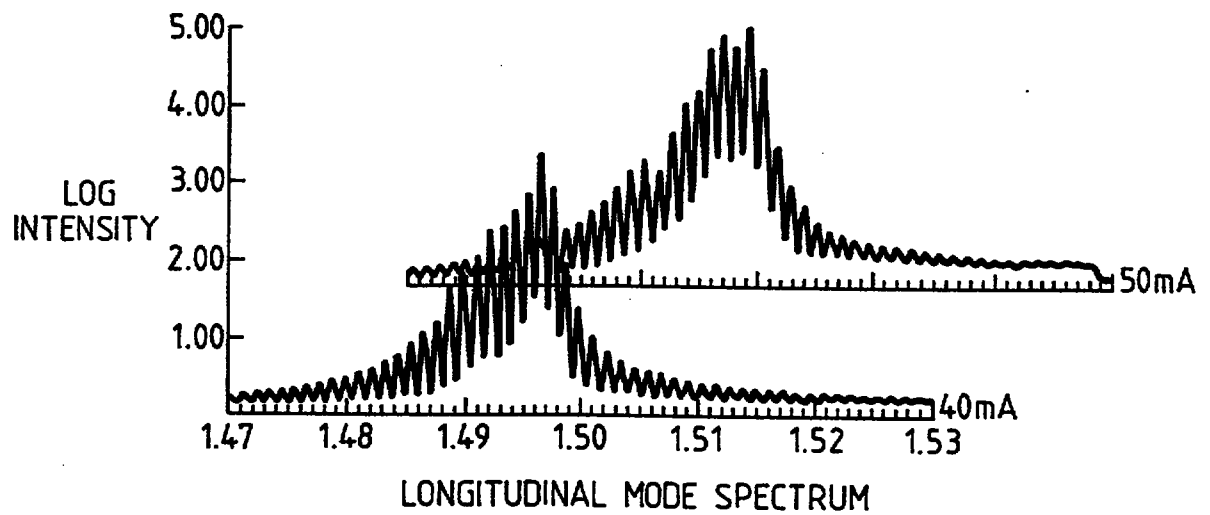


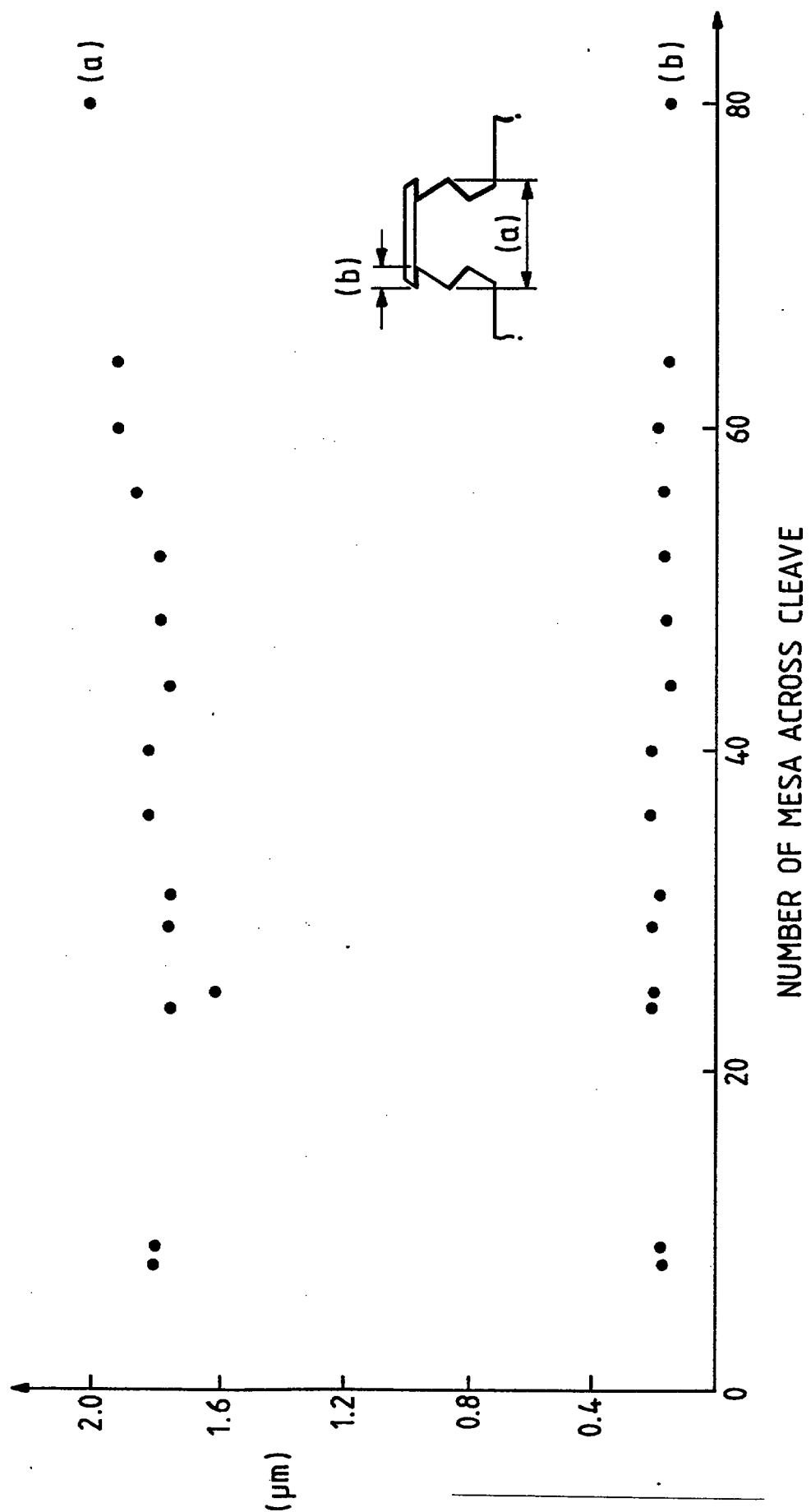
Fig. 9.



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Fig.8.



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Fig.10(a)

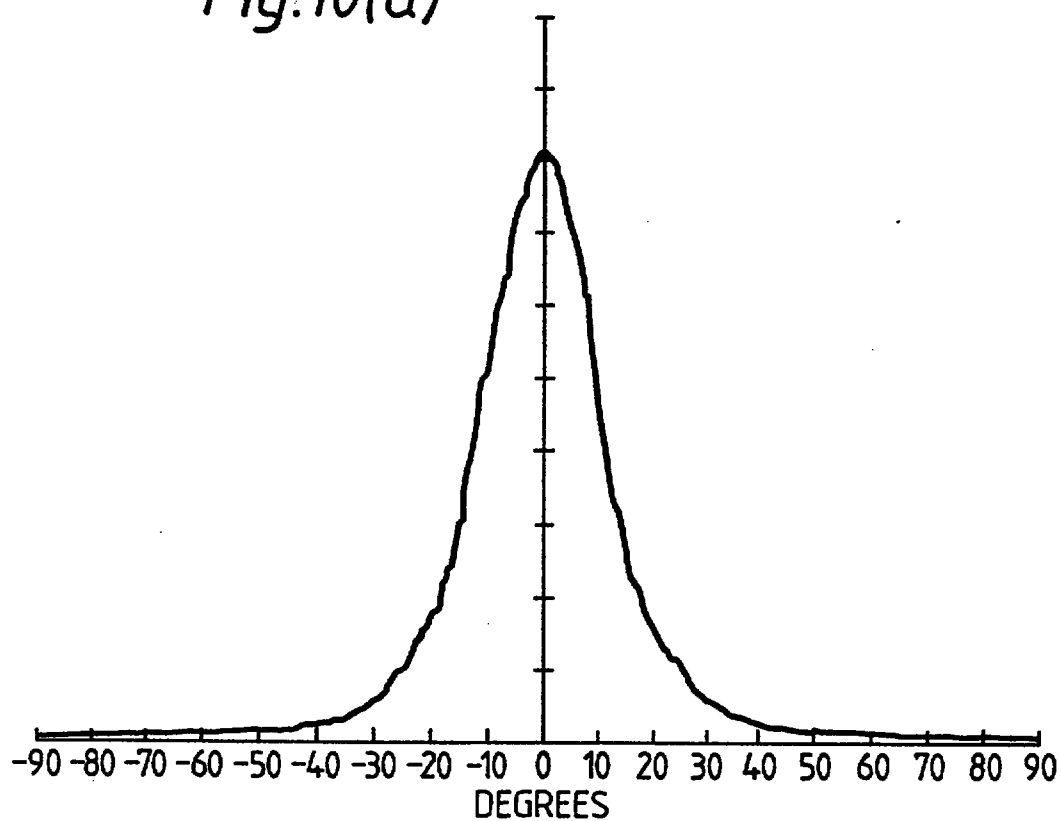
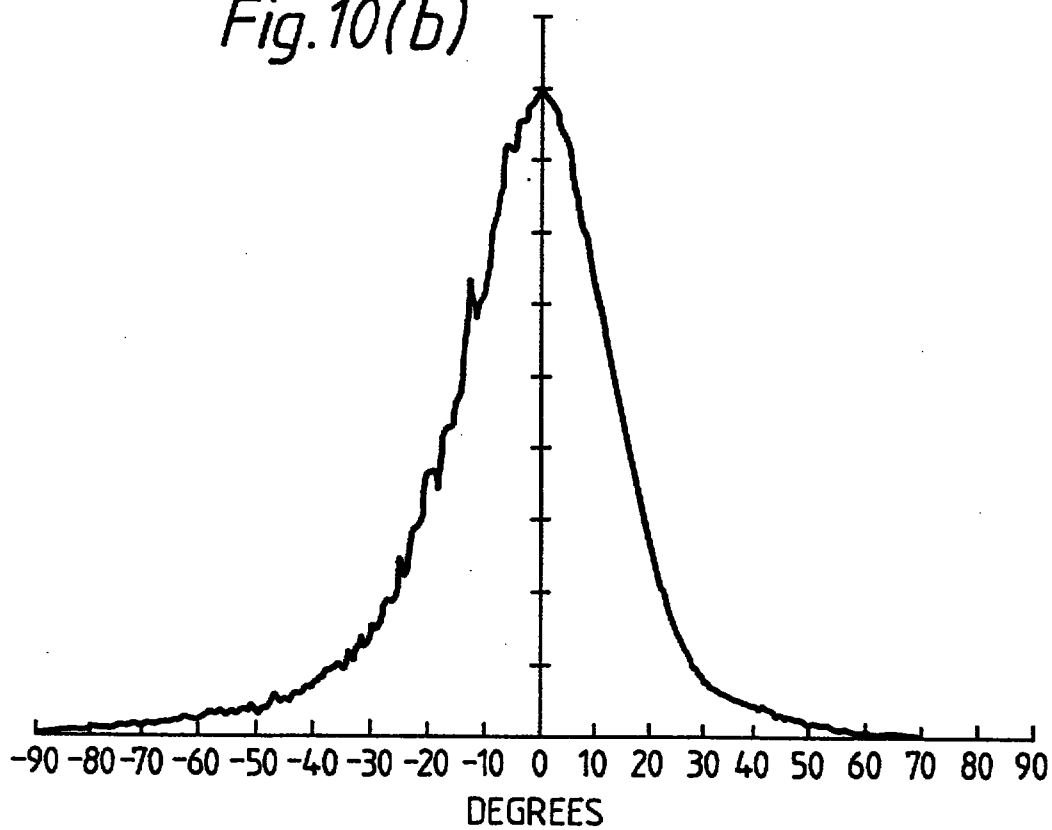


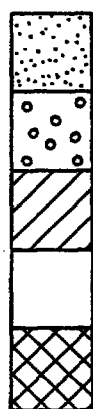
Fig.10(b)



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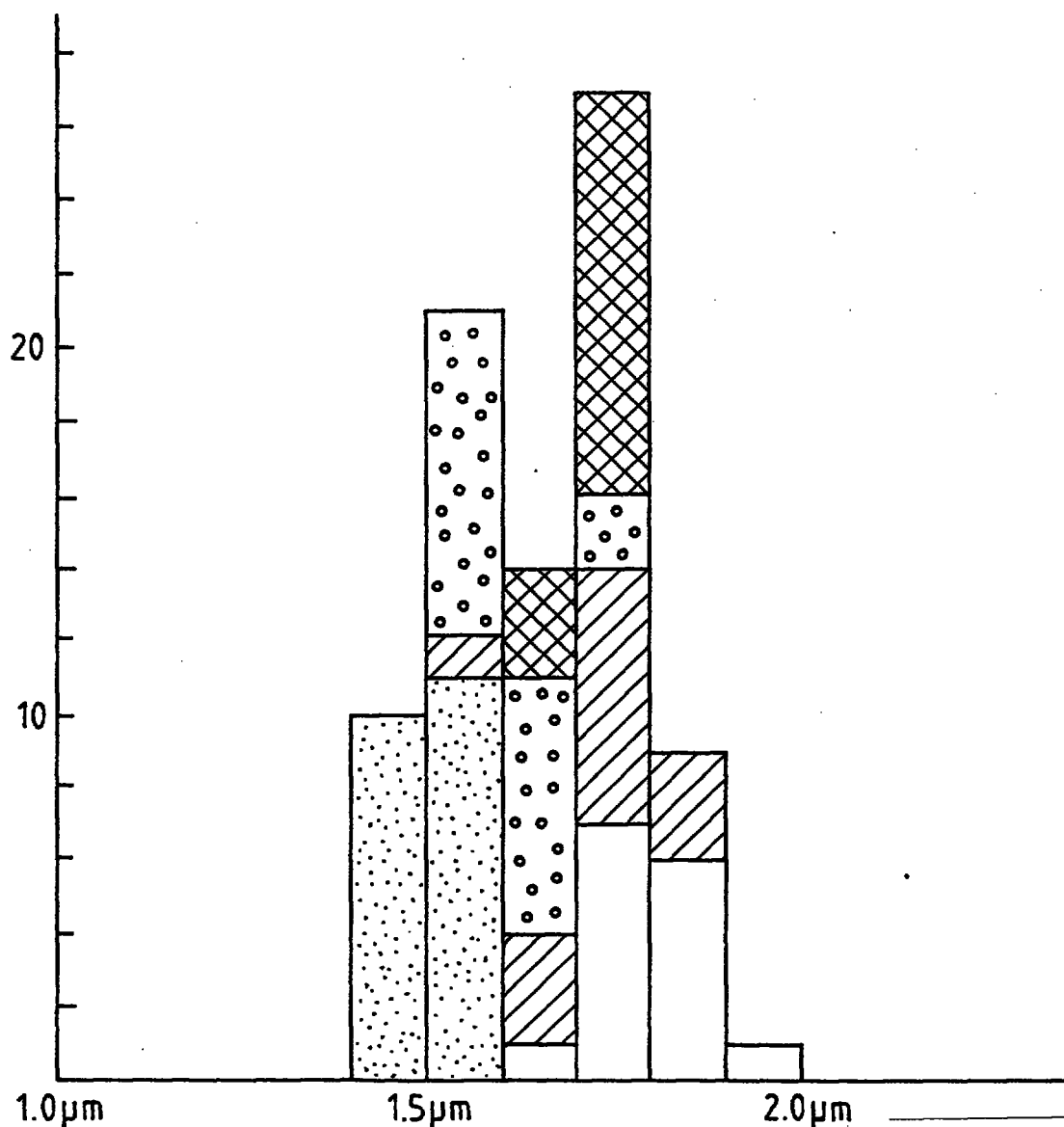


Fig. 11.



WAFER NO. AQ460; SILOX STRIPE WIDTH 2.0 μ m

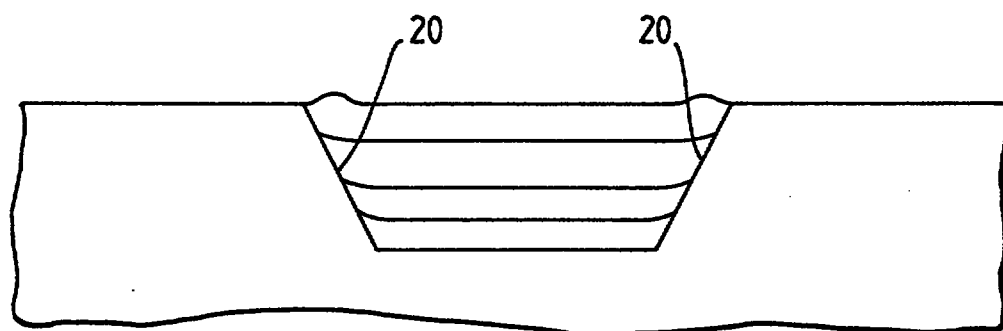
//	//	AQ485(ii);	//	//	//	1.85 μ m
//	//	AF108 ;	//	//	//	1.85 μ m
//	//	AQ482 ;	//	//	//	1.85 μ m
//	//	AQ485(i);	//	//	//	1.85 μ m



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Fig. 12.



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**SEMICONDUCTOR STRUCTURES AND A METHOD OF
MANUFACTURING SEMICONDUCTOR STRUCTURES**

The present invention relates to semiconductor structures. It finds particular application in the field of opto-electronic devices such as semiconductor lasers, and their manufacture.

A known family of opto-electronic devices, buried heterostructure (BH) semiconductor lasers, is based on the following general structure : a substrate of semiconductor material having a mesa thereon, with confinement layers on either side of the mesa. Such a device is described by O Mikami et al in "1.5 μm GaInAsP/InP Buried Heterostructure Lasers Fabricated by Hybrid Combination of Liquid - and Vapour-Phase Epitaxy", Electronics Letters, 18 (5) (4.3.82) pages 237-239. (The word "mesa" in this context is used to describe an upstanding stripe having a flat top.)

The devices of the family include a planar p-n junction across which current flows (the conventional current from p to n) and a waveguide region adjacent to the junction to which light is confined. The waveguide region may comprise an "active layer" in which electrons and holes combine with the production of photons by radiative recombination. Such an active layer has to relate suitably in band gap and refractive index to the other semiconductor regions of the structure in order to achieve a suitable degree of "confinement" of these processes to the active layer. The layers of material to either side of the waveguide region and in contact with

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the opposite faces of the waveguide region are known as "confinement layers".

5 A major field of application of semiconductor optical devices is in optical fibre communications systems. In general, the devices are constructed out of materials whose elemental components are selected from Groups III and V of the Periodic Table. Silica optical fibres as produced in recent years have loss minima at 1.3 μm and 1.55 μm approximately, the latter minimum being the lower. Accordingly, there is an especial need for devices 10 operating in the range from 1.1 to 1.65 μm , especially from 1.3 to 1.6 μm . (These wavelengths, like all the wavelengths herein except where the context indicates otherwise, are in vacuo wavelengths). Semiconductor 15 lasers operating in this region of the infrared usually comprise regions of indium phosphide, InP, and of quaternary materials indium gallium arsenide phosphides, $\text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$. By suitable choices of x and y it is possible to lattice-match the various regions while 20 varying the band gaps of the materials. (Band gaps can be determined experimentally by, for example, photoluminescence). Additionally, both indium phosphide and the quaternary materials can be doped to be p - or n-type as desired.

25 Describing a selected BH semiconductor laser, with its mesa uppermost, it has an active layer within the mesa. Electrical contacts are provided to the mesa and on the furthestmost face of the substrate from the mesa. The "confinement" required is provided optically in a vertical 30 direction, by changes in refractive index of the

semiconductor material, and both optically and electrically in a horizontal direction by the confinement layers. The confinement layers act to cause any current flowing between the contacts to flow preferentially through the mesa and therefore through the active layer. In one form, the confinement layers may present non-conducting semiconductor junctions to current flow between the contacts in use of the device.

Good electrical confinement is provided if the semiconductor layers between the contacts constitute a p-n junction and the confinement layers in combination with the substrate constitute an n-p-n junction when taken in the same direction. In use the confinement layers and substrate then comprise a reverse biased semiconductor junction in both directions. Alternatively the confinement layers and substrate could present multiple reverse biased semiconductor junctions in one or both directions.

In another form, the confinement layers may comprise "semi-insulating" materials such as Fe doped InP. These materials have a relatively high resistivity compared to for instance undoped InP. Confinement layers in this form have advantages in that they substantially completely oppose current flow and show low capacitance effects. Low capacitance effects tend to increase device speed.

In the past devices of this type have been fabricated by means of liquid phase epitaxy (LPE). However there are problems associated with these techniques such as solutal convection within the melts, inaccurate thickness control of the confinement layers and meltback of the mesas during fabrication. These have lead in particular to lack of uniformity over large areas and the techniques do not lend themselves easily to large scale production.

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In an attempt to solve the problem of meltback of the mesas during fabrication an LPE-VPE (vapour phase epitaxy) hybrid technique has been used. However there are still disadvantages. It retains an LPE growth step and therefore does not lend itself to large scale production, a significant leakage current has been observed in the confinement layers, and narrow mesas are difficult or impossible to achieve.

An alternative growth technique, metal organic vapour phase epitaxy (MOVPE), has been found promising for large scale device production. It offers a highly desirable combination of features : atomic scale interface abruptness, precise compositional control, and uniformity of thickness and composition over a large area.

Additional alternative growth techniques which have also been found advantageous in epitaxial fabrication processes are molecular beam epitaxy (MBE) and metal organic molecular beam epitaxy (MOMBE).

A method of fabricating buried mesa structure lasers using only low pressure "metalorganic chemical vapour deposition" (LP-MOCVD) epitaxial growth steps is outlined in the following paper : "Very Low Threshold Buried Ridge Structure Lasers Emitting at 1.3 μ m Grown by Low Pressure Metalorganic Chemical Vapour Deposition" by M Razeghi et al, Applied Physics Letters, 46 (2) (15.1.85) pages 131-133. (MOCVD is an alternative term for MOVPE.) The method comprises the steps of growing onto an InP substrate, an n-doped InP buffer layer, an undoped GaInAsP active layer, and a p-doped InP layer for avoiding the formation of defects near the active layer during etching. Etching using a mask, the active layer is reduced to a mesa. After removing the mask, the mesa is covered by a p-doped InP layer and a p-doped GaInAs cap layer.

All the growth steps of the above method are performed by low pressure MOVPE and hence large scale production should be facilitated. Further it is particularly convenient since only one growth technique must be employed. However, the devices produced rely on a built-in potential difference between the large area p-n homo-junctions to each side of the active region and the p-n heterojunction through the relatively small area active region itself. Although a lowest measured threshold current of 11 mA using continuous wave operation has been quoted, the values given for measurements relating to 269 devices were variable in the range from 17.9 mA to 50.0 mA inclusive. 44% of these devices had a threshold current of more than 45 mA. An optical power emission of only up to 15 mW is quoted, and current blocking on either side of the mesa had to be improved by proton bombardment to the depth of the p-n junction and beyond. Such bombardment is not easy to carry out with satisfactory results.

It is an object of the present invention to provide an improved semiconductor structure and a method of manufacture therefor.

Hereinafter, structures and devices may be described in terms, such as "uppermost", which imply a specific orientation of the structure or device. The use of such terms is for convenience of description only and should not be taken to limit any structure or device to a specific orientation.

According to a first aspect of the present invention there is provided a semiconductor structure, comprising a substrate having epitaxial layers deposited thereon, there being an interface which extends in a generally transverse direction with respect to the face of the substrate,

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between first and second regions of the layers, wherein at least a major portion of the interface corresponds at least substantially to a (111) B crystallographic plane of the material or materials of the first region, the layers of the first and second regions being at least substantially flat right up to the interface.

It has been found that, surprisingly, it is possible to grow layers in the second region, against such an interface, which tend to show no significant change in depth even immediately adjacent the interface. This means that relatively good control may be exercised over the positions of, for instance, transitions from one layer to the next in the first and second regions, even at the interface. Hence the relative positions of semiconductor junctions can be better controlled at the interface if layers of each region are appropriately doped.

Particularly advantageously, it has been found that such semiconductor structures can be fabricated using MOVPE growth techniques, having the advantages described above.

It has been thought that the layers referred to grow so flat against the interface because of the phosphorous-rich nature of (111) B crystallographic planes of InP. However it has further been found, surprisingly, that the major portion of the interface may correspond to modified (111) B crystallographic planes without significantly affecting the flat characteristic of the layers in the second region. This can be particularly advantageous in the fabrication of some semiconductor structures where for instance an improved device can be made by a technique incorporating a heating step which causes material transport at the interface before the layers of the second region are grown. An example of such



a device can be a buried heterostructure laser. A technique incorporating a heating step, and a semiconductor structure made by the use of the technique, is described below. (The heating step acts to "clean up" the sides of a mesa so that improved growth of confinement layers against the mesa occurs, in spite of the treatment history of the mesa before growth.)

The term "modified (111) B crystallographic plane" means that the major portion of the interface has been fabricated by exposing a (111) B crystallographic plane in the material of the first region, then subsequently modifying the plane, for instance by heat treatment causing material transport, so that it no longer accurately represents a (111) B crystallographic plane. However, the interface will retain general characteristics of the (111) B crystallographic plane, for instance the overall direction of slope and the characteristic interaction with certain growth techniques, particularly MOVPE, which allows the layers in the second region to grow relatively evenly, right up to the interface.

Preferably the major portion of the interface comprises of the order of 60⁰%, or more preferably of the order of 80⁰%, of that interface. Also preferably, said major portion should comprise parts of the interface both adjacent to, and furthest from the substrate. Both these preferred features tend to encourage a generally flat characteristic of the layers grown against the interface.

According to a second aspect of the present invention there is provided a semiconductor structure, comprising a substrate having a mesa supported by a face thereof, the mesa comprising a p-n junction which extends parallel to the face of the substrate, the lateral surfaces of the mesa being buried by one or more confinement layers,



wherein at least a major proportion of the lateral surfaces of the mesa correspond at least substantially to (111) B crystallographic planes of the material or materials of the corresponding part or parts of the mesa.

5 Semiconductor structures according to the second aspect of the present invention are particularly useful in buried heterostructure lasers.

Because semiconductor material such as InP can be used to grow surprisingly flat confinement layers against the lateral surfaces of such a mesa, for instance by means of MOVPE, the depth and positional relationship of the layers to a mesa can be relatively closely controlled. This is particularly important where the mesa contains a p-n junction and the confinement layers present an n-p junction to block current flow in use of a device. It can also be advantageous for subsequent steps in fabrication of a device.

As before, the (111) B crystallographic planes may be modified, for instance by heat treatment causing material transport.

It has been found that, as mentioned above, if the mesa incorporates an active layer of a device, the device may be improved by heating the structure, before growth of confinement layers against the lateral surfaces, so as to cause material transport onto the sides of the active layer. This is preferable to growing the confinement layers against the sides of the active layer directly after etching those sides, producing for instance a device with more reliable performance characteristics.

30 According to a third aspect of the present invention there is provided a method of making a semiconductor structure according to the first aspect of the present invention which comprises the stages of:

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f) etching a wafer of semiconductor material to create a step having a rising surface, corresponding to the interface, at least a major portion of which surface comprises (111) B crystallographic planes of the material, and

ii) growing semiconductor material by means of any one of a MOVPE, a MBE or a MOMBE technique to create the layer or layers of the second region.

The method may further comprise a stage in which the (111) B crystallographic planes are modified, for instance by heating to cause material transport at the interface, before the growth of the semiconductor material. To prevent growth on the layer or layers of the first region, an epitaxial growth suppressing material may be deposited on that layer or layers prior to stage ii) above.

According to a fourth aspect of the present invention there is provided a method of making a semiconductor structure according to the second aspect of the present invention which comprises the steps of:

- i. forming a stripe of an epitaxial growth suppressing material on a heterostructure wafer;
- ii. using the stripe as a mask, etching a mesa with an etchant or a selection of etchants such that at least a major proportion of the lateral surfaces of the mesa comprise (111) B crystallographic planes of the material of the mesa;
- iii. using epitaxial growth to grow the confinement layers against the lateral surfaces of the mesa; and
- iv. removing the stripe.

An important application of the present invention is in the production of lasers, particularly those which will operate in a single transverse mode. These lasers are of major importance in optical communication systems. Such

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lasers can be produced from semiconductor structures made by the method of the present invention in which the uppermost surface of the mesa is restricted to being not more than 5 μm wide.

5 Step iii. above may advantageously be preceded by a step in which the lateral surfaces of the mesa are modified by heat treatment which causes material transport at those surfaces.

10 MOVPE can be used as the epitaxial growth technique of step iv. above. This has the particular advantages already described.

15 Single transverse mode semiconductor lasers, and a waveguide, according to embodiments of the present invention will now be described, by way of example only, with reference to the accompanying Figures in which:

Figure 1 shows a vertical cross section of a laser according to a first embodiment of the present invention;

20 Figure 2 shows a cross section of part of a double heterostructure wafer for use in making the laser of Figure 1;

Figures 3a to 3f show stages in production of the laser of Figure 1;

25 Figure 4 shows a scanning electron microscope image of a cross section of a semiconductor structure according to an embodiment of the present invention;

Figures 5 and 7 show cross sections of semiconductor lasers according to second and third embodiments of the present invention;

30 Figure 6 shows a stage in the production of a laser according to an embodiment of the present invention, following an optional additional treatment step;

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Figure 8 shows a plot of the dimensions of a plurality of mesas fabricated from a common wafer according to embodiments of the present invention;

5 Figure 9 shows a longitudinal mode spectrum of a laser structure as shown in Figure 5;

Figures 10a and 10b show the far field patterns parallel and perpendicular respectively to the plane of the p-n junction of the mesa;

10 Figure 11 shows a histogram of active layer widths in mesas produced using methods according to the present invention, sampled from five different wafers; and Figure 12 shows a waveguide according to an embodiment of the present invention.

15 Figures 1 to 7, and 12, are not drawn to scale and cross hatching is omitted for the purposes of clarity.

As is the usual practice, although only one laser is shown in Figures 3a to 3f, several lasers will generally in fact be fabricated from the same wafer.

20 Referring to Figure 1, a laser structure 1 according to an embodiment of the present invention comprises a layered mesa 2, 3, 4 buried by three confinement layers 5, 6, 7, a capping layer 8 and a contact layer 9. The lateral surfaces 10 of the mesa 2, 3, 4, against which the confinement layers 5, 6, 7 have been grown, are defined by
25 (111) planes of the materials of the mesa 2, 3, 4. The resultant cross section of the mesa has a distinctive concertinalike appearance as a result.

30 In more detail, the laser structure 1 comprises a substrate 12 of (100) orientated S doped InP, doping level n approximately equal to $8 \times 10^{18} \text{ cm}^{-3}$, about 250 μm thick. Covering the upper surface of the substrate 12 is a quaternary layer 11 of S doped GaInAsP (quaternary material), doping level n of the order of $1 \text{ to } 2 \times 10^{18}$

cm^{-3} , up to about $0.2 \mu\text{m}$ thick and of a band gap lying in the range from 1.0 to $1.3 \mu\text{m}$. The layered mesa 2, 3, 4 is mounted on the quaternary material and has the following layers, starting with the lowermost:

- 5 i) an S-doped buffer layer 2 of InP, doping level n approximately equal to $2 \times 10^{18} \text{ cm}^{-3}$, $0.4 \mu\text{m}$ thick;
- ii) an undoped active layer 3 of GaInAsP of band gap $1.5 \mu\text{m}$ and $0.1 \mu\text{m}$ thick; and
- 10 iii) a Cd-doped layer 4 of InP, doping level p approximately equal to $5 \times 10^{17} \text{ cm}^{-3}$, $0.2 \mu\text{m}$ thick.

On each side of the mesa is a series of three confinement layers 5, 6, 7 as follows, again starting with the lower most:

- 15 iv) an S-doped layer 5 of InP, doping level n of the order of 1 to $2 \times 10^{18} \text{ cm}^{-3}$, of thickness $0.1 \mu\text{m}$;
- v) a Cd-doped layer 6 of InP, doping level p approximately equal to $5 \times 10^{17} \text{ cm}^{-3}$, of approximate thickness $0.4 \mu\text{m}$; and
- 20 vi) an S-doped layer 7 of InP, doping level n approximately equal to $1 \times 10^{18} \text{ cm}^{-3}$, of approximate thickness $0.4 \mu\text{m}$.

Extending across the uppermost surfaces of both the mesa and the confinement layers 5, 6, 7 is a capping
25 layer 8 of Cd-doped InP, doping level p approximately equal to $2 \times 10^{18} \text{ cm}^{-3}$, of thickness lying in the range 1 to $2 \mu\text{m}$. The capping layer 8 in turn is covered by a ternary contact layer 9 of Zn-doped GaInAs, doping level p approximately equal to $4 \times 10^{19} \text{ cm}^{-3}$, of thickness
30 lying in the range 0.05 to $0.3 \mu\text{m}$.

Contacts, for providing driving current to the laser structure, are provided through a window 13 in a silica layer 14 over the contact layer 9, and to the lowermost

surface of the substrate 12. The contacts 15, 16 and 17 comprise Ti Au tunnelling Schottky contacts applied by radio frequency sputtering and annealing. Pt may advantageously be included as a diffusion barrier between the Ti and the Au in the contact 15, 16 through the window 13. This contact configuration is known and further details are not therefore provided herein.

Referring to Figures 2 and 3a to 3f, in a method of fabricating a laser structure according to Figure 1, firstly a double heterostructure wafer is produced. The wafer (shown in Figure 2) comprises the substrate 12, the quaternary layer 11, and the layers 2, 3, 4 which are present in the mesa of the finished laser structure.

The layers 11, 2, 3, 4 are all lattice-matched to the respective layer below, being grown by MOVPE under normal growth conditions.

A silox stripe 18, 1.8 μm wide and 0.2 μm thick (shown in Figures 3a to 3e), is then produced extending in the (110) direction with respect to the crystalline structure of the substrate 12. The stripe 18 is produced by the use of the known combination of a positive photoresist mask and buffered HF as an etchant.

Etching the wafer, which comprises layers of different semi-conductor materials which must each be etched to produce the layered mesa 2, 3, 4, must be carried out using different selective etchants. The uppermost, InP layer 4 is etched using hydrobromic acid. The active layer 3 is etched using a mix of sulphuric acid, hydrogen peroxide and water. The InP buffer layer 2 is etched by again using hydrobromic acid. The actions of these etchants in this crystallographic orientation are well documented.

Alternatively the active layer 3 may be etched using a

mixture of potassium dichromate (1/6 molar), sulphuric acid, and hydrochloric acid in the ratio 3 : 1 : 1. The action of this etchant is further discussed below.

5 The hydrobromic acid etches through the uppermost InP layer 4 at a rate of about 6 μm per minute of InP at 20°C, or 2.5 μm per minute at 5°C, being stopped by the quaternary active layer 3. When the active layer 3 is reached, the etch rate drops significantly for instance by a factor of 3 or 4. Referring to Figure 3b, the
10 characteristic result at this stage is a shallow mesa profile with sides formed largely, or entirely, by (111) B planes. If the silox stripe 18 is well adhered to the InP layer 4, the planes exposed by the etchant are (111) A immediately below the silox stripe 18, then (111) B down
15 to the active layer 3. The ratio of A to B planes (in terms of the depth of the mesa showing each type of plane at this stage) has been observed to be about 1 : 4. If the silox stripe 18 is not well adhered, then the only plane exposed is generally the (111) B plane. Figure 3b
20 shows a mesa profile where the silox stripe 18 was not well adhered. In the latter case, as shown, there is a slight undercut, generally of up to 0.2 μm , of the silox stripe 18.

25 It was noted that in some cases the hydrobromic acid contained colloidal particles. These were removed by filtration.

30 Using the acid/peroxide mixed etchant, the active layer 3 is then etched. The mixed etchant etches at a rate of 0.4 μm per minute and is stopped by the InP buffer layer 2. Referring to Figure 3c, the sidewalls of the active layer 3 are characteristically etched to expose (111) A planes by this process. Hence at this stage a mesa has been formed which has an angular "bulge" in its sidewalls.

As mentioned above, the active layer 3 can alternatively be etched using a dichromate acid etchant. This etchant has the advantages of etching all wavelengths of quaternary material between InGaAs and InP, and of
5 etching the active layer 3 only relatively slowly in a lateral direction once the (111) A plane has been exposed. Because of the latter feature, over etching of the active layer 3 does not cause deep undercutting of the uppermost InP layer 4. It has been found that the
10 dichromate/acid etchant etches quaternary material of emission wavelength $1.5\ \mu\text{m}$ at a rate of about $0.8\ \mu\text{m}$ per minute in a downwards direction at 5°C . However the etch time for the active layer 3 in the present case has been found to tend to be variable where there is lattice
15 mismatch in the double heterostructure wafer. An etch time of 60 secs is used to ensure complete clearance of the active layer 3. (If the active layer 3 comprises a quaternary material having a band gap of $1.3\ \mu\text{m}$, then an etch time of 10 mins has been found suitable).

20 Reverting to hydrobromic acid as the etchant, the InP buffer layer 2 is then etched until the quaternary layer 11 which covers the substrate 12 stops the action of the etchant. Referring to Figure 3d, the resultant layered mesa 2, 3, 4 has the characteristic concertinalike
25 appearance referred to above. If the active layer 3 has been overetched, this final etching step has been found to cut the uppermost InP layer 4 back rapidly, but only as far as the top corner of the (111) A plane in the active layer 3. Hence the same mesa 2, 3, 4 profile is achieved,
30 though the degree of overetching will affect the mesa width.

It has been noted that during the final etching step, the active layer 3 appears to act as a strongly adherent

mask and the InP buffer layer 2 is at first etched along (111) A planes before the (111) B plane reasserts itself. This means that the angle produced in the mesa sidewall by the transition from A back to B planes does not coincide with the interface between the active and buffer layers 3, 2. This can be seen for instance in figure 3d.

After etching of the layered mesa 2, 3, 4, the three confinement layers 5, 6, 7 are grown in. The action of the silox stripe 18 during this stage is to suppress growth of InP. Referring to Figure 3e, the result is that the confinement layers 5, 6, 7 grow either side of the mesa leaving the silox stripe 18 exposed.

Growth conditions for the confinement layers are generally as are normal for MOVPE growth but before growth starts, the sample is heated to 700°C for 20 minutes in the presence of PH₃. This treatment has been found to enhance the action of the silox as a MOVPE growth-suppressing material even when the silox stripe is reduced in width for instance to values as low as about 1 um. Further, the heating involved appears to allow surface reconstruction to occur which improves the morphology of subsequently grown epitaxial layers. This surface reconstruction can be significant, modifying the lateral surfaces of the mesa by means of material transport particularly at the base of the mesa, and onto the exposed surfaces of the active layer. The concentration of PH₃ should be high enough to prevent incongruous evaporation of the InP. The period for which the sample must be heated in the presence of PH₃ will vary according to the conditions applied. For instance, if the concentration of PH₃ is increased, the period may be reduced.

Where the uppermost InP layer 4 had been etched so as to undercut the silox stripe 18, it was noted that high device yields were achieved. This was because the silica overhang forces the confinement layers to "wing", or flare away, from the bottom surface of the silox stripe 18.

Consequently few overgrowth bridges occur, where the confinement layers meet above the silox stripe 18. Such winging occurs even in the absence of an overhang but it is enhanced where an overhang is present.

Referring to Figure 3f, when the confinement layers 5, 6, 7 are complete, the silox stripe is removed in a 40% aqueous solution of HF and the capping and contact layers 8, 9 are grown, again by MOVPE.

Referring to Figure 4, it is possible to see, using a scanning electron microscope, that significant mass transport may take place onto the sides of the active layer in a mesa during the heating step prior to growing the confinement layers.

To complete the laser as shown in Figure 1, the contacts 15, 16, 17 are applied by conventional techniques. It can then be conveniently mounted on a heat sink (not shown) by soldering the heat sink to the Au layer of the contact 15, 16.

The laser described above with reference to Figures 1 to 3f has a number of advantageous features. Firstly, the confinement layers 5, 6, 7 tend to grow in substantially planar, particularly at a distance down the lateral surfaces of the mesa 2, 3, 4 of more than 0.5 μm from the silox stripe 18. Further, as mentioned above, the uppermost confinement layer 7 tends to "wing" away from the silox stripe 18, leaving a wide opening which gives good access for subsequent removal of the stripe 18. The capping and contact layers 8, 9 tend to grow with a planar

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characteristic which facilitates heat sinking and, also, at least two semiconductor junctions are grown by consecutive growth steps into the confinement layers 5, 6, 7. This avoids having junctions coincident with layer interfaces which have been chemically degraded for instance by the use of etchants.

Particularly advantageous is the novel use of a first quaternary layer 11, independent of the active layer 3, on the substrate 12. This acts as a stopping layer to the etchant used to etch the lowermost mesa layer 2. It also acts to prevent breakdown, even at large gate currents, of the p-n-p-n thyristor-like structure of the confinement layers 5, 6, 7 in combination with the capping layer 8. As a result leakage currents are blocked which would otherwise bypass the active region of the laser in use. By using a first quaternary layer 11 which is independent of the active layer 3, its characteristics such as band gap are not tied to those of the active layer 3. By reducing the bandgap, for instance to values in the range 1.0 to 1.3 μm as described above, the effectiveness of the first quaternary layer 11 in preventing leakage currents may then be improved.

The first quaternary layer 11 has even a third function, as part of the waveguiding structure of the laser. As long as the buffer layer 2 of the mesa is sufficiently thin, the first quaternary layer 11 can "dilute" the lateral refractive index step at the sides of the mesa, allowing wider mesas with the same mode cut-off properties. This is desirable for processing, device resistance and radiation beam width reasons. In addition the first quaternary layer 11 could have distributed feedback (DFB) gratings etched into it, planar growth being resumed to deposit the layers 2, 3 and 4 of the

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mesa. (Again the buffer layer 2 should be relatively thin, say from 0.1 to 0.5 μm thick, to allow the desired degree of optical interaction).

5 The use of a first quaternary layer in a semiconductor laser structure, independent of the active layer, lying above the substrate and extending below the mesa, may be found advantageous more generally than in structures of the type described in the present specification.

10 Referring to Figure 5, variations may be made in the layers of the laser structure. For instance the first quaternary layer 11 may be left out and a deeper buffer layer 2 used, the layered mesa 2, 3, 4 extending only partially down into the buffer layer 2. The final etching step, in which the buffer layer 2 is etched, will then
15 have to be controlled by timing rather than by relying on the action of the first quaternary layer 11 as a stopping layer.

Referring to figure 6, it has been found advantageous to "notch" the active layer 3 immediately before heating
20 and growth of the confinement layers. An etchant which attacks only the active layer 3, and which selectively exposes the (111) A planes, is used to narrow the active layer 3 preferentially. A suitable etchant comprises sulphuric acid, hydrogen peroxide, and water in the ratio
25 3:1:1. This "notching" of the active layer 3 is believed to provide a clean, fresh surface on the side of the active layer 3, which benefits the subsequent process steps.

30 Other variations may be that the unetched thickness of the buffer layer 2 may conveniently range up to 4 μm , and the height of the layered mesa 2, 3, 4 may be as much as 1.4 μm . Different dopants and doping levels may be used, such as Zn instead of Cd in the uppermost layer 4 of the mesa, doped to a level of $2 \times 10^{18} \text{ cm}^{-3}$ instead of $5 \times 10^{17} \text{ cm}^{-3}$.

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The second of the confinement layers 6 may comprise a "semi-insulating" material such as Fe doped InP instead of the p-doped InP referred to above. Such a material tends to have a relatively high resistivity.

5 The silox stripe 18 might be replaced by a stripe of different material, such as a different form of silica, or another dielectric material such as Si_3N_4 or alumina.

10 Referring to Figure 7, an additional p-doped layer 19 of InP may be grown onto the confinement layers 5, 6, 7. This avoids coincidence between the uppermost p-n junction provided by the confinement layers 5, 6, 7 and a chemically treated interface such as the interface between the confinement layers and the capping layer 8, which may be degraded during removal of the silox stripe 18.

15 The detailed growth of InP confinement layers by MOVPE against a layered mesa 2, 3, 4 of the type shown in Figure 5 has been investigated by growing alternating layers of p- and n-doped InP and using a scanning electron microscope (SEM) to obtain images of the layers. It was
20 noted that there were no voids on the sides of the mesa, or under the overhang of the silox stripe 18 at least for an overhang of up to $0.2 \mu\text{m}$. The most interesting feature was the growth of the confinement layers parallel to the (100) plane. Only when the confinement layers were
25 approaching within $0.2 \mu\text{m}$ of the silox stripe 18 did they begin to thicken preferentially at the points of contact with the mesa sidewalls.

30 Referring to Figure 8, the uniformity of a plurality of mesas produced on a single wafer was investigated by taking a cleave from one end of the wafer and examining mesa dimensions using an SEM. The approximate size of the wafer was $10\text{mm} \times 12\text{mm}$. All of the mesa dimensions were found to have been controllable to within $0.1 \mu\text{m}$. The

wafer was subsequently overgrown with confinement layers and only an insignificant number of bridges of the silox stripes could be visually observed.

5 Lasers fabricated according to embodiments of the present invention have produced up to 50 mW under direct current (dc) operation. The electrical characteristics have shown no appreciable conduction of current through the confinement layers due to mesa or overgrowth defects.

10 Referring to Figure 9, a longitudinal mode spectrum of a laser of the type shown in Figure 5, using n-, p- and n-doped confinement layers 5, 6, 7, has been found to show a smooth envelope of modes and no evidence of higher order transverse modes.

15 Referring to Figures 10a and 10b, far field spectra from such a laser have been found to show a full width at half maximum (fwhm) of 24° for the parallel direction and 30° for the perpendicular direction, with reference to the plane of the active layer. The far field spectra were also relatively smooth. It is considered that the smooth condition of the mesa sidewalls led to the smoothness of the far field spectra.

20 Referring to figure 11, the width of the active layer was measured in 80 different mesas, produced over five different wafers. Using silox stripes of $2.0\ \mu\text{m}$ and $1.85\ \mu\text{m}$ width, the active layer widths ranged from $1.4\ \mu\text{m}$ to $1.9\ \mu\text{m}$, with one active layer width lying in the range from $1.9\ \mu\text{m}$ to $2.0\ \mu\text{m}$. The active layer widths achieved on each wafer are shown as a histogram on Figure 11, differentiated as indicated by the markings within the columns of the histogram.

30 Although the embodiments of the present invention described above are fabricated using MOVPE, this could be replaced by MBE or MOMBE, although some changes in process conditions might then be necessary.

Referring to Figure 12, semiconductor structures other than lasers can be fabricated as embodiments of the present invention. As shown in the Figure, instead of a mesa, a channel might be created, the sides 20 of the channel being provided by (111) B crystallographic planes. If material is subsequently grown into the channel in layers having a substantially flat characteristic almost right up to the sides 20 of the channel, then a particularly useful waveguiding structure can be created.

The material grown into the channel may comprise a quaternary, InGaAsP, and the material into which the channel is created may comprise InP.

Other semiconductor structures which could beneficially be made according to embodiments of the present invention are optical detectors and opto-electronic integrated circuits (OEICS).

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CLAIMS

1. A semiconductor structure, comprising a substrate having epitaxial layers deposited on a face thereof, there being an interface which extends in a generally transverse direction with respect to the substrate, between first and second regions of the layers, wherein at least a major portion of the interface corresponds at least substantially to (111) B crystallographic planes of the material or materials of the first region, the layer or layers of the first and second regions being at least substantially flat right up to the interface.

2. A semiconductor structure according to claim 1, wherein the major portion of the interface corresponds to modified (111) B crystallographic planes of the material or materials of the first region.

3. A semiconductor structure according to either one of claims 1 or 2, wherein the major portion of the interface is at least of the order of 60% of the area of the interface.

4. A semiconductor structure according to either one of claims 1 or 2 wherein the major portion of the interface is at least of the order of 80% of the area of the interface.

5. A semiconductor structure according to any one of the preceding claims, wherein the major portion of the interface comprises parts of the interface adjacent to and furthest from the substrate.

6. A semiconductor structure comprising a substrate having a mesa supported by a face thereof, the mesa comprising a p-n junction which extends parallel to the face of the substrate, the lateral surfaces of the mesa being buried by one or more confinement layers, wherein at

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least a major proportion of the lateral surfaces of the mesa is provided by (111) crystallographic planes of the material or materials of the corresponding part or parts of the mesa.

- 5 7. A semiconductor structure according to claim 6, wherein the crystallographic planes comprise a (111) B crystallographic plane.
8. A semiconductor structure according to claim 6, wherein the major proportion of the lateral surfaces of the mesa is provided by modified (111) B crystallographic planes of the material or materials of the corresponding part or parts of the mesa.
- 10 9. A semiconductor structure according to any one of claims 6 to 8, wherein the material of the corresponding part or parts of the mesa is InP.
- 15 10. A semiconductor structure according to any one of claims 6 to 9, wherein the material of the confinement layer or layers comprises InP.
11. A semiconductor structure according to any one of claims 6 to 10, wherein the confinement layer or layers are grown by MOVPE.
- 20 12. A semiconductor structure according to any one of claims 6 to 11, wherein the p-n junction lies in or adjacent to an active layer in the mesa.
- 25 13. A semiconductor structure substantially as described hereinbefore with reference to any one of Figures 1 to 7 of the accompanying drawings.
14. A semiconductor laser comprising a semiconductor structure according to any one of the preceding claims.
- 30 15. A semiconductor laser structure comprising a substrate having a mesa supported by a face thereof, the mesa incorporating an active layer of quaternary material, the lateral surfaces of the mesa being buried by confinement

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layers which provide to each side of the mesa at least one current blocking semiconductor junction, wherein a second layer of quaternary material extends over the face of the substrate beneath the mesa and the confinement layers.

5 16. A semiconductor laser structure according to claim 15, wherein the band gap of the second layer of quaternary material is lower than the band gap of the active layer.

10 17. A semiconductor laser structure substantially as described hereinbefore with reference to Figures 1 to 3 of the accompanying drawings.

18. A method of making a semiconductor structure which comprises the stages of:

15 i) etching a wafer of semiconductor material to create a step having a rising surface, at least a major portion of which rising surface comprises a (111) B crystallographic plane of the material of the wafer; and

20 ii) preferentially growing semiconductor material by means of any one of a MOVPE, a MBE or a MOMBE technique onto the etched surface of the wafer, to meet the rising surface of the step.

25 19. A method according to claim 18, wherein stage i) is carried out using a mask of an epitaxial growth suppressing material to create the step, the mask being subsequently used to achieve the preferential growth of stage ii).

20. A method according to either one of claims 18 or 19 which further comprises a stage in which the (111) B crystallographic plane is modified prior to stage ii).

30 21. A method of making a semiconductor structure which comprises the steps of:

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- 5 i forming a stripe of an epitaxial growth
 suppressing material on a heterostructure
 wafer;
- ii using the stripe as a mask, etching a mesa
 with an etchant or a selection of etchants
 so as to expose (111) B crystallographic
 planes over at least a major portion of the
 lateral surfaces of the mesa;
- 10 iii using epitaxial growth to grow confinement
 layers against the lateral surfaces of the
 mesa; and
- iv removing the stripe.
22. A method according to claim 21 which further comprises
15 the step of modifying the exposed (111) B crystallographic
 planes by heat treatment sufficient to cause material
 transport at the lateral surfaces of the mesa, prior to
 step iii.
23. A method according to either one of claims 21 or 22,
20 wherein the stripe comprises a MOVPE growth suppressing
 material and the confinement layers are grown by MOVPE.
24. A method according to claim 23, wherein the
 semiconductor structure comprises a structure according to
 any one of claims 1 to 13.
25. A method of making a semiconductor structure
25 substantially as described hereinbefore with reference to
 any one of figures 1 to 7 of the accompanying drawings.
- 30

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ABSTRACT

SEMICONDUCTOR STRUCTURES AND A METHOD OF
MANUFACTURING SEMICONDUCTOR STRUCTURES

In a semiconductor buried heterostructure laser, having a
5 mesa 2, 3, 4 and confinement layers 5, 6, 7 on a substrate
12, at least the lowermost of the confinement layers 5, 6,
7 is substantially planar up to the mesa. This is
achieved by MOVPE growth of InP against lateral surfaces
of the mesa 2, 3, 4 which are defined by distinct
10 crystallographic planes of the material of the mesa. In
particular (111) B InP planes are used. The laser is
particularly for use in the field of optical
communications.

15 **FIGURE 1**

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Fig. 1.

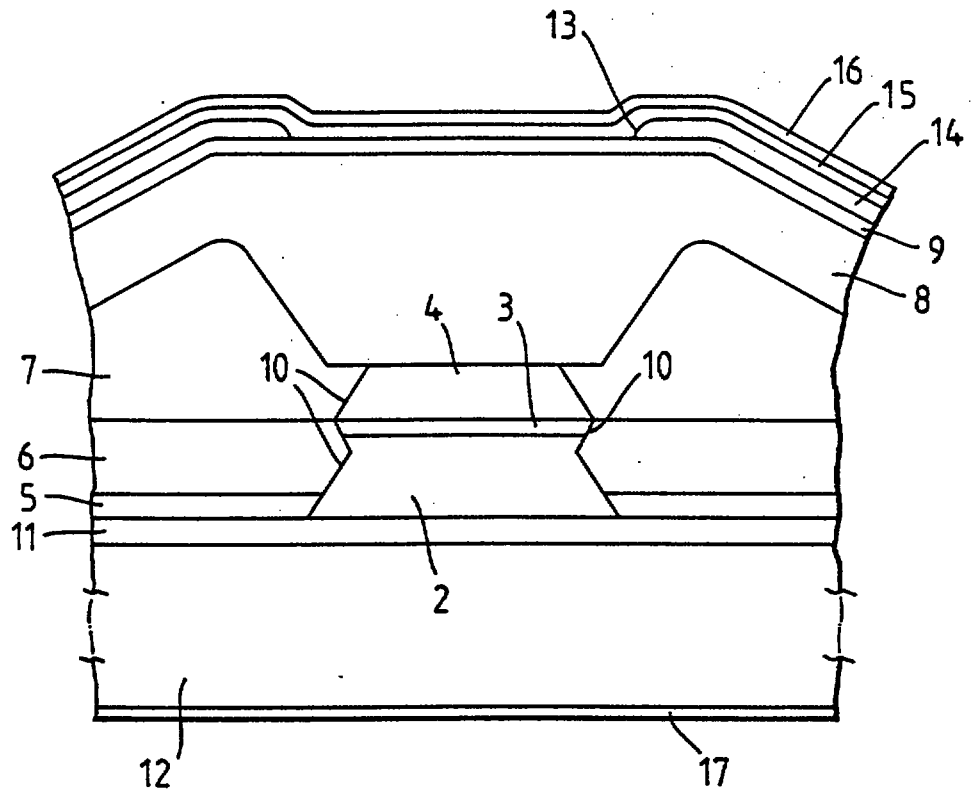
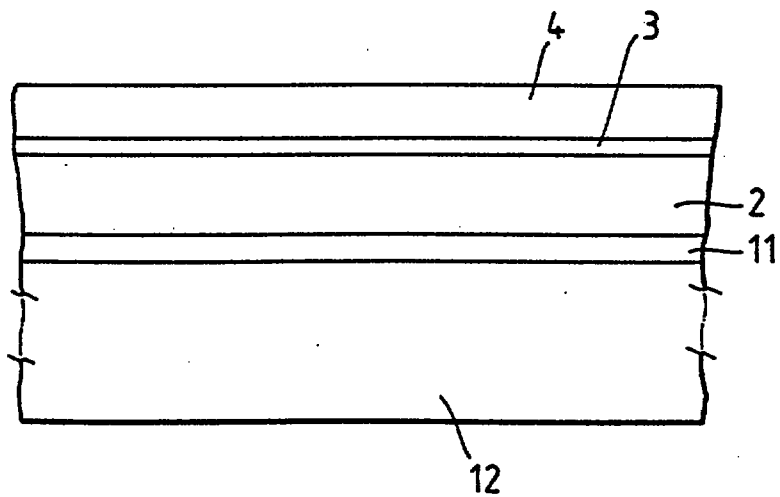
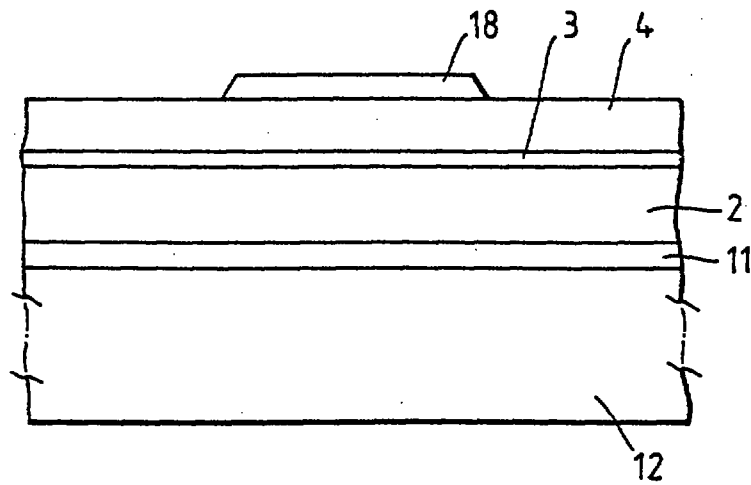
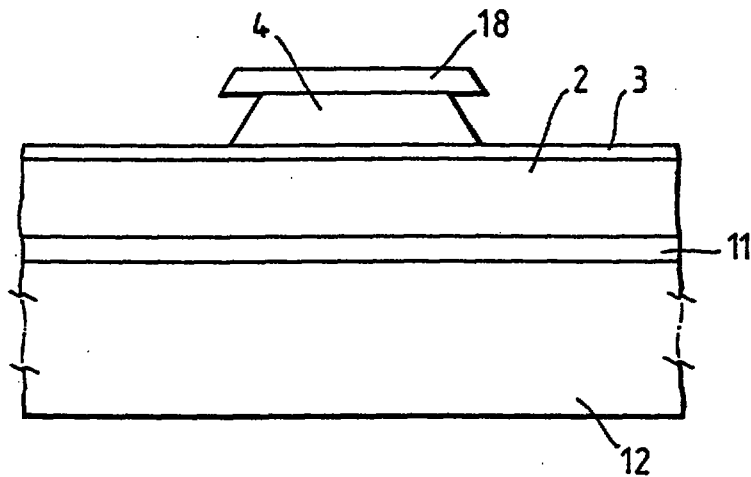
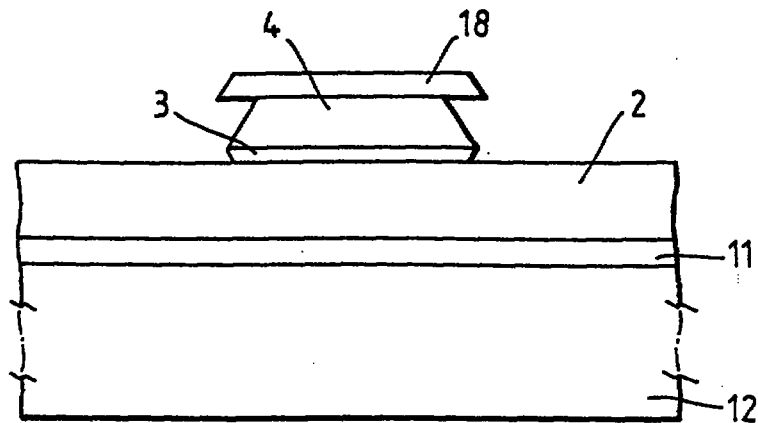


Fig. 2.



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Fig. 3a.*Fig. 3b.**Fig. 3c.*

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Fig. 3d.

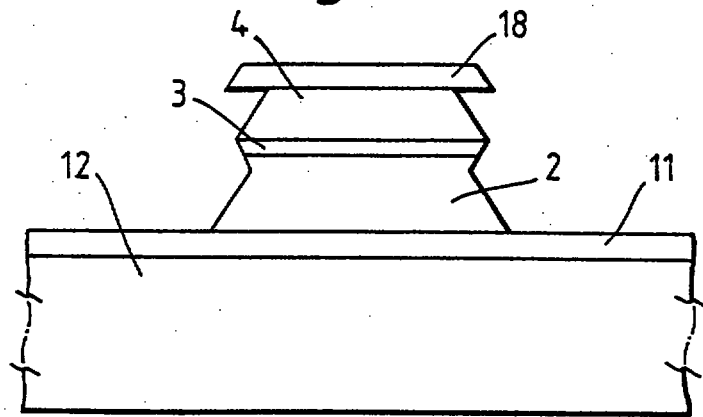


Fig. 3e.

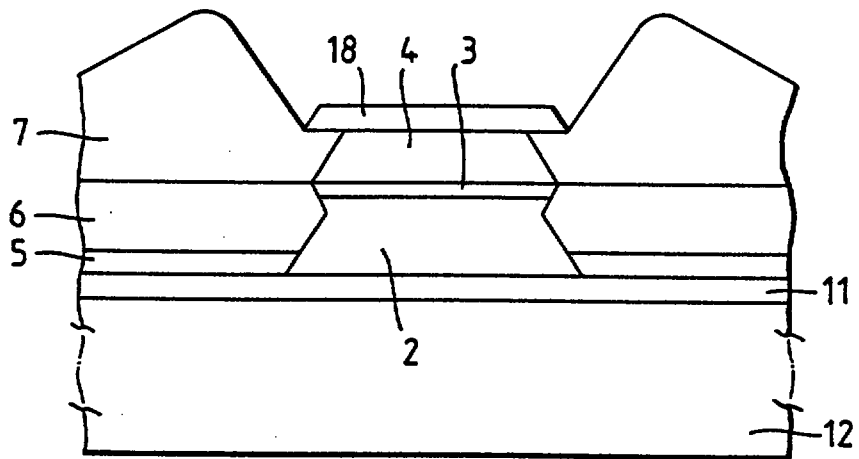
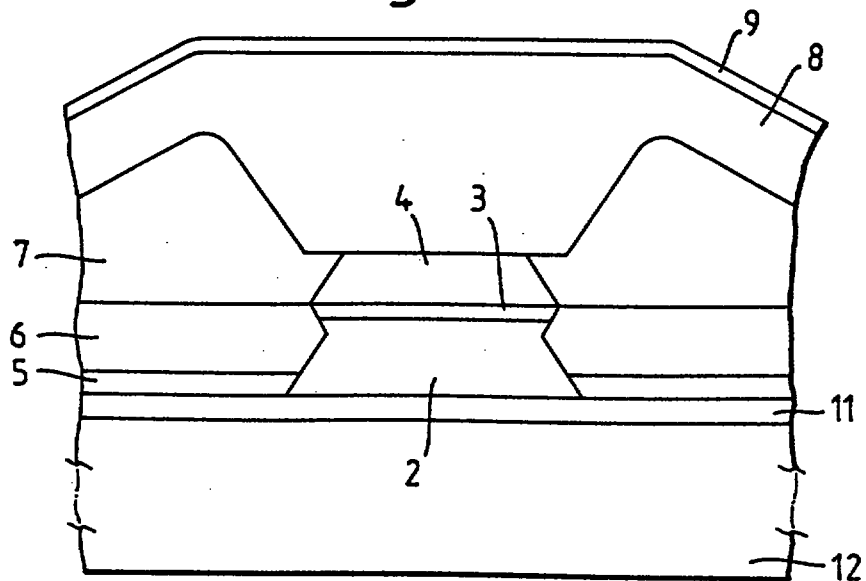


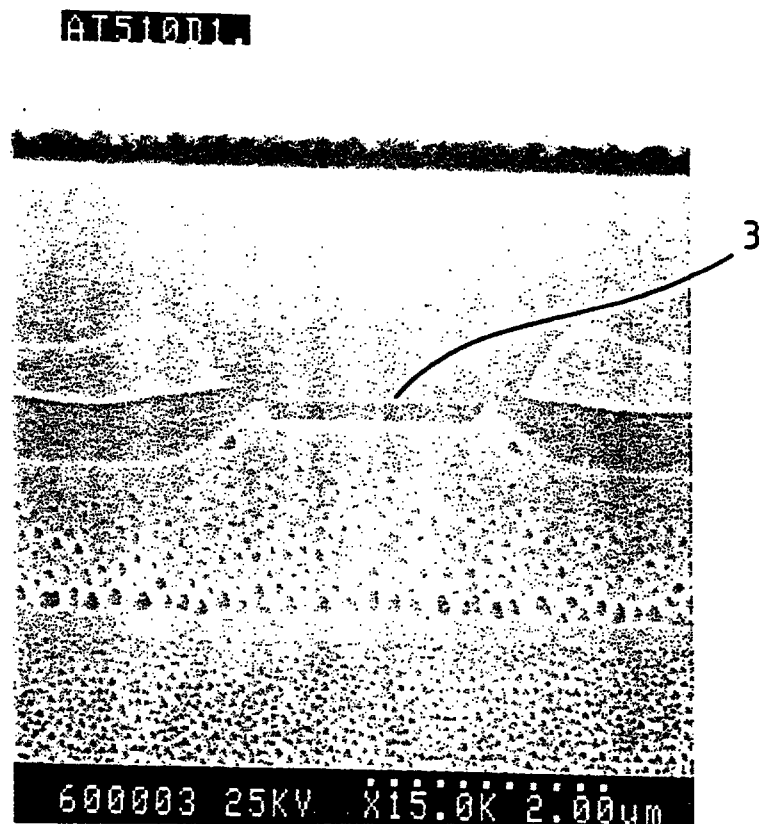
Fig. 3f.



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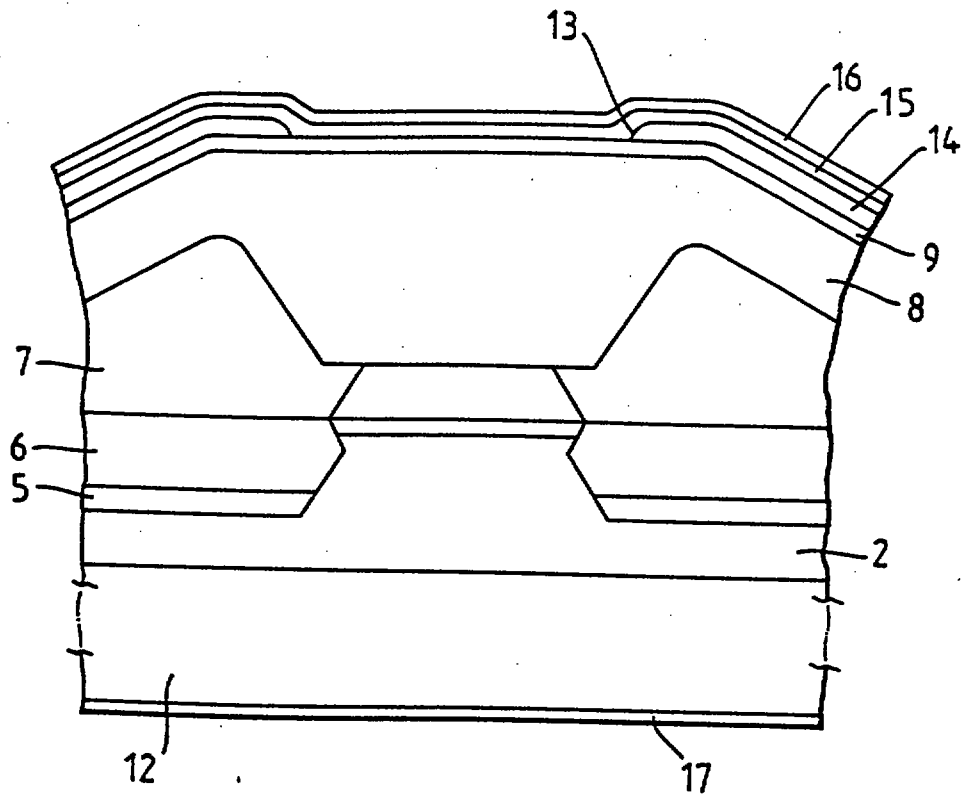
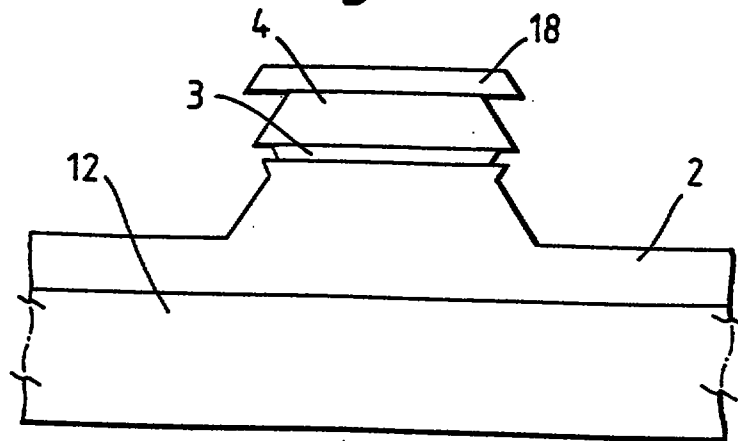
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Fig.4.



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Fig.5.*Fig.6.*

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Fig. 7.

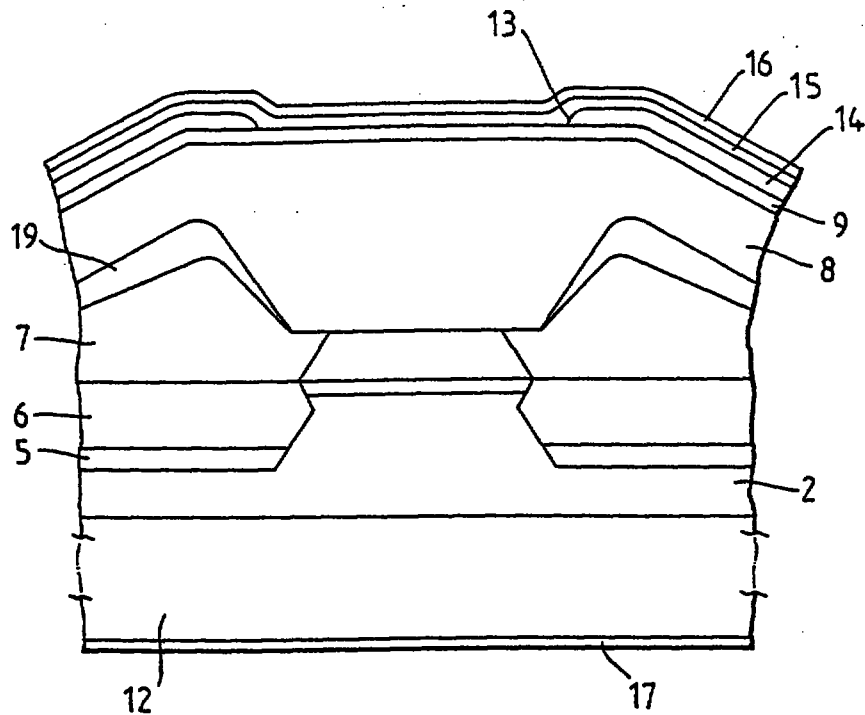
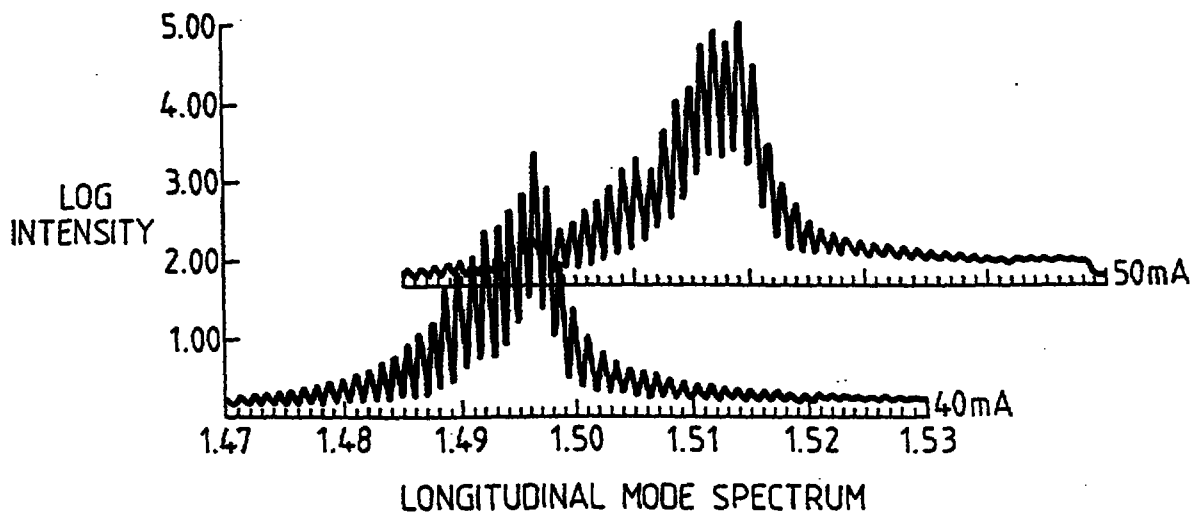


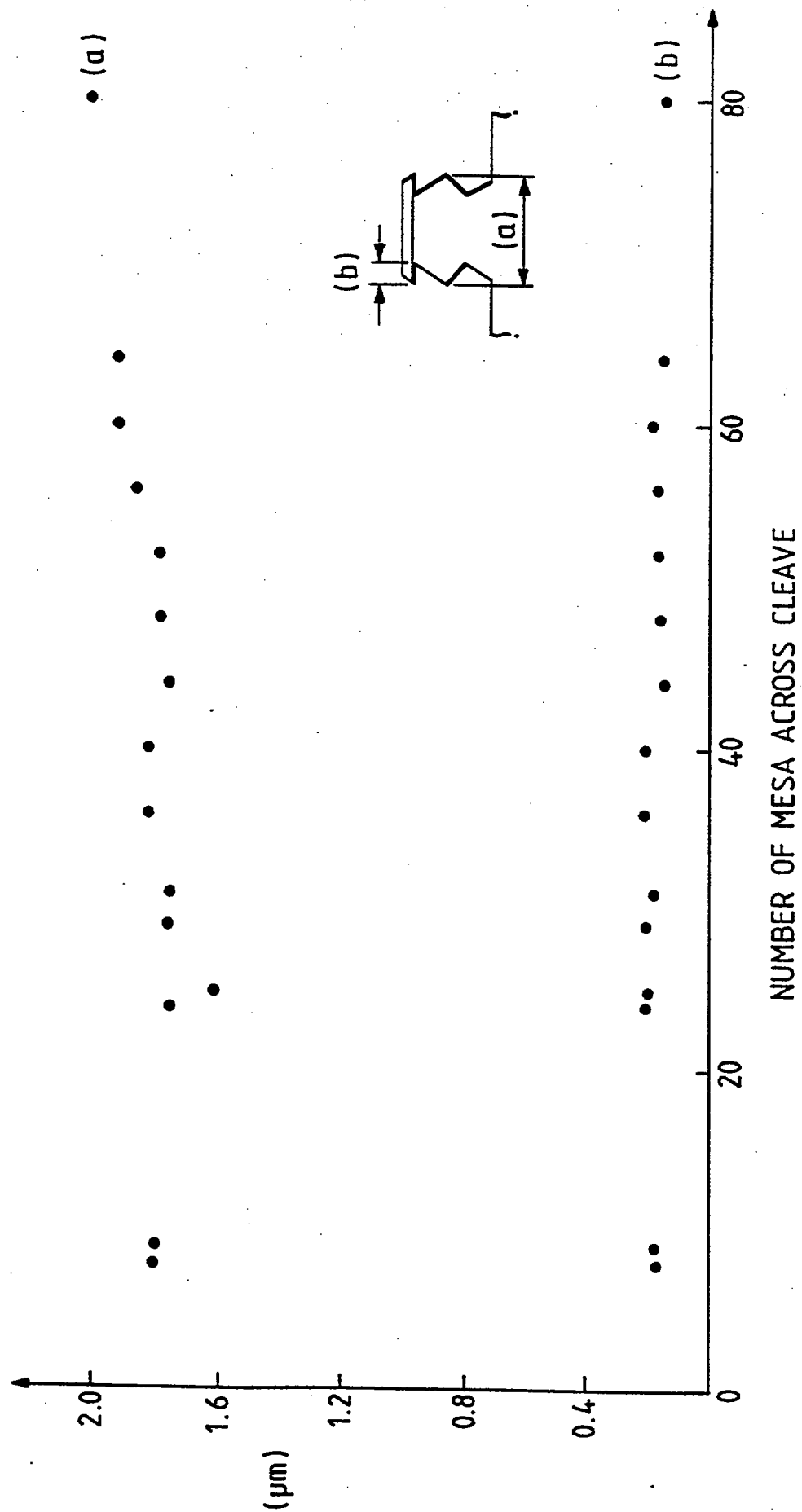
Fig. 9.



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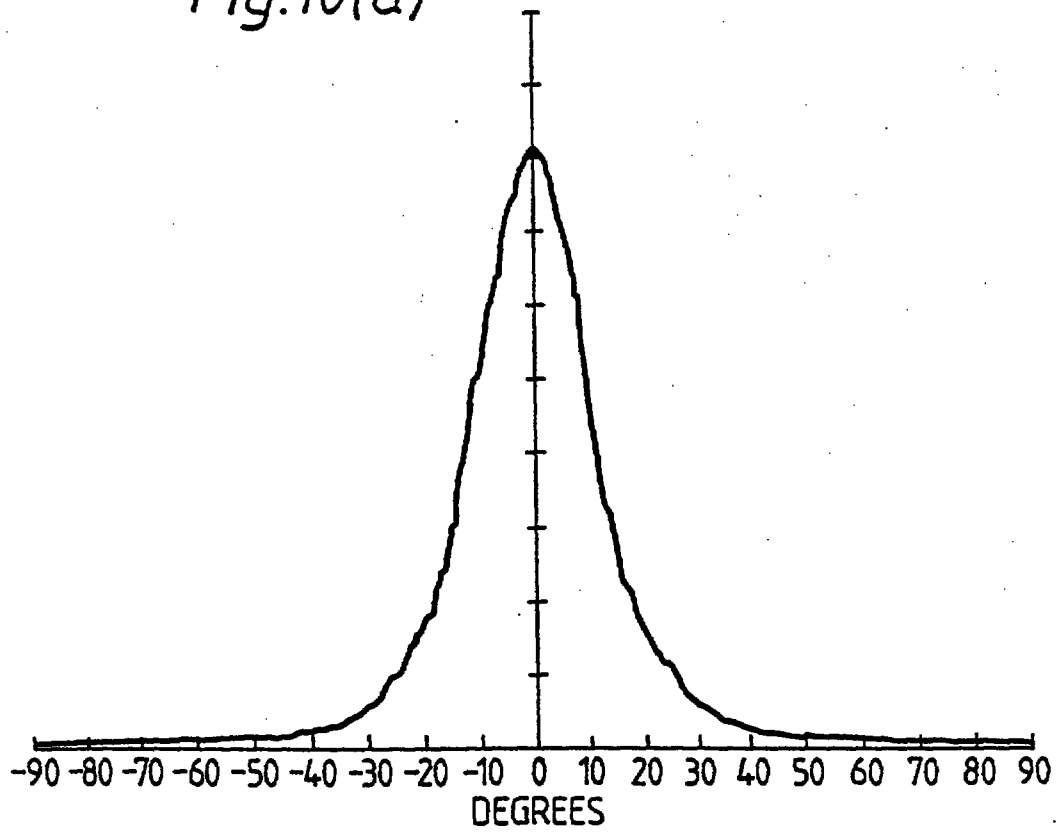
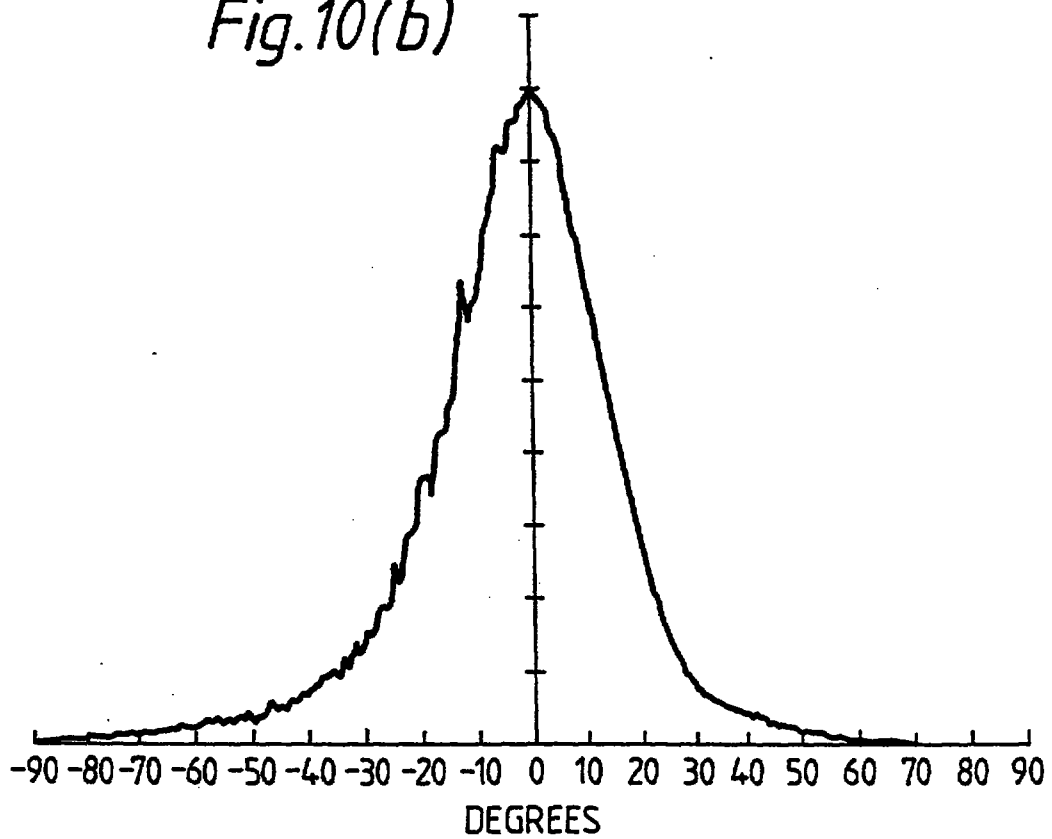
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Fig.8.



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Fig.10(a)*Fig.10(b)*

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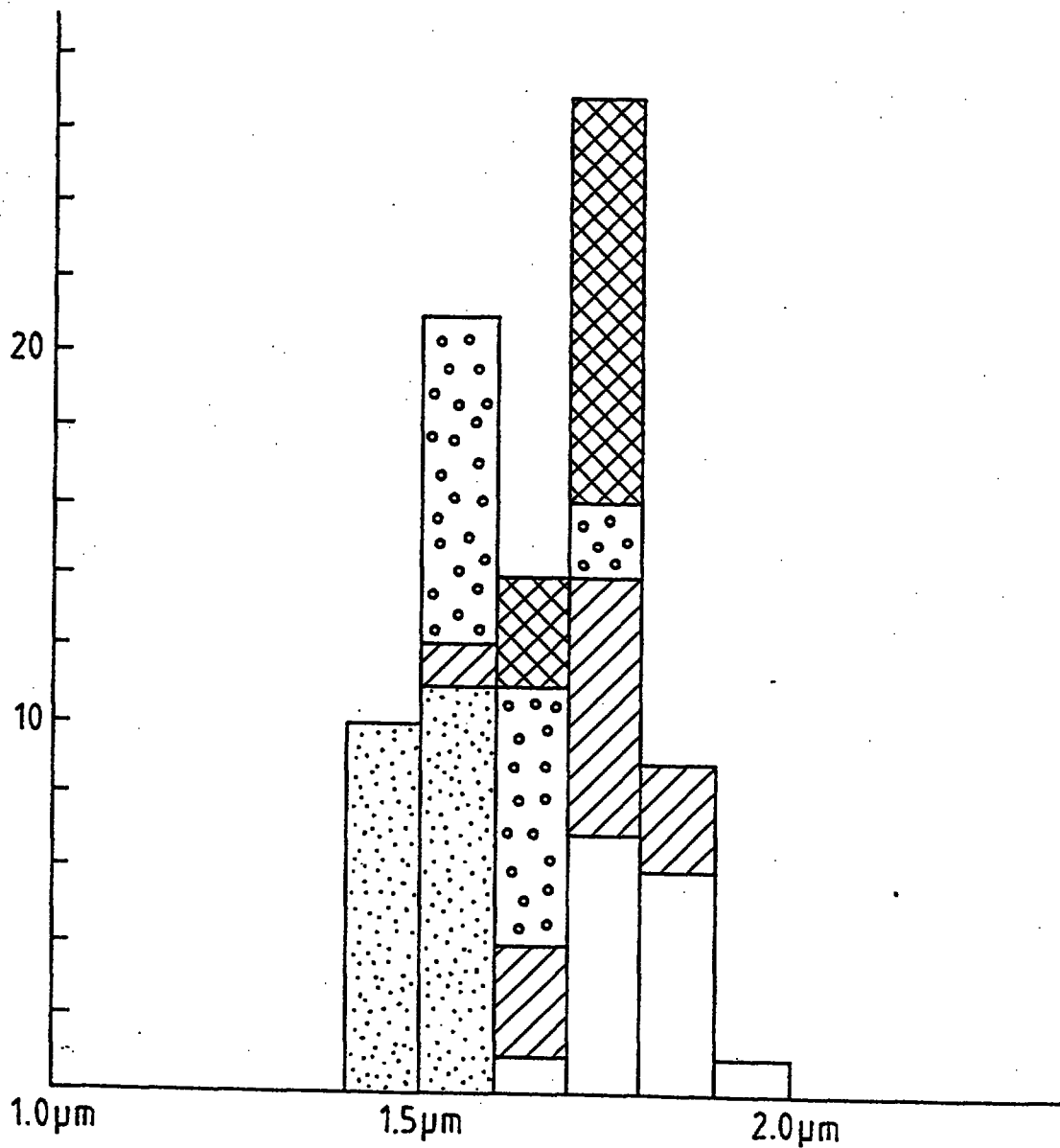
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Fig. 11.



WAFER NO. AQ460; SILOX STRIPE WIDTH 2.0 μ m

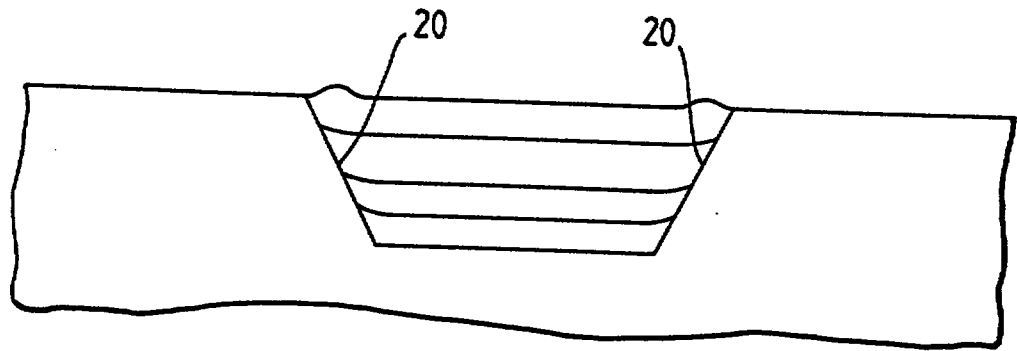
"	"	AQ485(ii);	"	"	"	1.85 μ m
"	"	AF108 ;	"	"	"	1.85 μ m
"	"	AQ482 ;	"	"	"	1.85 μ m
"	"	AQ485(i);	"	"	"	1.85 μ m



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Fig.12.



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✓ Author(s) :	pages 23, 24	to page 24
✓ Abstract :	pages 23, 24	to page 24

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semiconductor material, and both optically and electrically in a horizontal direction by the confinement layers. The confinement layers act to cause any current flowing between the contacts to flow preferentially through the mesa and therefore through the active layer. In one form, the confinement layers may present non-conducting semiconductor junctions to current flow between the contacts in use of the device.

Good electrical confinement is provided if the semiconductor layer between the contacts constitute a p-n junction and the confinement layers in combination with the substrate constitute an n-p-n junction when taken in the same direction. In use the confinement layers and substrate then comprise a reverse biased semiconductor junction in both directions. Alternatively the confinement layers and substrate could present multiple reverse biased semiconductor junctions in one or both directions.

In another form, the confinement layers may comprise "semi-insulating" material such as Fe doped InP. These materials have a relatively high resistivity compared to for instance undoped InP. Confinement layers in this form have advantages in that they substantially completely oppose current flow and show low capacitance effects. Low capacitance effects tend to increase device speed.

In the past devices of this type have been fabricated by means of liquid phase epitaxy (LPE), see for example DE-A-3502326, and "A Novel Technique To Fabricate GaInAsP/InP Buried Heterostructure Laser Diodes", Applied Physics Letters, 44(10), 15 May 1994. However there are problems associated with these techniques such as solutal convection within the melts, inaccurate thickness control of the confinement layers and meltback of the mesas during fabrication. These have lead in particular to lack of uniformity over large areas and the techniques do not lend themselves easily to large scale production.

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All the growth steps of the above method are performed by low pressure MOVPE and hence large scale production should be facilitated. Further it is particularly convenient since only one growth technique must be employed. However, the
5 devices produced rely on a built-in potential difference between the large area p-n homo-junctions to each side of the active region and the p-n heterojunction through the relatively small area active region itself. Although a lowest measured threshold current of 11 mA using continuous
10 wave operation has been quoted, the values given for measurements relating to 269 devices were variable in the range from 17.9 mA to 50.0 mA inclusive. 44% of these devices had a threshold current of more than 45 mA. An optical power emission of only up to 15 mW is quoted, and
15 current blocking on either side of the mesa had to be improved by proton bombardment to the depth of the p-n junction and beyond. Such bombardment is not easy to carry out with satisfactory results.

It is an object of the present invention to provide an
20 improved semiconductor structure and a method of manufacture therefor.

Hereinafter, structures and devices may be described in terms, such as "uppermost", which imply a specific orientation of the structure or device. The use of such
25 terms is for convenience of description only and should not be taken to limit any structure or device to a specific orientation.

According to a first aspect of the present invention there is provided a semiconductor structure comprising a
30 substrate having a first region of epitaxial layers and a second region of epitaxial layers grown on a face thereof, there being an interface between said first and second regions, said interface extending in a generally transverse direction with respect to the substrate, and the first region
35 being constituted by a mesa supported by the face of the substrate, wherein at least a major portion of the interface corresponds at least substantially to (111) B

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crystallographic planes of the material or materials of the first region, characterised in that the common surfaces between adjacent layers of the second region are substantially parallel to (100) crystallographic planes of the material or materials of the first region right up to the interface between said first and second regions.

It has been found that, surprisingly, it is possible to grow layers in the second region, against such an interface, which tend to show no significant change in depth even immediately adjacent the interface. This means that relatively good control may be exercised over the positions of, for instance, transitions from one layer to the next in the first and second regions, even at the interface. Hence the relative positions of semiconductor junctions can be better controlled at the interface if layers of each region are appropriately doped.

Particularly advantageously, it has been found that such semiconductor structures can be fabricated using MOVPE growth techniques, having the advantages described above.

It has been thought that the layers referred to grow so flat against the interface because of the phosphorous-rich nature of (111) B crystallographic planes of InP. However it has further been found, surprisingly, that the major portion of the interface may correspond to modified (111) B crystallographic planes without significantly affecting the flat characteristic of the layers in the second region. This can be particularly advantageous in the fabrication of some semiconductor structures where for instance an improved device can be made by a technique incorporating a heating step which causes material transport at the interface before the layers of the second region are grown. An example of such a device can be a buried heterostructure laser. A technique incorporating a heating step, and a semiconductor structure made by the use of the technique, is described below. (The heating step acts to "clean up" the sides of a mesa so that improved growth of confinement layers against the mesa occurs, in spite of the treatment history of the

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mesa before growth.)

The term "modified (111) B crystallographic plane" means that the major portion of the interface has been fabricated by exposing a (111) B crystallographic plane in the material of the first region, then subsequently modifying the plane, for instance by heat treatment causing material transport, so that it no longer accurately represents a (111) B crystallographic plane. However, the interface will retain general characteristics of the (111) B crystallographic plane, for instance the overall direction of slope and the characteristic interaction with certain growth techniques, particularly MOVPE, which allows the layers in the second region to grow relatively evenly, right up to the interface.

Preferably the major portion of the interface comprises of the order of 60%, or more preferably of the order of 80%, of that interface. Also preferably, said major portion should comprise parts of the interface both adjacent to, and furthest from the substrate. Both these preferred features tend to encourage a generally flat characteristic of the layers grown against the interface.

Advantageously, in a semiconductor structure, according to the present invention, the mesa comprises a p-n junction which extends parallel to the face of the substrate, the lateral surfaces of the mesa being buried by one of more confinement layers.

Such semiconductor structures are particularly useful in buried heterostructure lasers.

Because semiconductor material such as InP can be used to grow surprisingly flat confinement layers against the lateral surfaces of such a mesa, for instance by means of MOVPE, the depth and positional relationship of the layers to a mesa can be relatively closely controlled. This is particularly important where the mesa contains a p-n junction and the confinement layers present an n-p junction to block current flow in use of a device. It can also be advantageous for subsequent steps in fabrication of a device.

As before, the (111) B crystallographic planes may be

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modified, for instance by heat treatment causing material transport.

It has been found that, as mentioned above, if the mesa incorporates an active layer of a device, the device may be improved by heating the structure, before growth of confinement layers against the lateral surfaces, so as to cause material transport onto the sides of the active layer. This is preferable to growing the confinement layers against the sides of the active layer directly after etching those sides, producing for instance a device with more reliable performance characteristics.

According to a second aspect of the present invention there is provided a method of making a semiconductor structure comprising a substrate having a first region of epitaxial layers and a second region of epitaxial layers grown on a face thereof, there being an interface between said first and second regions, said interface extending in a generally transverse direction with respect to the substrate, the method comprising the stages of:

- i) growing epitaxial layers on the surface of a substrate and etching away regions thereof to form a step, the major portion of the side of said step corresponding at least substantially to (111) B crystallographic planes of the material or materials of said first region; and
- (ii) preferentially growing epitaxial layers of semiconductor material by means of any one of a MOVPE, a MBE or a MOMBE technique onto the exposed surface of the substrate and up against the side of said step, so that said epitaxial layers of semiconductor material are substantially parallel to (100) crystallographic planes of the material of the first region right up to where said layers meet the side of said step.

The method may further comprise a stage in which the (111) B crystallographic planes are modified, for instance by

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heating to cause material transport at the interface, before the growth of the semiconductor material. To prevent growth on the layer or layers of the first region, an epitaxial growth suppressing material may be deposited on that layer or
5 layers prior to stage ii) above.

According to a third aspect of the present invention, there is provided a method of making a semiconductor structure according to the first aspect of the present invention which comprises the steps of:

- 10 i) growing epitaxial layers on the surface of a substrate;
- ii) forming a stripe of an epitaxial-growth-suppressing material on the resulting structure;
- 15 iii) using the stripe as a mask, etching a mesa with an etchant or a selection of etchants so as to expose (111) B crystallographic planes over at least a major portion of the side surfaces of the thus-formed mesa;
- 20 iv) preferentially growing semiconductor material, by means of any one of a MOVPE, a MBE or a MOMBE technique, to grow confinement layers onto the exposed surface of the substrate and up against the side surfaces of the mesa, said confinement layers being substantially parallel to (100)
- 25 crystallographic planes of the mesa; and
- v) removing the stripe.

An important application of the present invention is in the production of lasers, particularly those which will operate in a single transverse mode. These lasers are of
30 major importance in optical communication systems. Such lasers can be produced from semiconductor structures made by the method of the present invention in which the uppermost surface of the mesa is restricted to being not more than 5 μm wide.

35 Step iv. above may advantageously be preceded by a step in which the lateral surfaces of the mesa are modified by heat treatment which causes material transport at those

surfaces.

Single transverse mode semiconductor lasers, and a waveguide, according to embodiments of the present invention will now be described, by way of example only, with reference
5 to the accompanying figures in which:

Figure 1 shows a vertical cross section of a laser according to a first embodiment of the present invention;

Figure 2 shows a cross section of part of a double heterostructure wafer for use in making the laser of Figure
10 1;

Figure 3a to 3f shows stages in production of the laser of Figure 1;

Figure 4 shows a scanning electron microscope image of a cross section of a semiconductor laser according to second
15 and third embodiments of the present invention;

Figure 6 shows a stage in the production of a laser according to an embodiment of the present invention, following an optional additional treatment step;

CLAIMS

1. A semiconductor structure comprising a substrate having a first region of epitaxial layers and a second region of epitaxial layers grown on a face thereof, there being an
5 interface between said first and second regions, said interface extending in a generally transverse direction with respect to the substrate, and the first region being constituted by a mesa supported by the face of the substrate, wherein at least a major portion of the interface corresponds
10 at least substantially to (111) B crystallographic planes of the material or materials of the first region, characterised in that the common surfaces between adjacent layers of the second region are substantially parallel to (100)
crystallographic planes of the material or materials of the
15 first region right up to the interface between said first and second regions.

2. A semiconductor structure according to claim 1, wherein the major portion of the interface corresponds to (111) B crystallographic planes of the material or materials
20 of the first region which have been modified by a previous heat treatment step.

3. A semiconductor structure according to claim 1 or claim 2, wherein the major portion of the interface is at least 60% of the area of the interface.

25 4. A semiconductor structure according to claim 1 or claim 2, wherein the major portion of the interface is at least 80% of the area of the interface.

5. A semiconductor structure according to any one of the preceding claims, wherein the major portion of the interface
30 comprises parts of the interface adjacent to, and furthest from, the substrate.

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which extends parallel to the face of the substrate, the lateral surfaces of the mesa being buried by one or more confinement layers constituting the second region.

7. A semiconductor structure according to any one of
5 claims 1 to 6, wherein the material of the first region is InP.

8. A semiconductor structure according to any one of
claims 1 to 7, wherein the material of the second region is InP.

10 9. A semiconductor structure according to any one of
claims 5 to 8, wherein the p-n junction lies in, or adjacent
to, an active layer in the mesa.

10. A semiconductor structure according to claim 9,
wherein the width of the active layer is less than the width
15 of the mesa.

11. A semiconductor structure according to claim 9 or
claim 10, wherein the active layer is a layer of quaternary
material, the confinement layers providing each side of the
mesa with at least one current blocking semiconductor
20 junction, and wherein a second layer of quaternary material
extends over the face of the substrate beneath the mesa and
the confinement layers.

12. A semiconductor structure according to claim 11,
wherein the band gap of the second layer of quaternary
25 material is lower than the band gap of the active layer.

13. A semiconductor structure according to any one of the
preceding claims, wherein said structure forms part of a
semiconductor laser.

14. A method of making a semiconductor structure



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comprising a substrate having a first region of epitaxial layers and a second region of epitaxial layers grown on a face thereof, there being an interface between said first and second regions, said interface extending in a generally transverse direction with respect to the substrate, the method comprising the stages of:

- i) growing epitaxial layers on the surface of a substrate and etching away regions thereof to form a step, the major portion of the side of said step corresponding at least substantially to (111) B crystallographic planes of the material or materials of said first region; and
- (ii) preferentially growing epitaxial layers of semiconductor material by means of any one of a MOVPE, a MBE or a MOMBE technique onto the exposed surface of the substrate and up against the side of said step, so that said epitaxial layers of semiconductor material are substantially parallel to (100) crystallographic planes of the material of the first region right up to where said layers meet the side of said step.

15. A method according to claim 14, wherein stage i) is carried out using a mask of an epitaxial growth suppressing material to create the step, the mask being left in place during stage ii) thereby to achieve the preferential growth of stage ii).

16. A method according to claim 14 or claim 15, which further comprises a stage in which the (111) B crystallographic plane is modified by heat treatment prior to stage ii).

17. A method of making a semiconductor structure according to any of claims 1 to 13, the method comprising the steps of:

- i) growing epitaxial layers on the surface of a

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- substrate;
- ii) forming a stripe of an epitaxial-growth-suppressing material on the resulting structure;
 - iii) using the stripe as a mask, etching a mesa with
5 an etchant or a selection of etchants so as to expose (111) B crystallographic planes over at least a major portion of the side surfaces of the thus-formed mesa;
 - iv) preferentially growing semiconductor material, by
10 means of any one of a MOVPE, a MBE or a MOMBE technique, to grow confinement layers onto the exposed surface of the substrate and up against the side surfaces of the mesa, said confinement layers being substantially parallel to (100)
15 crystallographic planes of the mesa; and
 - v) removing the stripe.

18. A method according to claim 17, which further comprises the step of selectively etching an active layer of the mesa, prior to step iv), so that the width of said active
20 layer is less than the width of the mesa.

19. A method according to claim 17 or claim 18, which further comprises the step of modifying the exposed (111) B crystallographic planes by heat treatment sufficient to cause material transport at the lateral surfaces of the mesa, prior
25 to step iv).

20. A method according to claim 16 or claim 17, wherein the stripe comprises a MOVPE growth-suppressing material, and the confinement layers are grown by MOVPE.



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