

CLAIMS:

1. A current-to-digital converter module comprising:
 - a modulation switch, SW_K , configured to modulate an input current, I_{IN} , to produce a scaled current, I_{INK} , wherein the switch SW_K is controlled by a modulation clock F_K ;
 - a delta-sigma analogue-to-digital converter, $\Delta\Sigma$ ADC, comprising an integrator coupled to a hysteresis comparator that is coupled to a D-type Flip-Flop being driven by a master clock, F_S , whereby an inverting output from the D-type Flip-Flop is coupled to an inverting input of the integrator using a 1-bit feedback current digital-to-analogue converter, DAC, the $\Delta\Sigma$ ADC being configured to generate digital outputs at a non-inverting output and the inverting output of the D-type Flip-Flop based on a balanced current, I_{BAL} , received at the inverting input of the integrator, whereby the balanced current I_{BAL} comprises a summation of the scaled current I_{INK} with a reference current, I_{REF} , produced by the 1-bit feedback current DAC;
 - a successive-approximation-register (SAR) control logic configured to generate control signals based on the non-inverting outputs from the D-type Flip-Flop, a reset clock signal and the master clock F_S ; and
 - a clock generator module that is driven by the master clock, F_S , being configured to use the control signals from the SAR control logic to determine an optimal modulation clock F_K for controlling the switch SW_K .
2. The module according to claim 1 wherein the modulation switch SW_K comprises:
 - a transmission gate switch that is body biased with a reference voltage V_{CM} when the switch is at an OFF-state, wherein the reference voltage V_{CM} is used as the reference voltage at the non-inverting inputs of the integrator and hysteresis comparator of the $\Delta\Sigma$ ADC.
3. The module according to claim 1 wherein the integrator of the $\Delta\Sigma$ ADC comprises:
 - a two-stage integrator circuit having a first and a second stage, wherein a compensation capacitor C_C couples a low impedance node of the first stage to an output of the second stage.
4. The module according to claim 1 wherein the hysteresis comparator of the $\Delta\Sigma$ ADC comprises:
 - an inverter based hysteresis comparator circuit having an inverter provided at the input of the comparator circuit, wherein a threshold voltage of the inverter is similar as threshold voltages of transistors used in the comparator circuit.

5. The module according to claim 1 wherein the 1-bit feedback current DAC comprises:
a cascaded current mirror circuit.
6. The module according to claim 1 wherein the clock generator module comprises:
a plurality of D-type Flip Flop, logic AND gate pairs and a logic OR gate, configured in a frequency divider configuration to generate a modulation pulse.
7. A method for converting current to digital signals using a current-to-digital converter module having a modulation switch SW_K , a delta-sigma analogue-to-digital converter, $\Delta\Sigma$ ADC, comprising an integrator coupled to a hysteresis comparator that is coupled to a D-type Flip-Flop being driven by a master clock, F_S , a successive-approximation-register (SAR) control logic, and a clock generator module that is driven by the master clock, F_S , the method comprising:
 - modulating, using the modulation switch, SW_K , an input current, I_{IN} , to produce a scaled current, I_{INK} , wherein the switch SW_K is controlled by a modulation clock F_K ;
 - coupling an inverting output from the D-type Flip-Flop an inverting input of the integrator using a 1-bit feedback current digital-to-analogue converter, DAC,
 - generating, using the $\Delta\Sigma$ ADC, digital outputs at a non-inverting output and the inverting output of the D-type Flip-Flop based on a balanced current, I_{BAL} , received at the inverting input of the integrator, whereby the balanced current I_{BAL} comprises a summation of the scaled current I_{INK} with a reference current, I_{REF} , produced by the 1-bit feedback current DAC;
 - generating, using the SAR control logic, control signals based on the non-inverting outputs from the D-type Flip-Flop, a reset clock signal and the master clock F_S ; and
 - determining, using a clock generator module, based on the control signals from the SAR control logic an optimal modulation clock F_K for controlling the switch SW_K .
8. The method according to claim 7 wherein the modulation switch SW_K comprises:
a transmission gate switch that is body biased with a reference voltage V_{CM} when the switch is at an OFF-state, wherein the reference voltage V_{CM} is used as the reference voltage at the non-inverting inputs of the integrator and hysteresis comparator of the $\Delta\Sigma$ ADC.
9. The method according to claim 7 wherein the integrator of the $\Delta\Sigma$ ADC comprises:

a two-stage integrator circuit having a first and a second stage, wherein a compensation capacitor C_c couples a low impedance node of the first stage to an output of the second stage.

10. The method according to claim 7 wherein the hysteresis comparator of the $\Delta\Sigma$ ADC comprises:

an inverter based hysteresis comparator circuit having an inverter provided at the input of the compactor circuit, wherein a threshold voltage of the inverter is similar as threshold voltages of transistors used in the comparator circuit.

11. The method according to claim 7 wherein the 1-bit feedback current DAC comprises a cascaded current mirror circuit.

12. The method according to claim 7 wherein the clock generator module comprises:

a plurality of D-type Flip Flop, logic AND gate pairs and a logic OR gate, configured in a frequency divider configuration to generate a modulation pulse.