WHAT IS CLAIMED IS:

1. A multi-bit perpendicular magnetic tunnel junction, comprising an upper synthetic antiferromagnetic layer, pinned layer, lower dual free layer, and upper free layer formed in a laminated manner between a top electrode and a bottom electrode,

wherein the multi-bit perpendicular magnetic tunnel junction exhibits any one resistance state of first to fourth resistance states depending on magnetization directions of the lower dual free layer and the upper free layer,

wherein, when a magnitude of a magnetic field applied from outside is swept in a range of a predetermined first threshold value to a predetermined second threshold value, the any one resistance state is sequentially switched in an order of the second resistance state, the fourth resistance state, the first resistance state, and the third resistance state.

2. The multi-bit perpendicular magnetic tunnel junction according to claim 1, wherein the first resistance state is a resistance state that appears when magnetization directions of the upper synthetic antiferromagnetic layer plus the pinned layer and the magnetization direction of the lower dual free layer are parallel and the magnetization direction of the lower dual free layer and the magnetization direction of the upper free layer are parallel.

3. The multi-bit perpendicular magnetic tunnel junction according to claim 1, wherein the second resistance state is a resistance state that appears when magnetization directions of the upper synthetic antiferromagnetic layer plus the pinned layer and the magnetization direction of the lower dual free layer are anti-parallel and the magnetization direction of the lower dual free layer and the magnetization direction of the upper free layer are parallel,

the third resistance state is a resistance state that appears when the magnetization

directions of the upper synthetic antiferromagnetic layer plus the pinned layer and the magnetization direction of the lower dual free layer are parallel and the magnetization direction of the lower dual free layer and the magnetization direction of the upper free layer are anti-parallel, and

the fourth resistance state is a resistance state that appears when the magnetization directions of the upper synthetic antiferromagnetic layer plus the pinned layer and the magnetization direction of the lower dual free layer are anti-parallel and the magnetization direction of the lower dual free layer and the magnetization direction of the upper free layer are anti-parallel.

4. The multi-bit perpendicular magnetic tunnel junction according to claim 1, further comprising a lower tunnel barrier layer formed between the pinned layer and the lower dual free layer, and

an upper tunnel barrier layer formed between the lower dual free layer and the upper free layer.

5. The multi-bit perpendicular magnetic tunnel junction according to claim 1, wherein the lower dual free layer comprises a first lower free layer, upper spacing layer, and second lower free layer formed in a laminated manner.

6. The multi-bit perpendicular magnetic tunnel junction according to claim 1, further comprising a lower synthetic antiferromagnetic layer formed under the upper synthetic antiferromagnetic layer.

7. The multi-bit perpendicular magnetic tunnel junction according to claim 6, further comprising a lower spacing layer formed between the lower and upper synthetic antiferromagnetic layers and

a bridge layer disposed between the upper synthetic antiferromagnetic layer and the pinned layer.

8. A multi-bit perpendicular magnetic tunnel junction, comprising an upper synthetic antiferromagnetic layer, pinned layer, lower dual free layer, and upper multiple free layer formed in a laminated manner between a top electrode and a bottom electrode,

wherein the multi-bit perpendicular magnetic tunnel junction exhibits any one resistance state of first to fourth resistance states depending on magnetization directions of the lower dual free layer and the upper multiple free layer,

wherein, when a magnitude of a magnetic field applied from outside is swept in a range of a predetermined first threshold value to a predetermined second threshold value, the any one resistance state is sequentially switched in an order of the third resistance state, the second resistance state, the first resistance state, and the fourth resistance state.

9. The multi-bit perpendicular magnetic tunnel junction according to claim 8, wherein the first resistance state is a resistance state that appears when magnetization directions of the upper synthetic antiferromagnetic layer plus the pinned layer and the magnetization direction of the lower dual free layer are parallel and the magnetization direction of the lower dual free layer and the magnetization direction of the upper multiple free layer are parallel.

10. The multi-bit perpendicular magnetic tunnel junction according to claim 8, wherein the second resistance state is a resistance state that appears when magnetization directions of the upper synthetic antiferromagnetic layer plus the pinned layer and the magnetization direction of the lower dual free layer are parallel and the magnetization direction of the lower dual free layer and the magnetization direction of the upper multiple free layer are anti-parallel,

the third resistance state is a resistance state that appears when the magnetization directions of the upper synthetic antiferromagnetic layer plus the pinned layer and the magnetization direction of the lower dual free layer are anti-parallel and the magnetization direction of the lower dual free layer and the magnetization direction of the upper multiple free layer are parallel, and

the fourth resistance state is a resistance state that appears when the magnetization directions of the upper synthetic antiferromagnetic layer plus the pinned layer and the magnetization direction of the lower dual free layer are anti-parallel and the magnetization direction of the lower dual free layer and the magnetization of the upper multiple free layer are anti-parallel.

11. The multi-bit perpendicular magnetic tunnel junction according to claim 8, further comprising a lower tunnel barrier layer formed between the pinned layer and the lower dual free layer and

an upper tunnel barrier layer formed between the lower dual free layer and the upper multiple free layer.

12. The multi-bit perpendicular magnetic tunnel junction according to claim 8, wherein the

upper multiple free layer comprises a first upper free layer, bridge layer, and second upper free layer formed in a laminated manner, and

the second upper free layer is formed in a multilayer structure based on [Co/Pt]b (b being a positive integer).

13. The multi-bit perpendicular magnetic tunnel junction according to claim 8, further comprising a lower synthetic antiferromagnetic layer formed under the upper synthetic antiferromagnetic layer.