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METHOD FOR PROVIDING DUAL WORKFUNCTION DOPING AND PROTECTIVE INSULATING CAP

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to a method for providing dual work function doping, and more particularly relates to providing an array of gate structures whereby some of the gate structures are P+ doped and other gate structures are N+ doped. The present invention is especially advantageous for providing structures that include both DRAMs and logic circuits.

Description of the Related Art

Over the last several years, significant advances have occurred in increasing the circuit density in integrated circuit chip technology. The ability to provide significantly increased numbers of devices and circuits on an integrated circuit chip has, in turn, created an increased desire to incorporate or integrate additional system functions onto a single integrated circuit chip. In particular, an increasing need exists for joining both memory circuits and logic circuits together on the same integrated circuit chip.

In fabricating dynamic random access memory (DRAM) circuits, the emphasis has been on circuit density along with reduced cost. On the other hand, when fabricating logic circuits, the emphasis has been on creating circuits that operate faster. Accordingly, this desire for dual work function creates additional problems with respect to the complexity and relative cost of the fabricating process. For instance, memory circuits achieve increased density requirements by employing self-aligned contacts (borderless bit line contacts), which are easily implemented in a process having a single type (e.g. typically N+ type) gate work function. A buried-channel P-type metal oxide semiconductor (PMOSFET) is used in creating DRAMs since such permits a single work function gate conductor, N+, to be used throughout the fabrication process. This results in significant cost savings in fabricating DRAMs, but at the expense of creating an inferior performing PMOSFET. On the other hand, logic circuits require both P+ and N+ gated MOSFETs in order to achieve the necessary switching speeds. P+ and N+ gate conductor devices are highly desirable for merged logic and DRAM products.

High-performance logic requires the use of both N+ and P+ doped gate conductors. Although currently practiced high-performance logic processes provide dual workfunction gate conductors, they do not use an insulating gate cap because of density requirements, and hence the need for diffusion contacts borderless to gate conductors, which are of secondary importance to speed. In 13

DRAMs, an insulating cap which is self-aligned to the gate conductor is essential for forming bitline contacts which are borderless to the wordlines. Borderless contacts are needed for achieving the highest density memory cell layouts. However, cost-effective DRAM processes use only a single N+ polysilicon gate conductor. Thus, there is currently no economically attractive process for providing both dual workfunction gate doping and the capability of borderless diffusion contacts.

SUMMARY OF THE INVENTION

In view of the foregoing and other problems of the conventional techniques, an object of the present invention is to provide dual workfunction doping gate conductors and including a self-aligned insulating gate cap.

It is another object of the present invention to provide dual work function doping. This may include providing a semiconductor substrate, a gate insulator conductor (comprising intrinsic polysilicon and overlying silicide layer) and an insulating cap. The method may also include providing insulating spacers (such as boron silicate glass spacers) along sides of the silicide layer (WSi_x) and the insulating cap, doping portions of the semiconductor substrate and the conductor with a first conductive type and other portions with a second conductive type, and

annealing the conductor such that the dopants of the first and second conductive types spread over the respective conductors.

Portions of the silicide layer and portions of the insulating cap may be etched to form a partial gate conductor stack prior to providing the insulating spacers. After providing the insulating spacers and prior to doping, the method may further include etching the intrinsic conductor at areas of the conductor not covered by the spacer material.

An oxide layer may be formed on portions of the semiconductor substrate not covered with the intrinsic conductor. Insulating spacers may be removed prior to doping portions of the semiconductor substrate and the conductor.

Portions of the semiconductor substrate may correspond to source and drain contact regions. The method may further include extending the source and drain regions in the support region of the substrate to a region at least under the annealed conductor. The method may also include forming source and drain regions in the array regions.

It is also an object of the present invention to achieve the dual work function requirement for selectively applying either P+ or N+ doping to the gate conductor while at the same time creating a self-aligned insulating cap on the gate conductor.

Other objects, advantages and salient features of the invention will become apparent from the following detailed description taken in conjunction with the annexed drawings, which disclose preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements and wherein:

Fig. 1 shows an initial semiconductor structure;

Fig. 2 shows the Fig. 1 semiconductor structure after etching;

Figs. 3A and 3B show the semiconductor structure in the array and support regions, respectively, after depositing spacer material;

Figs. 4A and 4B show the semiconductor structure after etching spacer material;

Figs. 5A and 5B show the semiconductor structure after formation of a screen oxide layer;

Figs. 6A and 6B show the semiconductor structure after doping;

Figs 7A and 7B show the semiconductor structure after annealing;

Figs. 8A and 8B show the semiconductor structure after source-drain extension;

Figs. 9A and 9B show the semiconductor structure after deposition of interlayer dielectric layer; and

Fig. 10 is a flowchart showing steps of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Figs. 1 and 2 will now be described with respect to forming a partial gate conductor stack. Following that discussion, the figures will be divided to show the gate conductor stack in support regions and array regions of the semiconductor structure.

Fig. 1 shows a semiconductor substrate 5 which is initially provided and a gate oxide layer 10 provided over the substrate 5. The semiconductor substrate 5 is typically silicon but can be any semiconductor material such as group II-VI semiconductors, group III-V semiconductors, or a composite silicon semiconductor such as silicon carbide. The semiconductor substrate 5 typically contains well doping regions which have been implanted prior to the formation of the overlying layers. Further, a nitride or oxy nitride gate insulator may be used rather than the gate oxide layer 10.

A gate stack is deposited over the substrate 5 and the gate oxide layer 10. The gate stack may include an intrinsic (i.e., undoped) polysilicon layer 11, a

tungsten silicide (WSi_x) layer 12, and a silicon nitride layer 13 acting as a nitride cap 13.

A gate conductor (GC) mask, such as a layer of resist material (not shown) of the type employed in known lithographic masking and etching techniques, is placed over the nitride cap 13. Any well-known photosensitive polymerizable resist materials may be used. The resist material may be applied by spinning or by spraying, for example. The gate stack is patterned and etched through the nitride cap 13 and the WSi_x layer 12 down to the polysilicon layer 11 as shown in Fig. 2. Overetching into the polysilicon layer 11 is acceptable.

As is known in the art, the semiconductor structure may include array regions and support regions and the following discussion regarding Figs. 3A-9B contains different processes between the support region and the array region. Since the layout in the array region requires the utmost density, minimum channel length (minimum polysilicon gate conductor stack width) and minimum space between gate conductors is utilized. In the array region, a minimum space between gate conductors requires that diffusion contacts be borderless to the array gate conductors (wordlines). Borderless contact technology is most compatible and least expensive for single workfunction gate conductors (i.e., preferably N+).

Since density requirements in the support regions are more relaxed than in the array, borderless diffusion contacts and gate conductors with insulating caps are not required. However, dual workfunction gate conductors in the supports are

desired for improved performance. In the following discussion each of Figs. 3A, 4A, 5A, 6A, 7A, 8A, and 9A shows the structure in the array region and each of Figs. 3B, 4B, 5B, 6B, 7B, 8B and 9B shows the structure in the support region.

As shown in Fig. 3, a layer of boron silicate glass (BSG) 32 is conformally deposited over the partially patterned gate stack. The BSG 32 thickness is selected such that the narrow spaces between gate conductors (wordlines) in the array region (Fig. 3A) are completely filled while the wider spaces in the support region (Fig. 3B) contain the topography of the conformal layer of the BSG 32 (Fig. 3B). In an exemplary case, for a 150 nm minimum feature size, the spacing between gate conductors in the array region (Fig. 3A) is nominally approximately 150 nm, whereas the spacing between gate conductors in the support region (Fig. 3B) is typically 300 nm or greater. A BSG layer 32 thickness of between approximately 80 nm and 140 nm is preferably used.

The deposited BSG 32 is then reactive ion etched (RIE'd) selectively to the silicon nitride, forming spacers 30 on the gate sidewalls in the support region (Fig. 4B), but leaving the spaces filled in with the BSG 32 in the array region (Fig. 4A).

In the support region, the exposed intrinsic polysilicon layer 11 of the gate stack is reactive ion etched selectively to oxide and nitride, stopping on the gate oxide layer 10 over the substrate 5. Because of the spacers 30 in the support region (Fig. 5B) and the protective BSG 32 (i.e., blocking layer) filling the gaps between gate conductors in the array region (Fig. 5A), only the support region

gate polysilicon layer 11 is opened by the RIE process. A screen oxide layer 41 is preferably thermally grown on the exposed silicon substrate 5 as shown in Fig. 5B. The screen oxide layer 41 protects the surface of the substrate 5 from ion implant damage due to subsequent implantation of source-drain dopant. Furthermore, screen oxidation also "heals" the silicon surface from any plasma damage induced during the gate polysilicon reactive ion etch.

The BSG 32 is then isotropically etched selective to SiN silicon, WSi_x and thermal oxide using etchants well known in the art (i.e., wet HF/sulphuric acid). Since BSG etches much more rapidly than the thermally grown oxide layer 41, the screen oxide layer 41 is left mostly intact. Masked ion implants are then used to introduce N+ dopant (e.g., As or Phos) into the gate polysilicon layer 11 of the array region (Fig. 6A), into the gate polysilicon layer 11 of the support region's (Fig. 6B) NFETs (i.e., in the exposed ledges 43), and into a portion of the source-drain regions 51 of the support region's NFETs. The support region's PFETs receive a P-type dopant implant (typically boron) into the gate polysilicon layer and the source-drain regions 51. The energy of the N+ implant is selected such that the amount of dopant penetrating through the array region's gate polysilicon layer 11 into the substrate 5 is negligible.

Then, as shown in Figs. 7A and 7B, a high temperature anneal is used to distribute the dopants throughout the lateral extent of the gate polysilicon layer 11. This anneal may have a broad range of time and temperature; for example 1100°C

for 10s to 850°C for 30 minutes. Since the diffusivity of dopant in polysilicon is typically 100X greater than in single crystal silicon, the junctions which were implanted into the silicon substrate 5 diffuse by an insignificant amount during the anneal. A silicon reactive ion etch is then used to remove the gate polysilicon ledges 43 in the support region (Fig. 7B) and to separate the gate polysilicon conductors in the array region (Fig. 7A).

Then, the oxide ears 42 are removed by a dilute HF etch and a gate sidewall oxide 90 is grown (Fig. 8B). Array diffusions (N-type) 53 and support source-drain extensions (N and P-type) 54 are implanted depending on the type of FET as shown in Fig. 8B. Typical extension implants for NFETs preferably may be done using Phos at $5x10^{13}$ - $5x10^{14}$ cm^{-2} at 5-20 keV or As at $5x10^{13}$ - $5x10^{14}$ cm^{-2} at 15-50 keV. For PFETs, boron may be used at $5x10^{13}$ - $5x10^{14}$ cm^{-2} at 5-20 keV.

Then, as shown in Figs. 9A and 9B, nitride spacers 92 are formed on the gate conductor sidewalls (needed for borderless contacts) following standard processing well known in the art. An interlayer dielectric 100 (typically CVD oxide) is deposited and vias are etched for subsequent formation of contact studs. The vias are opened borderless to the gate conductors in the array region (via opening overlaps gate conductor), while the vias are formed between gate conductors in the support region (Fig. 9B). The reason for this distinction is that the metal studs 94 (i.e., tungsten) needed for low-resistance and performance in

the support region make the borderless contacts for the support region complicated and expensive. Therefore, to avoid contact stud 94 to gate shorts in the support region, the vias are not opened over the gate conductor. This necessitates wider spacing of the gate conductors in the support region. Since higher series resistance is acceptable in the array region, polysilicon studs 95 are used which allow relatively easy formation of borderless contacts. This dual workfunction/capped gate conductor process is applicable to DRAMs containing either deep trench or stacked capacitor storage elements. The storage capacitors are not shown in Fig. 9A for simplicity.

Fig. 10 shows a flowchart showing steps of the present invention. In particular, in step S100, the semiconductor structure is formed and preferably includes the semiconductor substrate 5 containing isolation regions and well doping regions on which is formed the gate oxide layer 10, the intrinsic polysilicon layer 11, the tungsten silicide layer 12 and the nitride cap 13. Then, in step S102, the respective layers are appropriately etched down to the polysilicon layer 11. Subsequently, in step S104, a maskless process forms a blocking layer in the array region and adds spacers 30 in the support region. The exposed polysilicon layer 11 is then etched in step S106 and the screen oxide layer 41 is grown in step S108.

Subsequently, in step S110, the BSG blocking layer in the array region and the spacers 30 in the support region are removed. The source/drain contact areas 51 and the exposed ledges 43 of the polysilicon layer 11 are implanted in step

S112. Then, in step S114, the structure is annealed to spread the dopants throughout the polysilicon layer 11 and form a doped polysilicon layer 61. Exposed portions of the doped polysilicon layer 61 are etched in step S116. Subsequently, in step S118, portions of the oxide layer 41 and the oxide layer 10 are removed. Subsequently, the sidewall oxide layer 90 is grown, the source/drain extensions 54 are implanted and the array diffusions 53 are implanted in step S120. Then, in step S122, nitride spacers 92 are formed and an interlayer dielectric 100 is deposited.

The resulting structure thereby forms the desired dual workfunction doping including the self-aligned insulating gate cap. That is, the present invention achieves a dual workfunction requirement by applying either P+ or N+ doping to the gate conductor while at the same time creating a self-aligned cap on the gate conductor. The present invention further allows lightly doped source-drains in the array region for low junction leakage, allows formation of source-drain extensions in support regions for high hot-carrier reliability and does not introduce extra masks.

Still further, the present invention allows the formation of borderless diffusion contacts in the array region for high density. The dual workfunction gates in the support region allow surface channel MOSFETs for high performance.

While the invention has been described with reference to specific embodiments, the description of the specific embodiments is illustrative only and is

not to be considered as limiting the scope of the invention. Various other modifications and changes may occur to those skilled in the art without departing from the spirit and scope of the invention.



What is claimed is:

1. A method for providing dual work function doping, the method comprising:

providing a semiconductor substrate, a gate insulator over said semiconductor substrate, a conductor comprising intrinsic polysilicon and overlying silicide layer over said conductor and an insulating cap over said overlying silicide layer;

providing insulating spacers comprising spacer material along sides of said silicide layer and said insulating cap;

doping first portions of said semiconductor substrate and said conductor with a first conductive type dopant and second portions of said semiconductor substrate and said conductor with a second conductive type dopant; and

annealing said conductor such that dopants of said first and second conductive types spread over said respective conductors.

2. The method of claim 1, further comprising etching portions of said silicide layer and portions of said insulating cap to form a partial gate conductor stack prior to providing said insulating spacers.



3. The method of claim 1, wherein said silicide layer comprises WSi_x.

4. The method of claim 1, wherein said insulating spacers comprise boron silicate glass spacers.

5. The method of claim 1, wherein after providing the insulating spacers and prior to doping, the method further comprises etching said intrinsic conductor at areas of the conductor not covered by said spacer material.

6. The method of claim 5, further comprising forming an oxide layer on portions of the semiçonductor substrate not covered with said intrinsic conductor.

7. The method of claim 1, further comprising removing said insulating spacers prior to doping said first and second portions of said semiconductor substrate and said conductor.

8. The method of claim 1, wherein said first and second portions of the semiconductor substrate correspond to source and drain contact regions.

9. The method of claim 8, wherein said semiconductor substrate includes support regions and array regions.

10. The method of claim 9, wherein after annealing the conductor, the method further comprises extending the source and drain regions in said support region of said substrate to a region at least under said annealed conductor.

11. The method of claim 9, wherein after annealing said conductor, the method further comprises forming source and drain regions in said array regions.

12. The method of claim 1, wherein after annealing said conductor, the method further comprises etching portions of said conductor.

13. The method of claim 1, further comprising forming a gate sidewall oxide on sidewalls of said annealed conductor.

14. An array of gate structures obtained by the method of claim 1.

15. A method of forming dual work function doping, the method comprising:

providing a semiconductor substrate, a gate insulator layer over said semiconductor substrate, a relatively undoped polysilicon layer over the gate insulator layer, a highly conductive silicide layer and an insulating cap over said relatively undoped polysilicon layer;

providing insulating spacers comprising spacer material on sidewalls of said insulating cap and said silicide layer;

etching portions of said relatively undoped polysilicon layer which are not covered by the spacer material;

removing the spacer material such that said relatively undoped polysilicon layer includes first and second exposed portions;

doping first exposed portions of said polysilicon layer with a first conductive type dopant;

doping second exposed portions of said polysilicon layer with a second conductive type dopant; and

annealing the polysilicon layer such that remaining portions of said polysilicon layer become doped with said first and second conductive types.

16. The method of claim 15, further comprising etching portions of said silicide layer and portions of said insulating cap to form a partial gate conductor stack prior to providing said insulating spacers.

17. The method of claim 15, wherein said silicide layer comprises WSi_x.

18. The method of claim 15, wherein said insulating spacers comprise boron silicate glass spacers.

19. The method of claim 15, further comprising forming an oxide layer on portions of said semiconductor substrate not covered with said polysilicon layer.

20. The method of claim 15, further comprising doping portions of the substrate with said first conductive type prior to annealing said polysilicon layer, said portions of the substrate corresponding to source and drain contact regions.

21. The method of claim 20, wherein said semiconductor substrate includes support regions and array regions.

22. The method of claim 21, further comprising extending the source and drain contact regions in said substrate region of said substrate to a region at least under said annealed polysilicon layer.

23. The method of claim 21, wherein after annealing said polysilicon layer, the method further comprises forming source and drain regions in said array regions.

24. The method of claim 15, wherein after annealing said polysilicon layer, the method further comprises etching portions of said polysilicon layer.

25. The method of claim 15, further comprising forming a gate sidewall oxide on sidewalls of said annealed polysilicon layer.

26. An array of gate structures obtained by the method of claim 15.

27. A method for providing dual workfunction doping, the method comprising:

providing a semiconductor substrate, a gate insulator over said semiconductor substrate and conductors comprising a deposited semiconductor material over said gate insulator;

doping first portions of said semiconductor substrate and first ones of said conductors with a first conductive type dopant and second portions of said semiconductor substrate and second ones of said conductors with a second conductive type dopant; and

annealing said conductors such that said first and second dopants spread over said respective first and second conductors.

METHOD FOR PROVIDING DUAL WORKFUNCTION DOPING AND PROTECTIVE INSULATING CAP

ABSTRACT

A method for providing dual work function doping and borderless array diffusion contacts includes providing a semiconductor substrate (15), a gate insulator (10), a conductor (11, 12) on the gate insulator, an insulating cap (13) on the conductor (11, 12) and insulating spacers (30) on sidewalls of a portion of the conductor (11, 12) and the insulating cap (13). The method also includes doping portions of the semiconductor substrate (5) and the conductor (11) with a first conductive type and other portions with a second conductive type. The conductor may be annealed such that dopants of the first and second conductive types spread over the respective conductors.

Fig 10

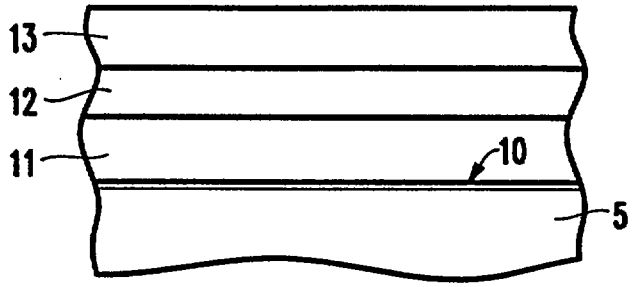


FIG.1

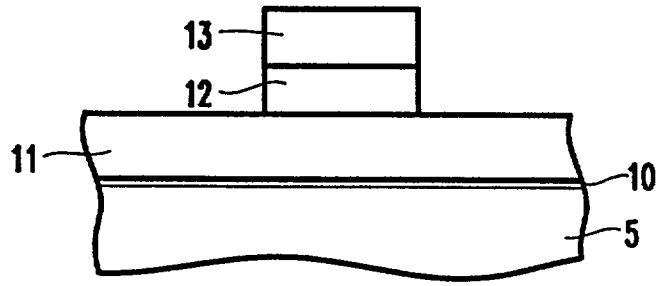


FIG.2

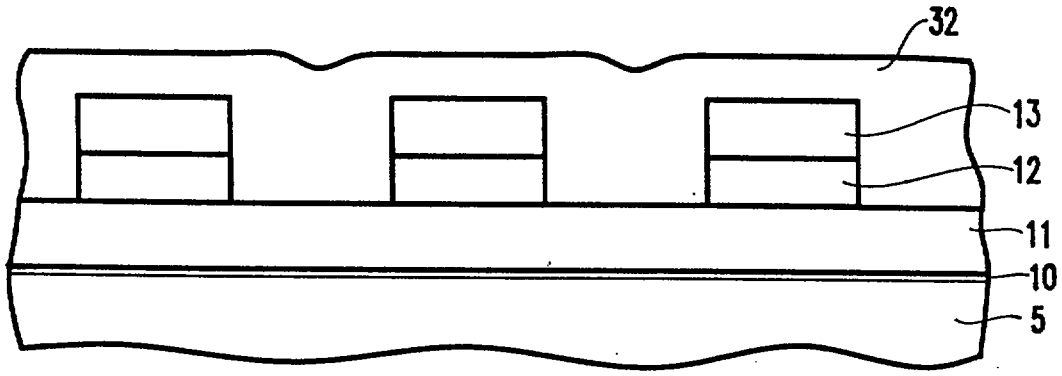


FIG.3A

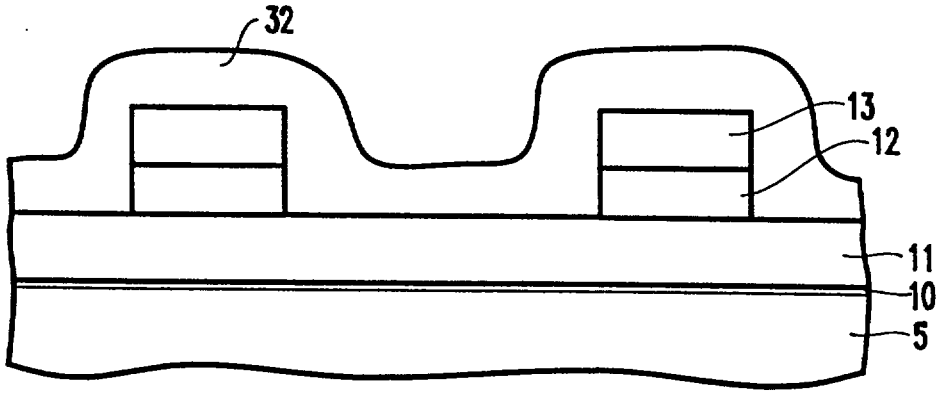


FIG.3B

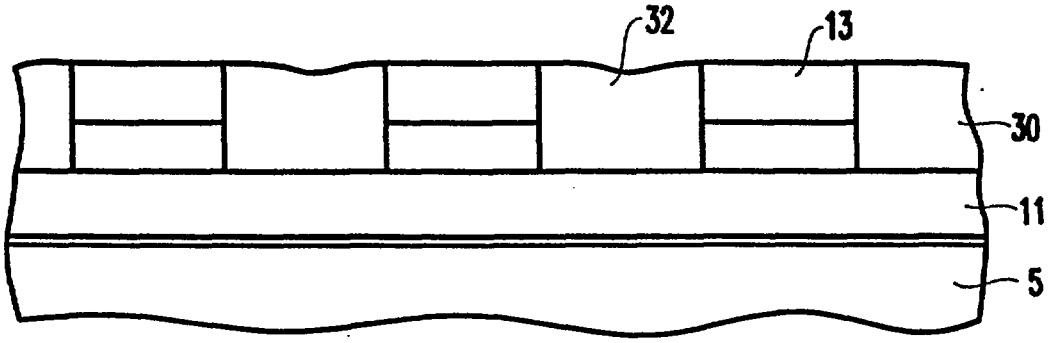


FIG.4A

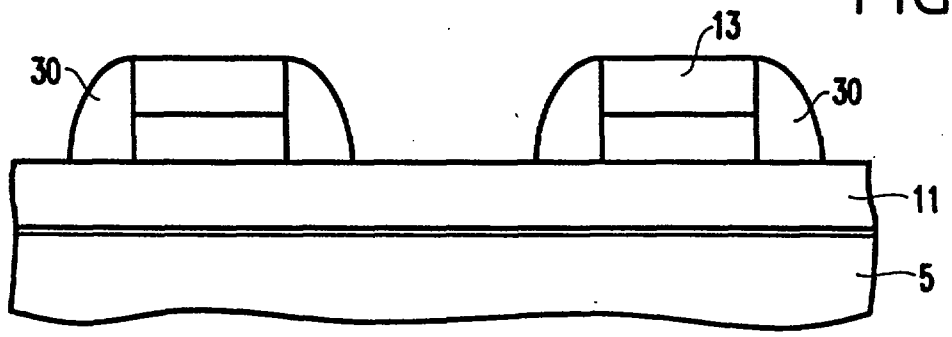


FIG.4B

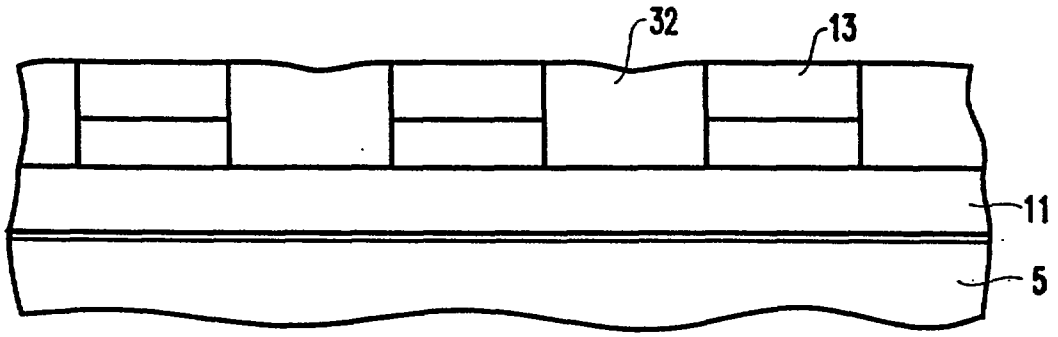


FIG.5A

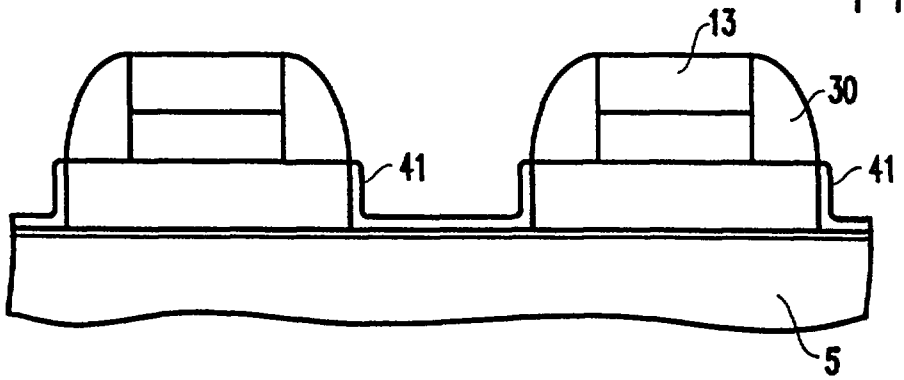


FIG.5B

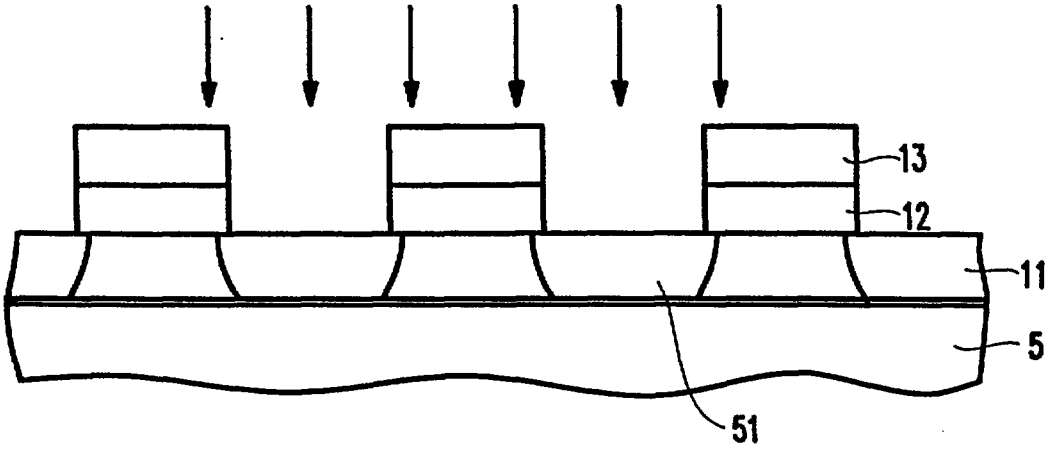


FIG.6A

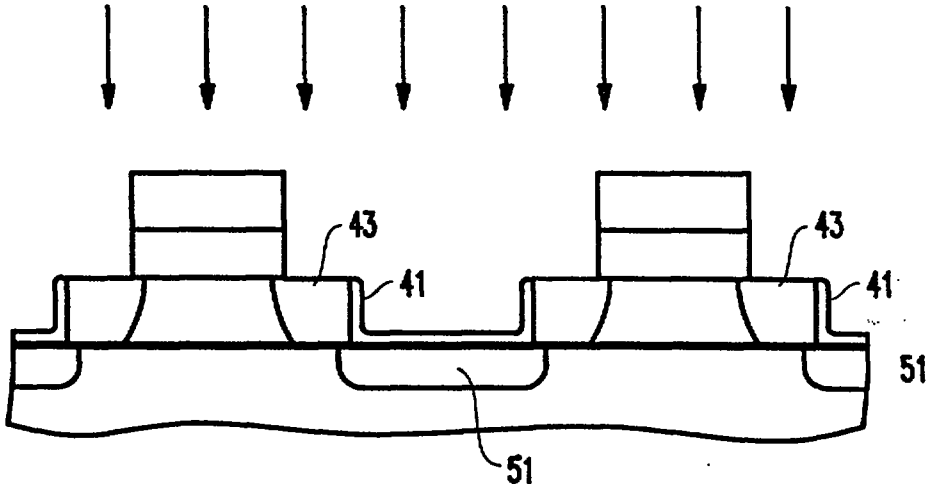


FIG.6B

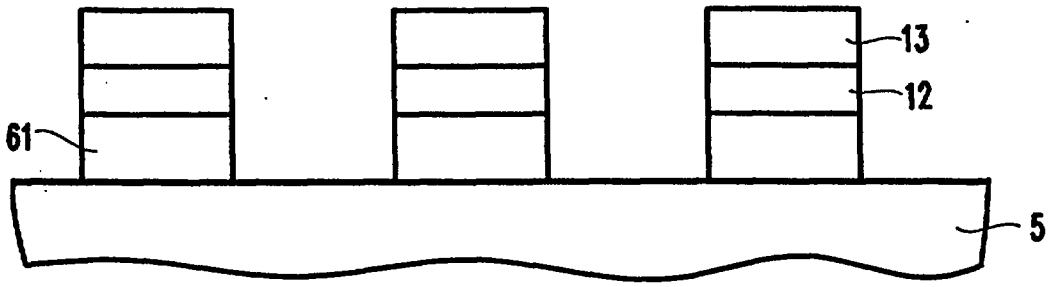


FIG.7A

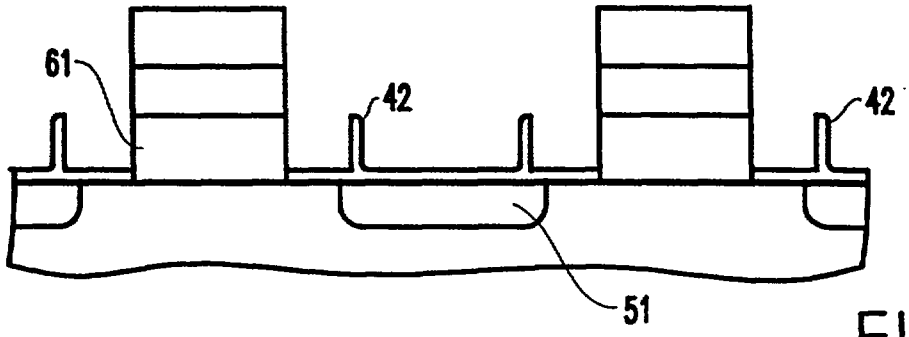


FIG.7B

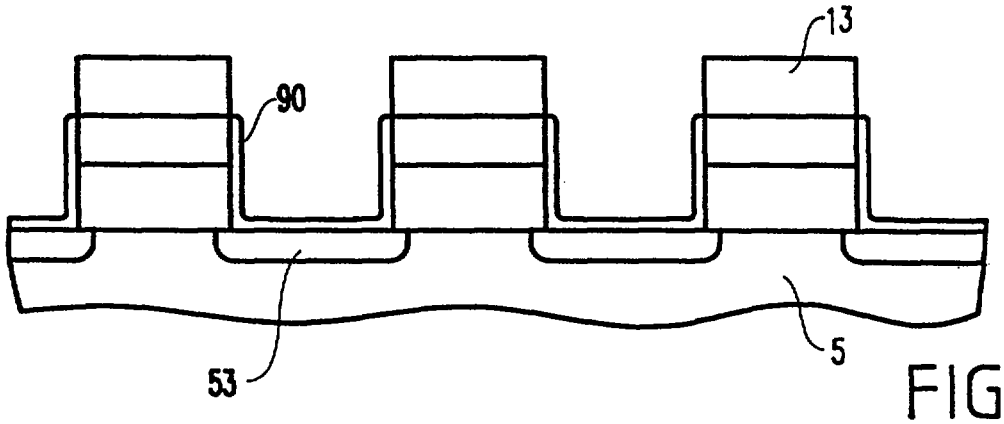


FIG.8A

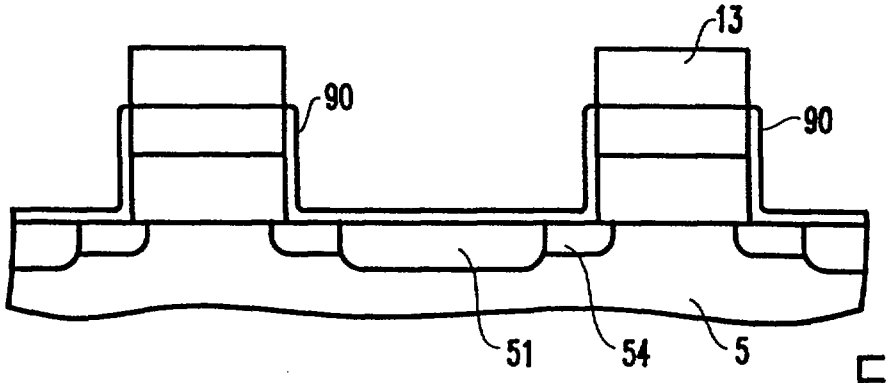


FIG.8B

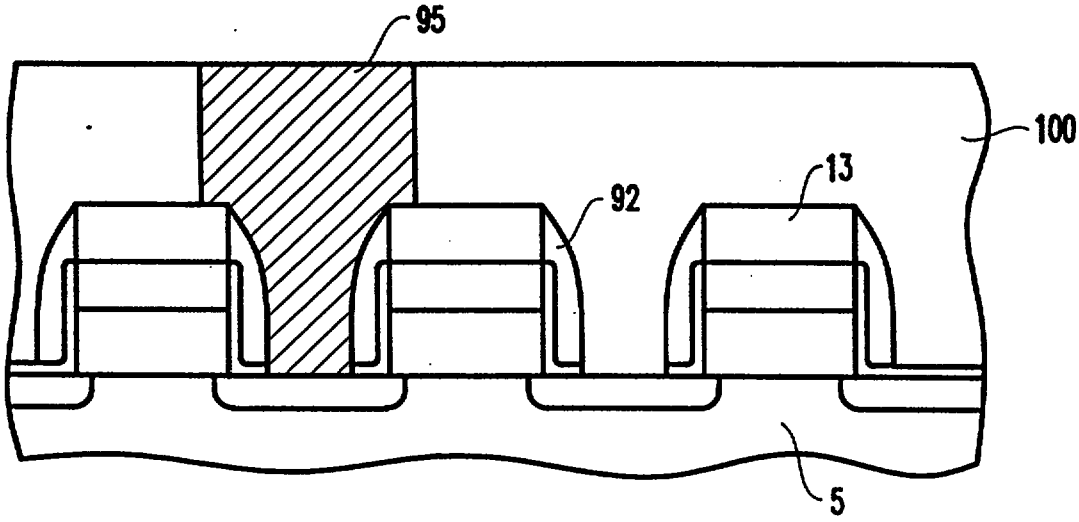


FIG.9A

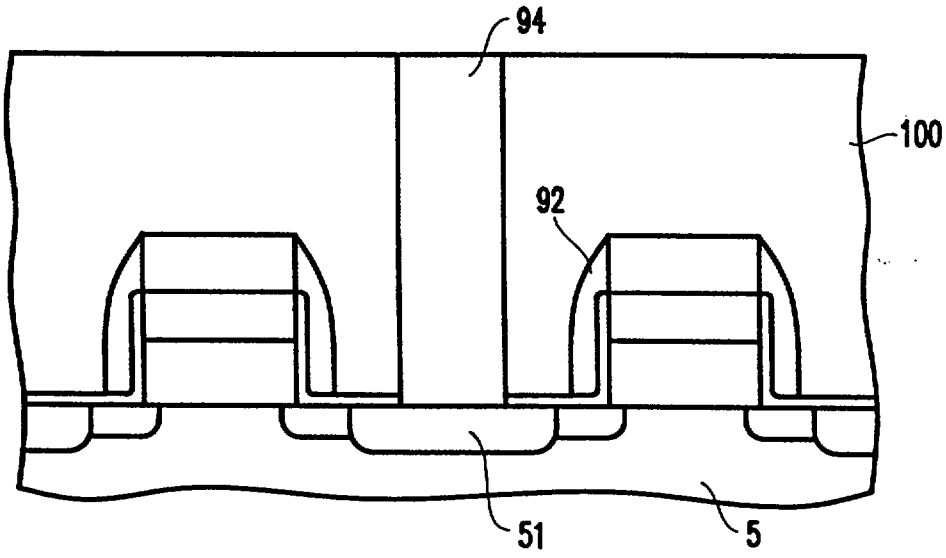


FIG.9B

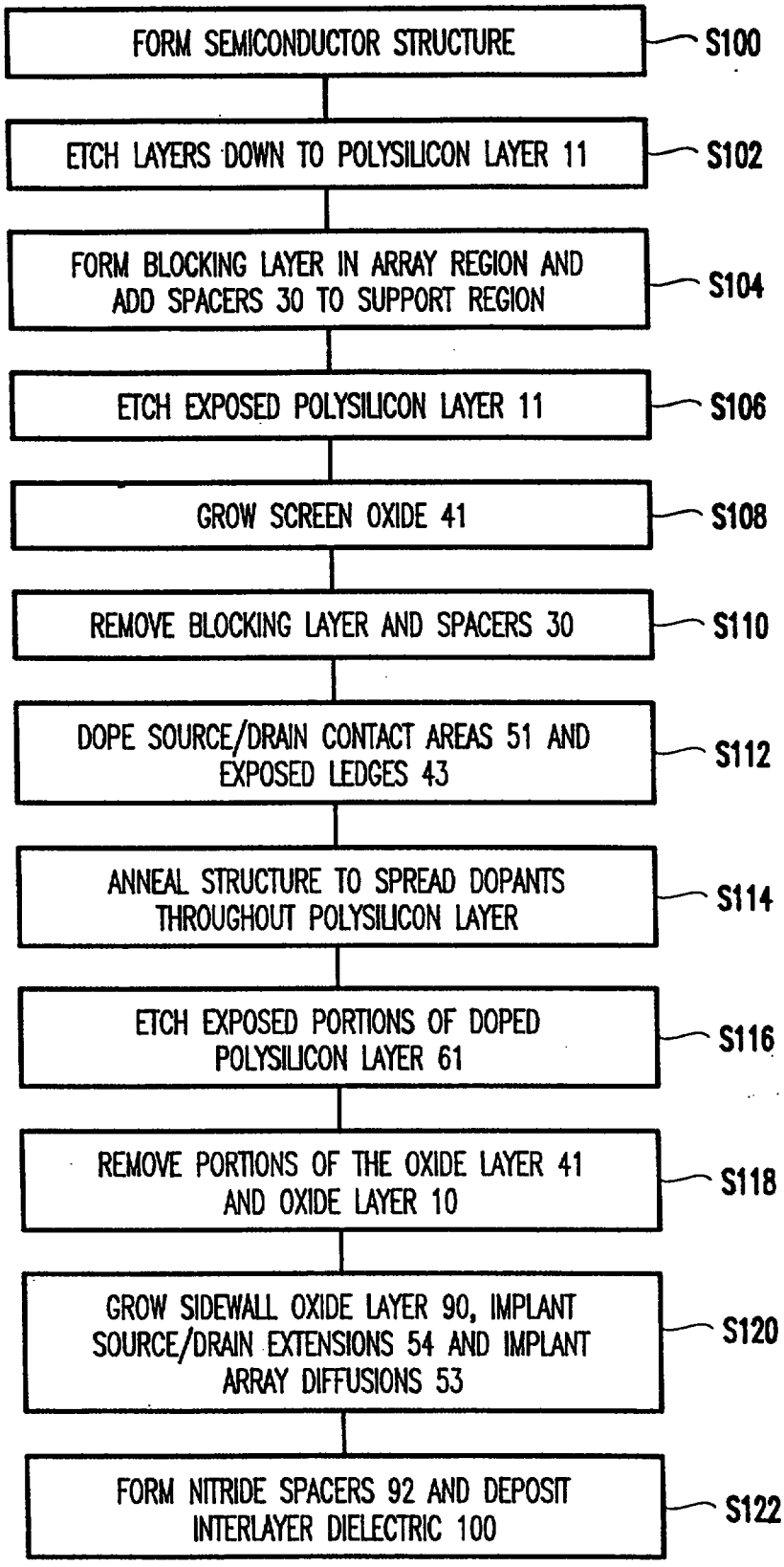

FORM SEMICONDUCTOR STRUCTURE
S100
ETCH LAYERS DOWN TO POLYSILICON LAYER 11
S102
FORM BLOCKING LAYER IN ARRAY REGION AND ADD SPACERS 30 TO SUPPORT REGION
S104
ETCH EXPOSED POLYSILICON LAYER 11
S106
GROW SCREEN OXIDE 41
S108
REMOVE BLOCKING LAYER AND SPACERS 30
S110
DOPE SOURCE/DRAIN CONTACT AREAS 51 AND EXPOSED LEDGES 43
S112
ANNEAL STRUCTURE TO SPREAD DOPANTS THROUGHOUT POLYSILICON LAYER
S114
ETCH EXPOSED PORTIONS OF DOPED POLYSILICON LAYER 61
S116
REMOVE PORTIONS OF THE OXIDE LAYER 41 AND OXIDE LAYER 10
S118
GROW SIDEWALL OXIDE LAYER 90, IMPLANT SOURCE/DRAIN EXTENSIONS 54 AND IMPLANT ARRAY DIFFUSIONS 53
S120
FORM NITRIDE SPACERS 92 AND DEPOSIT INTERLAYER DIELECTRIC 100
S122

FIG.10