

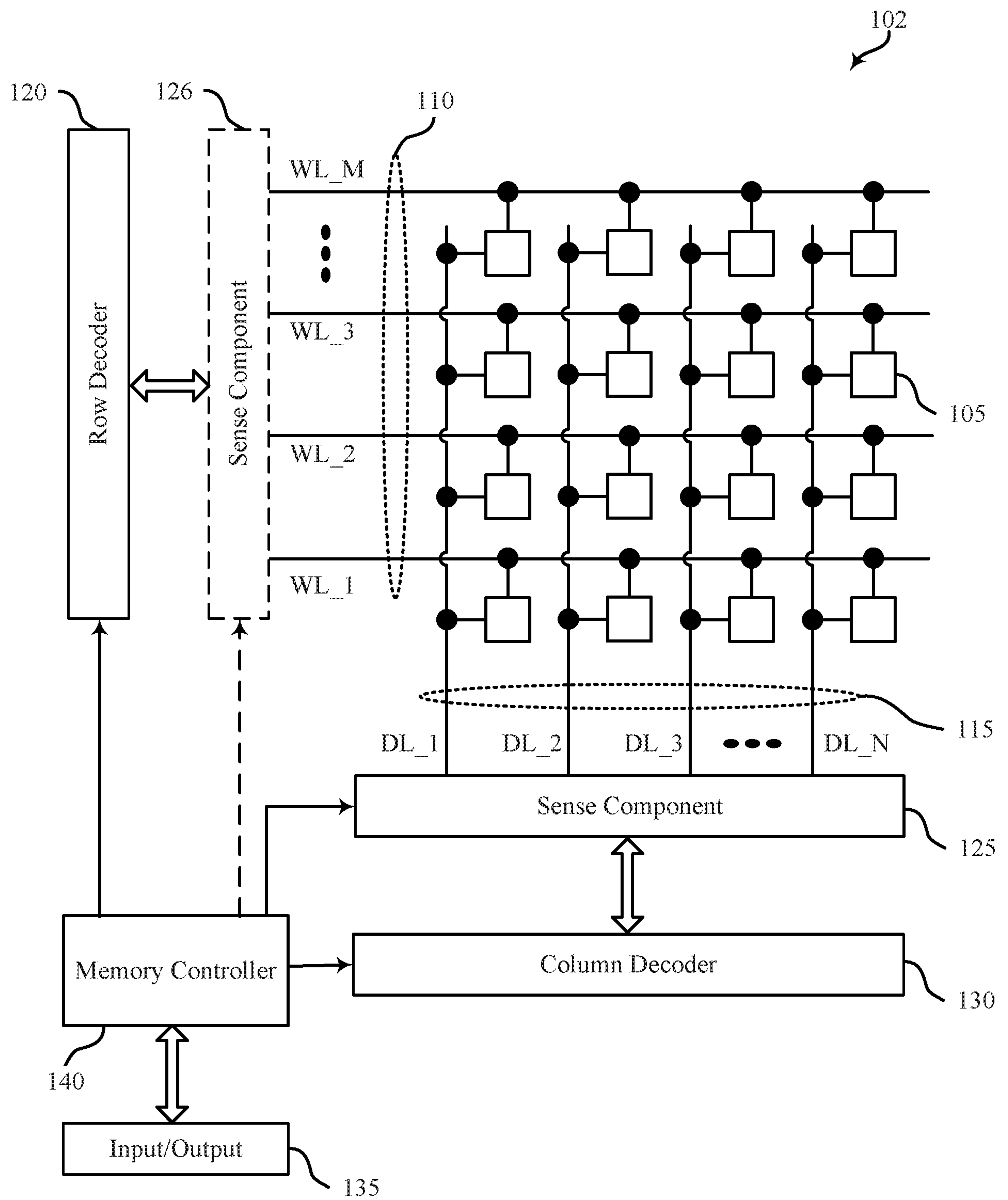


FIG. 1

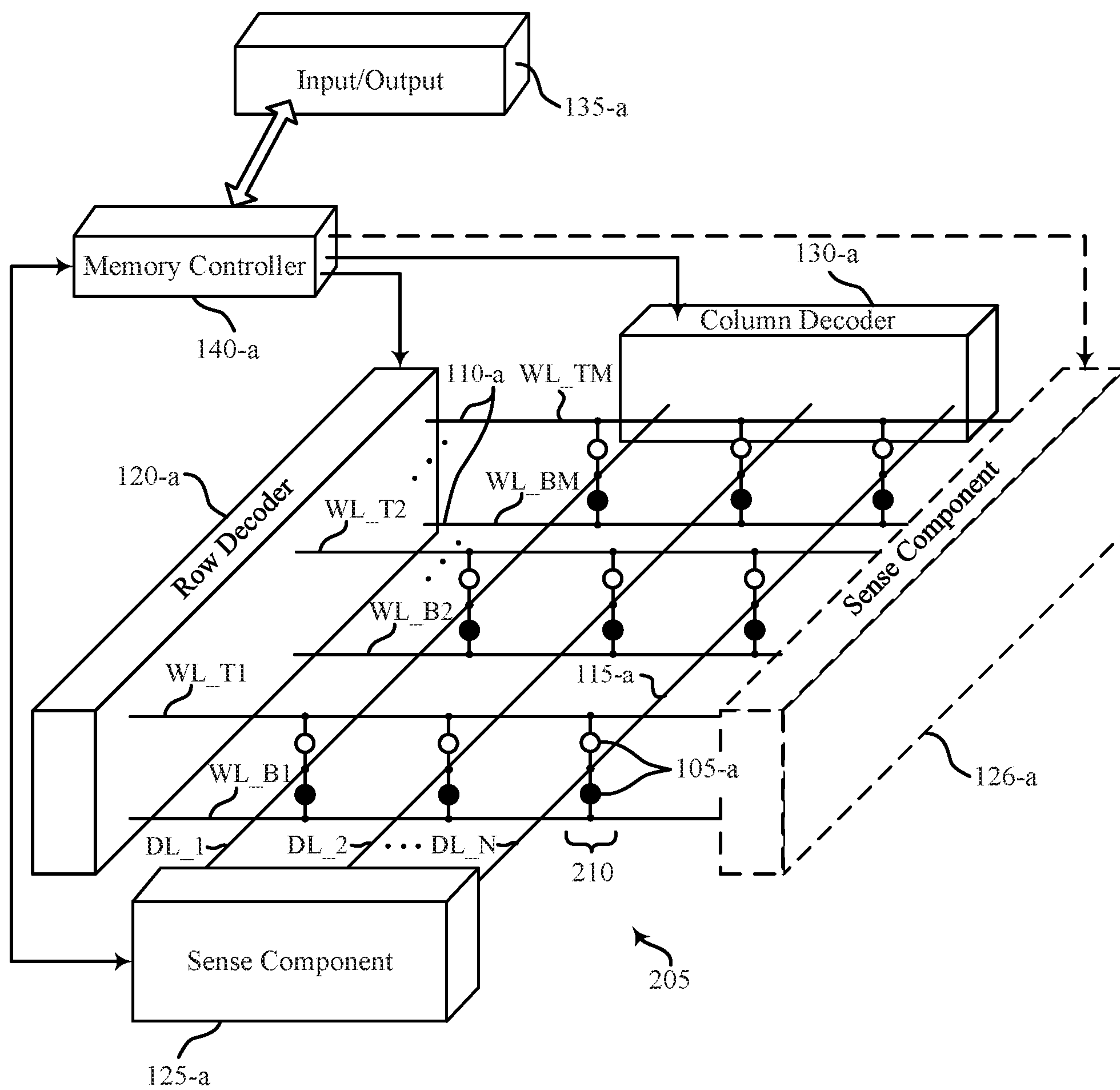


FIG. 2

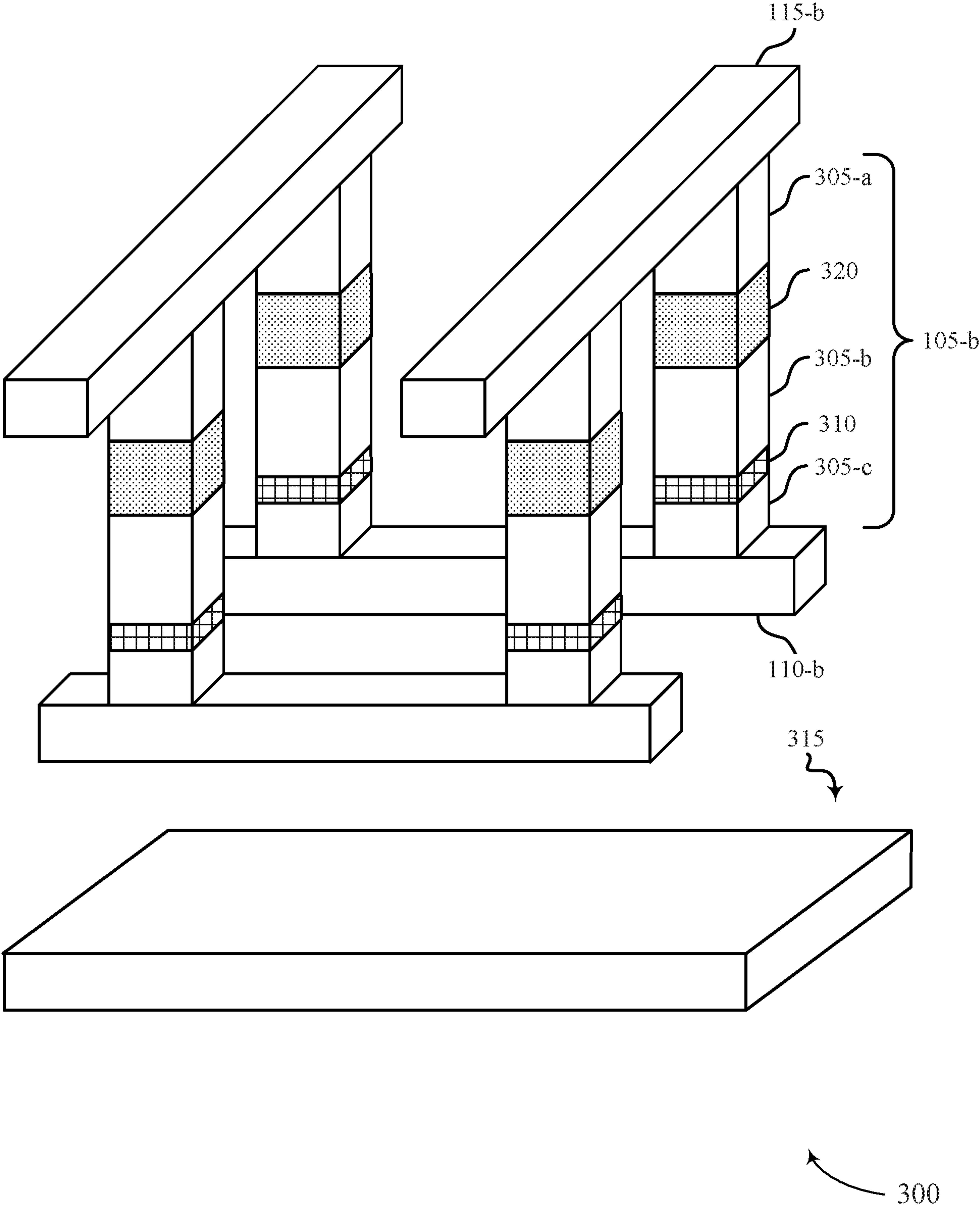
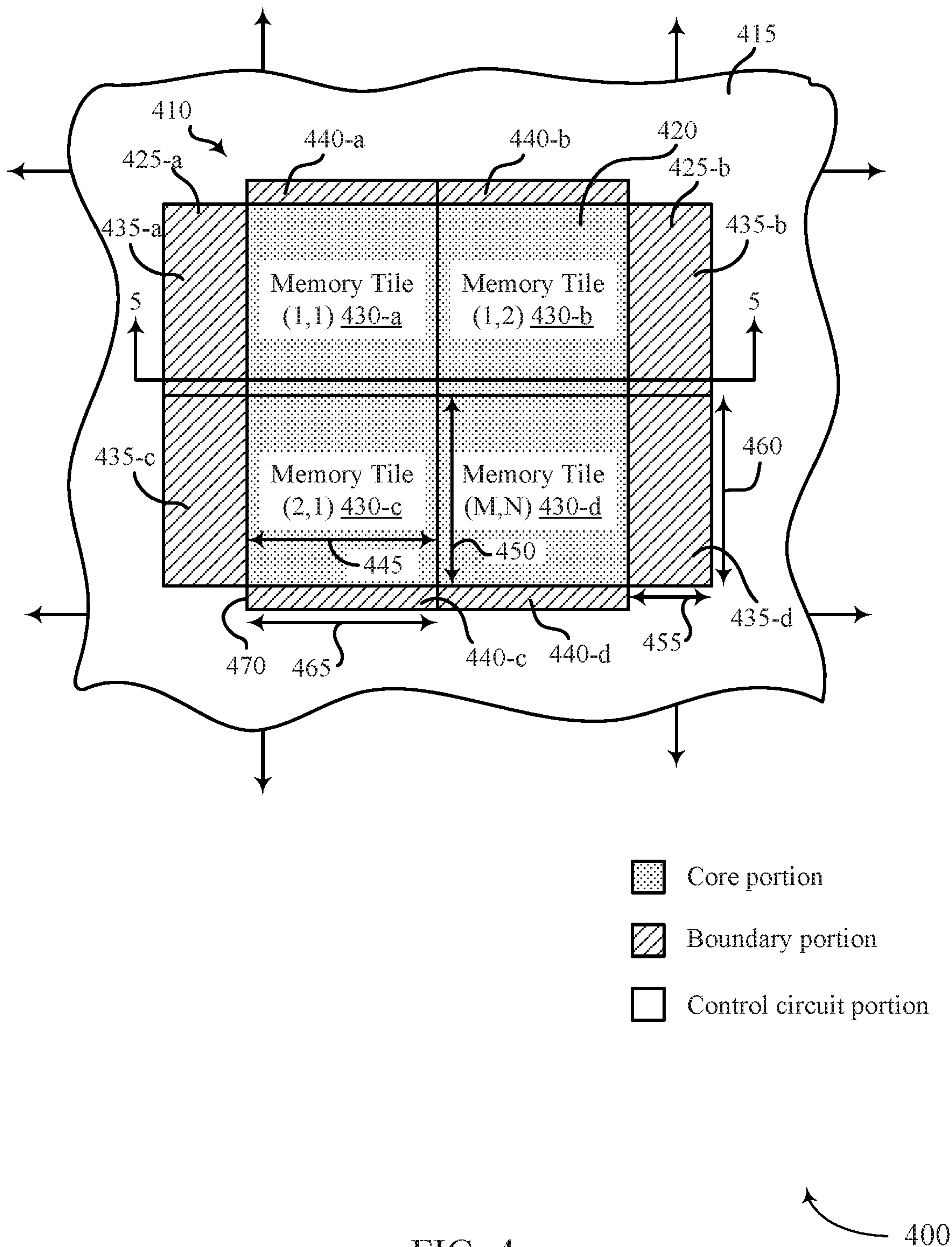


FIG. 3



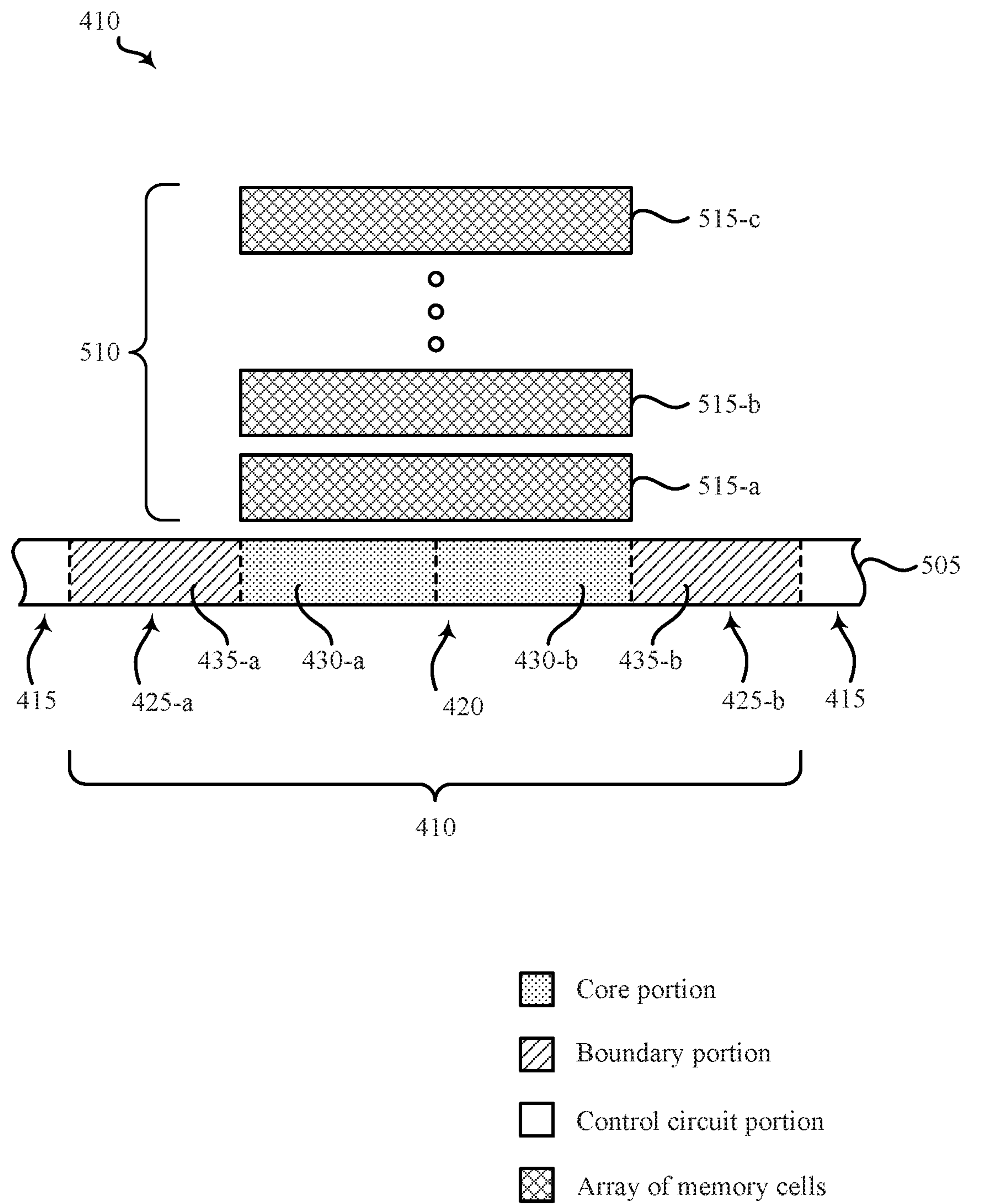
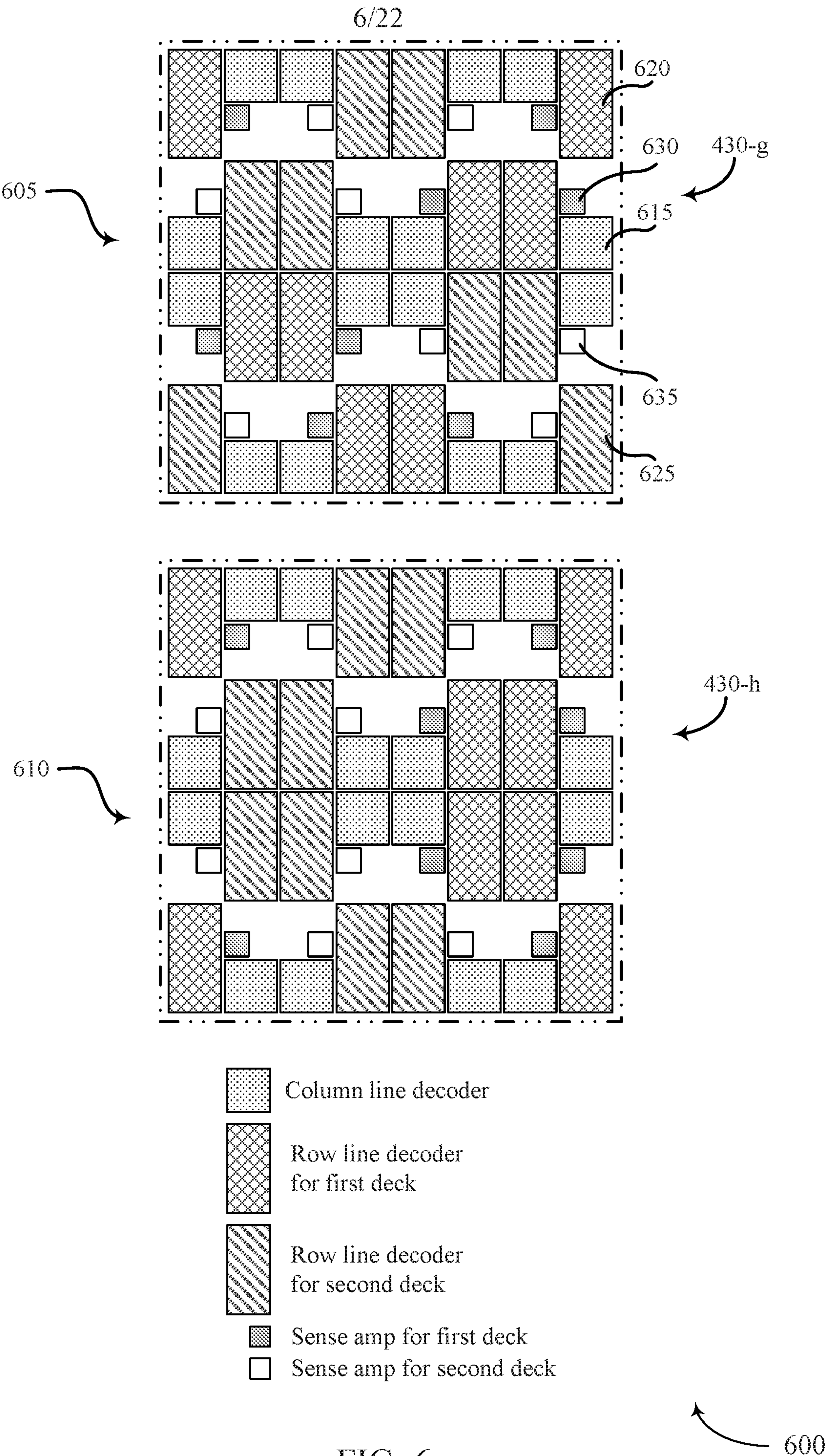


FIG. 5



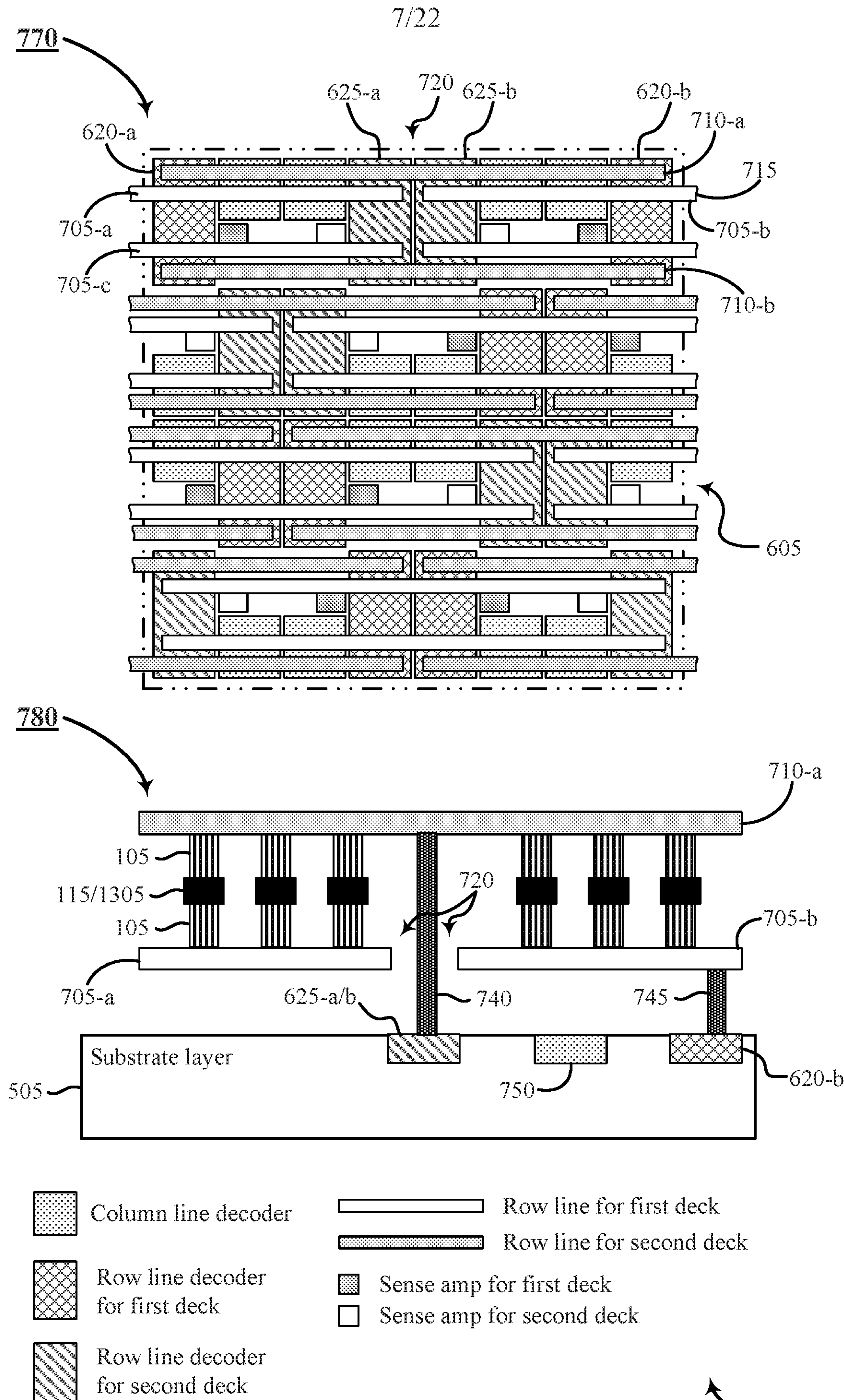


FIG. 7

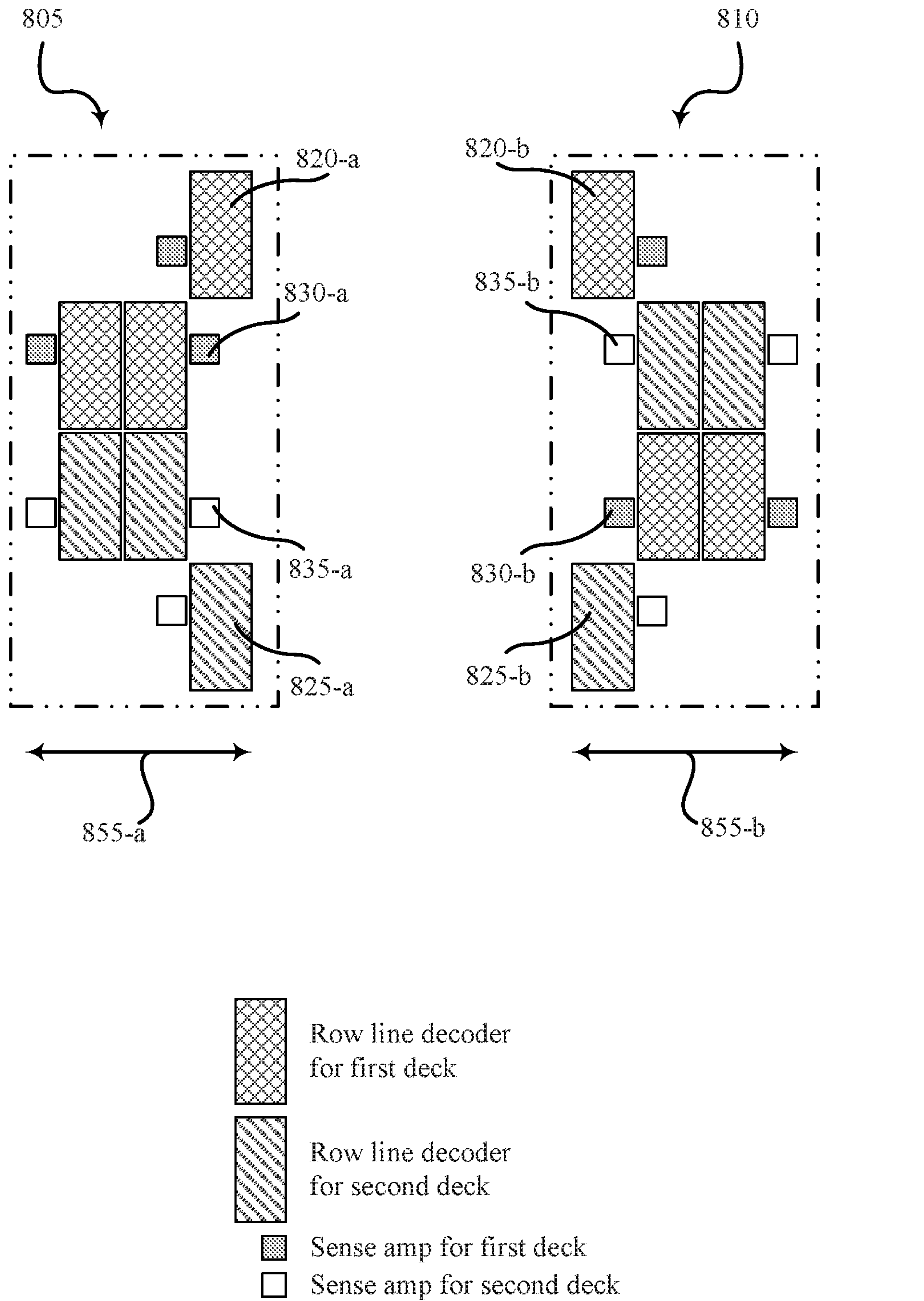


FIG. 8

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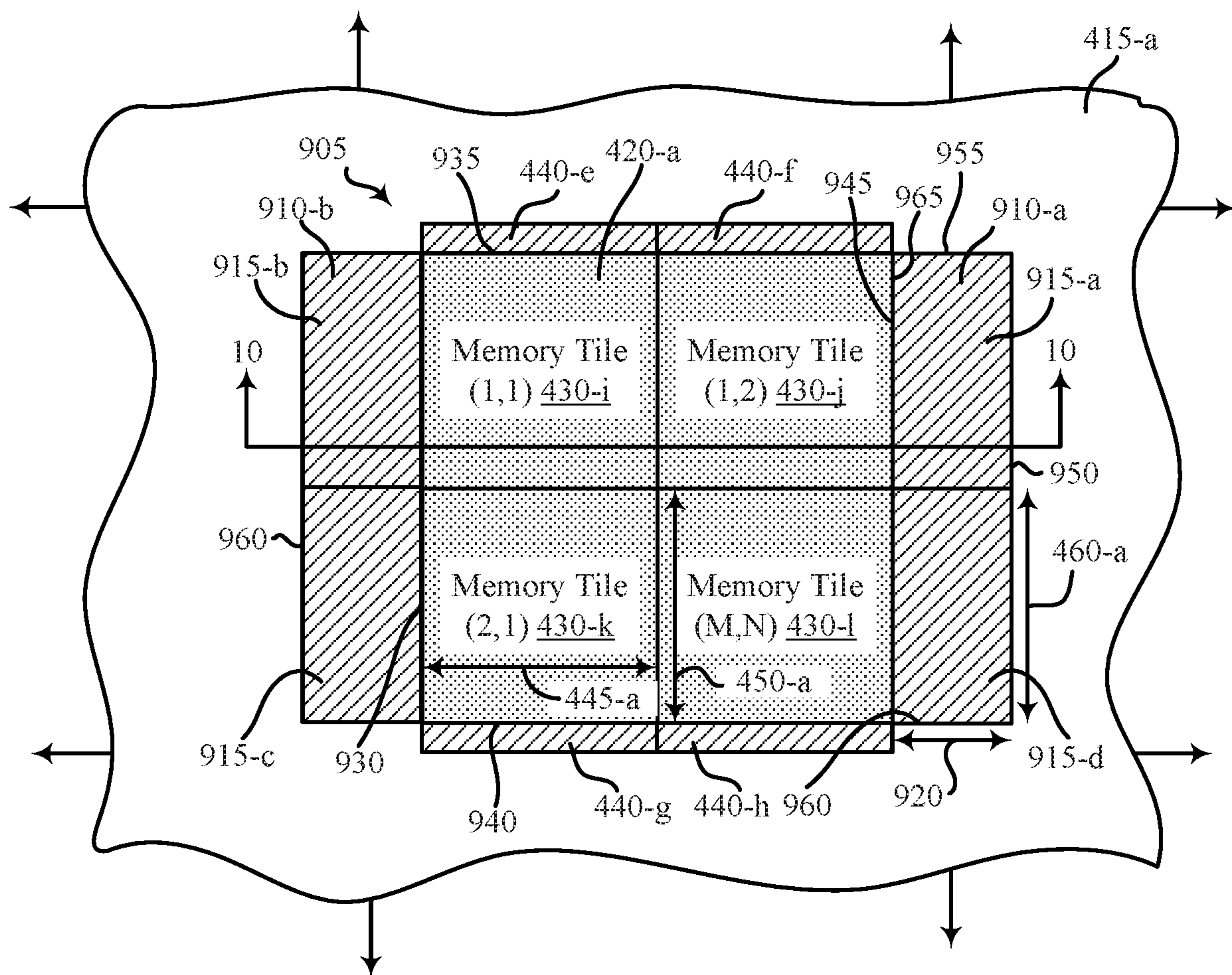
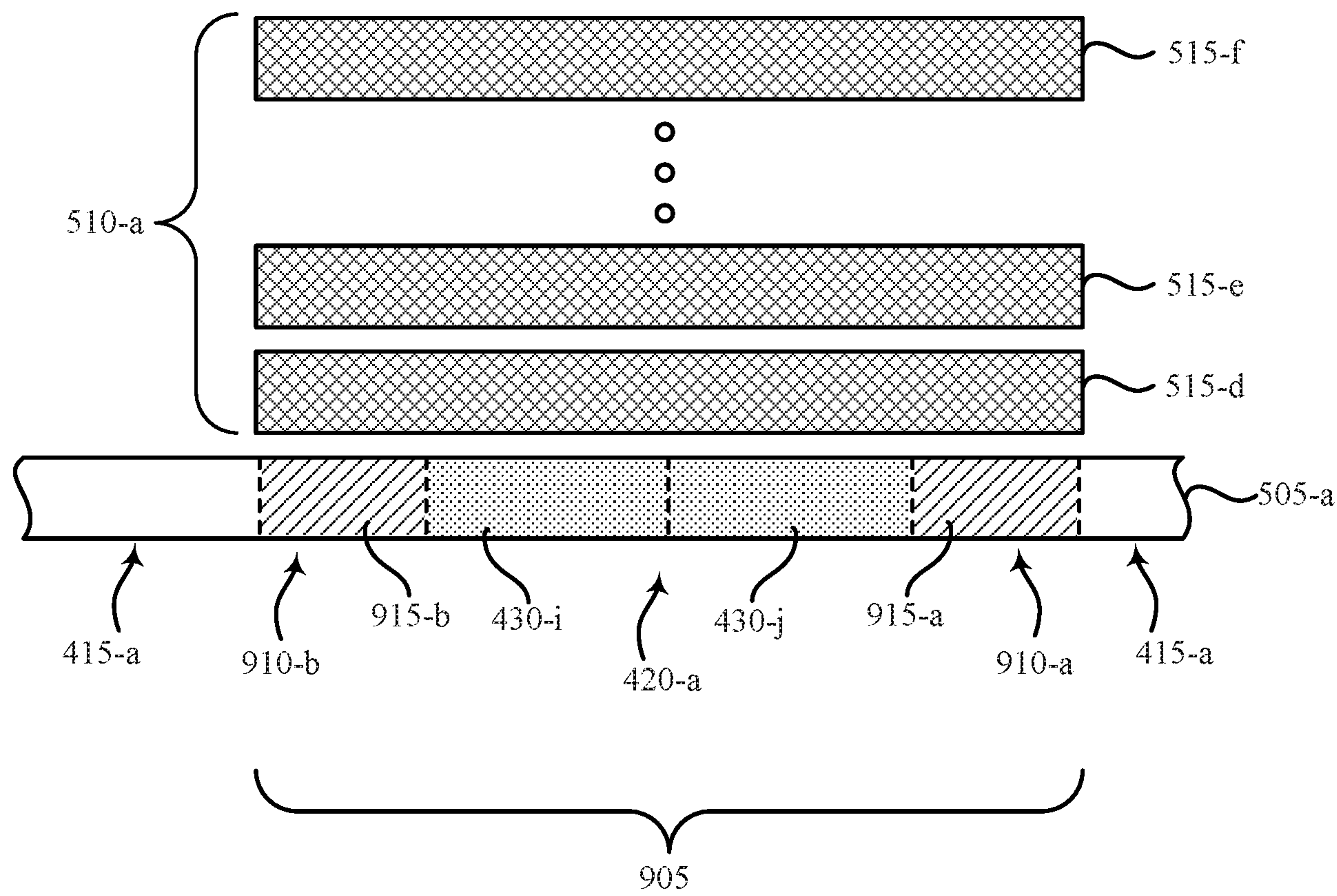


FIG. 9

900



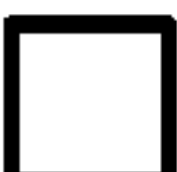
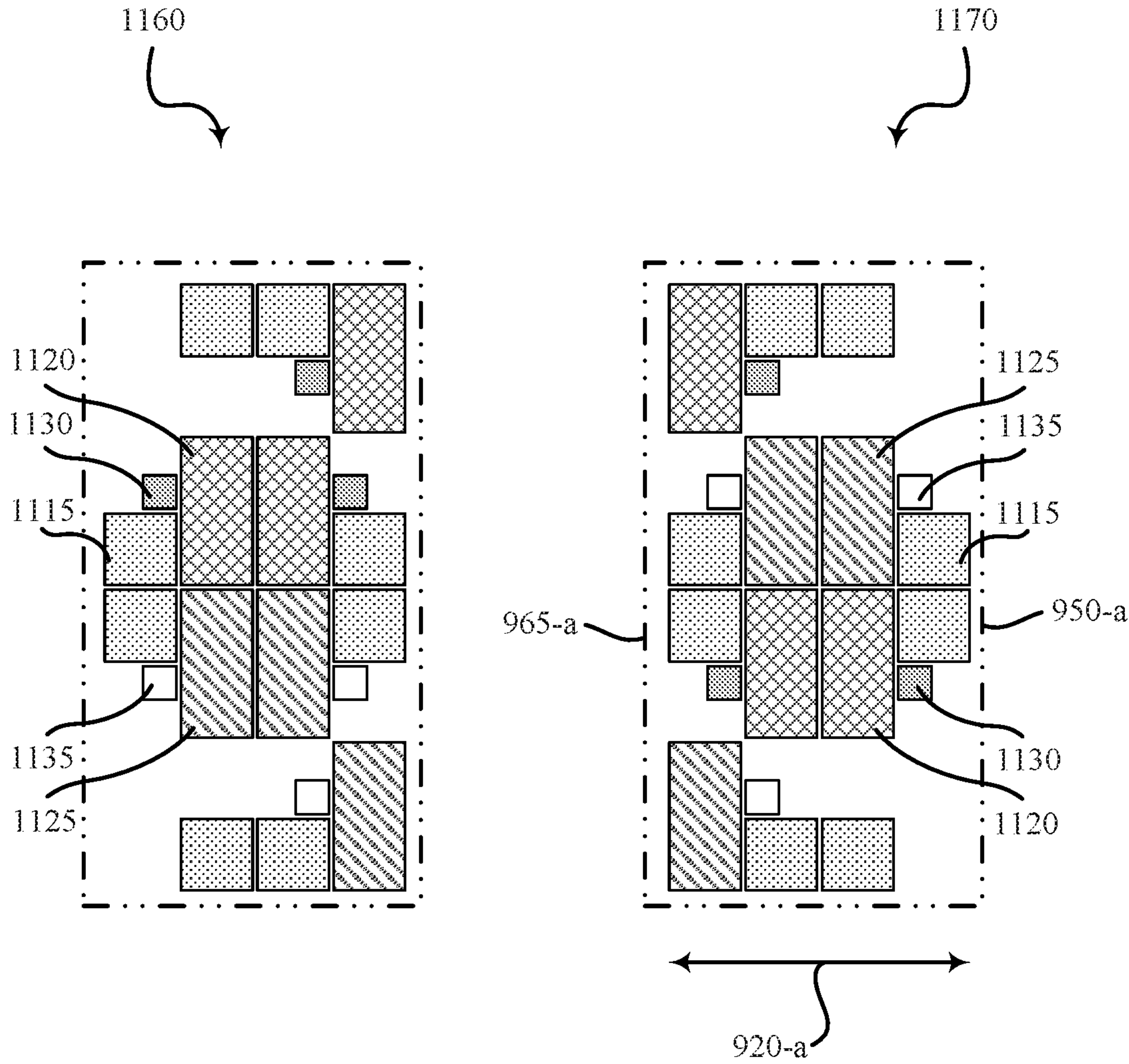
-  Core portion
-  Boundary portion
-  Control circuit portion
-  Array of memory cells

FIG. 10

1000



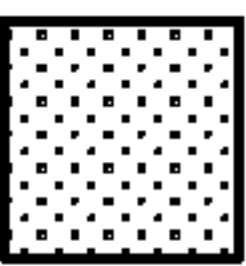
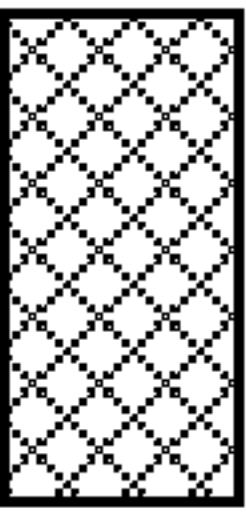
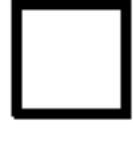
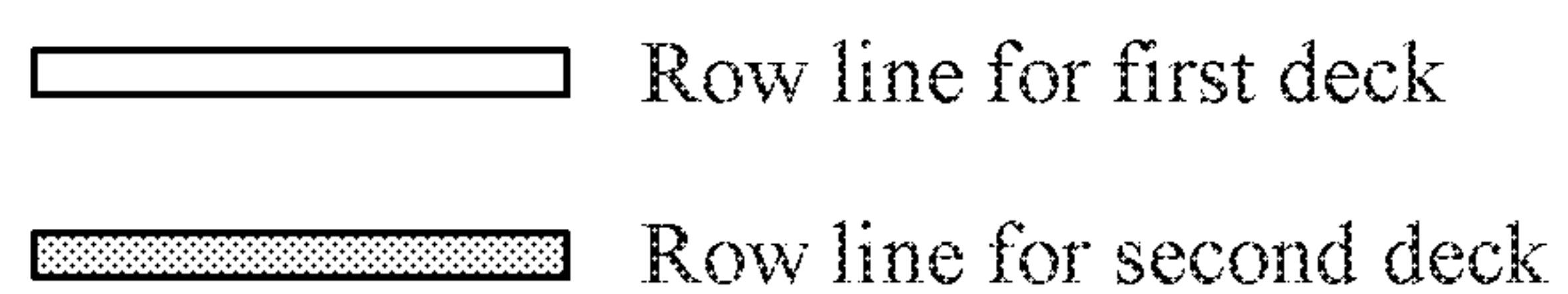
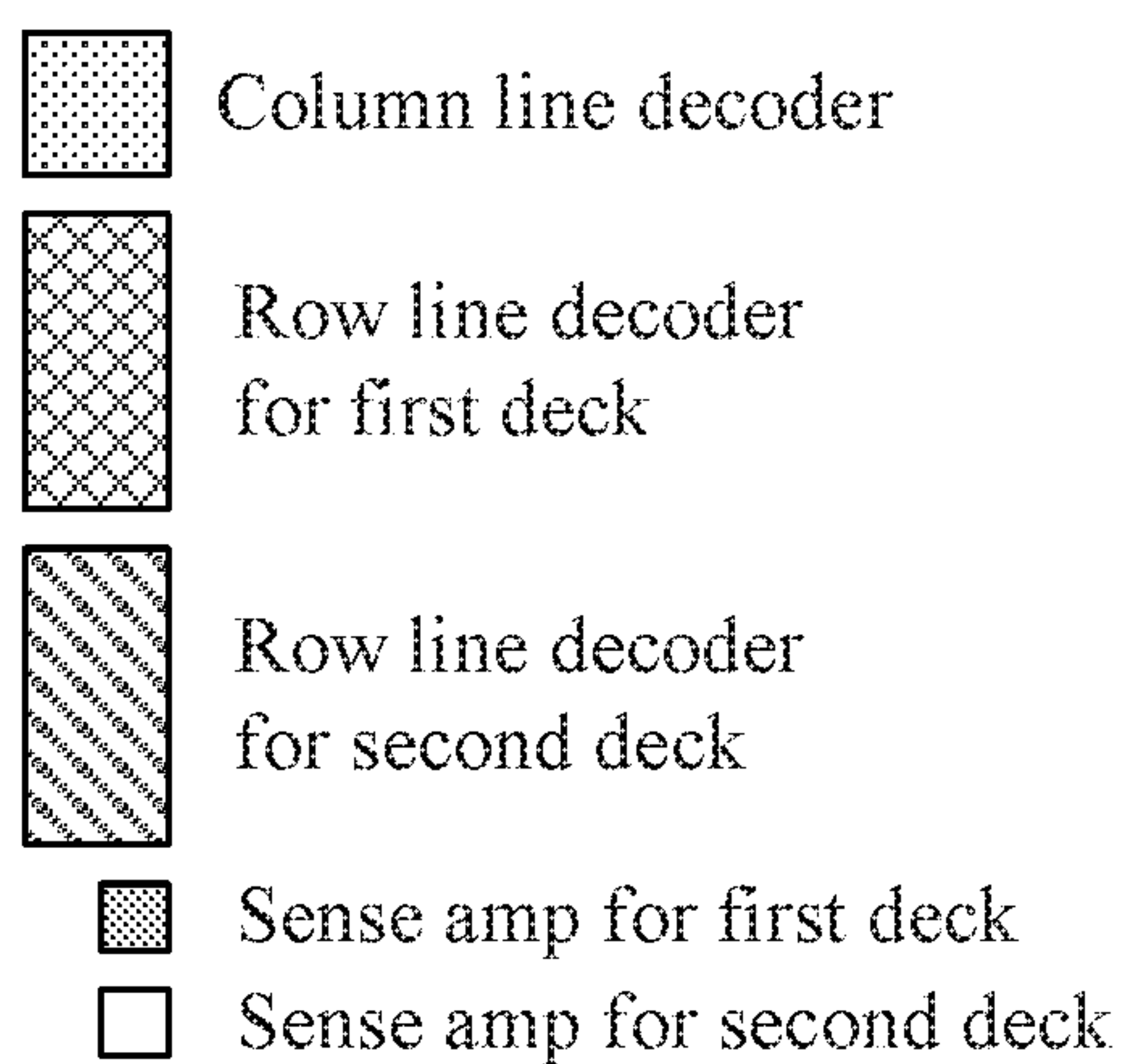
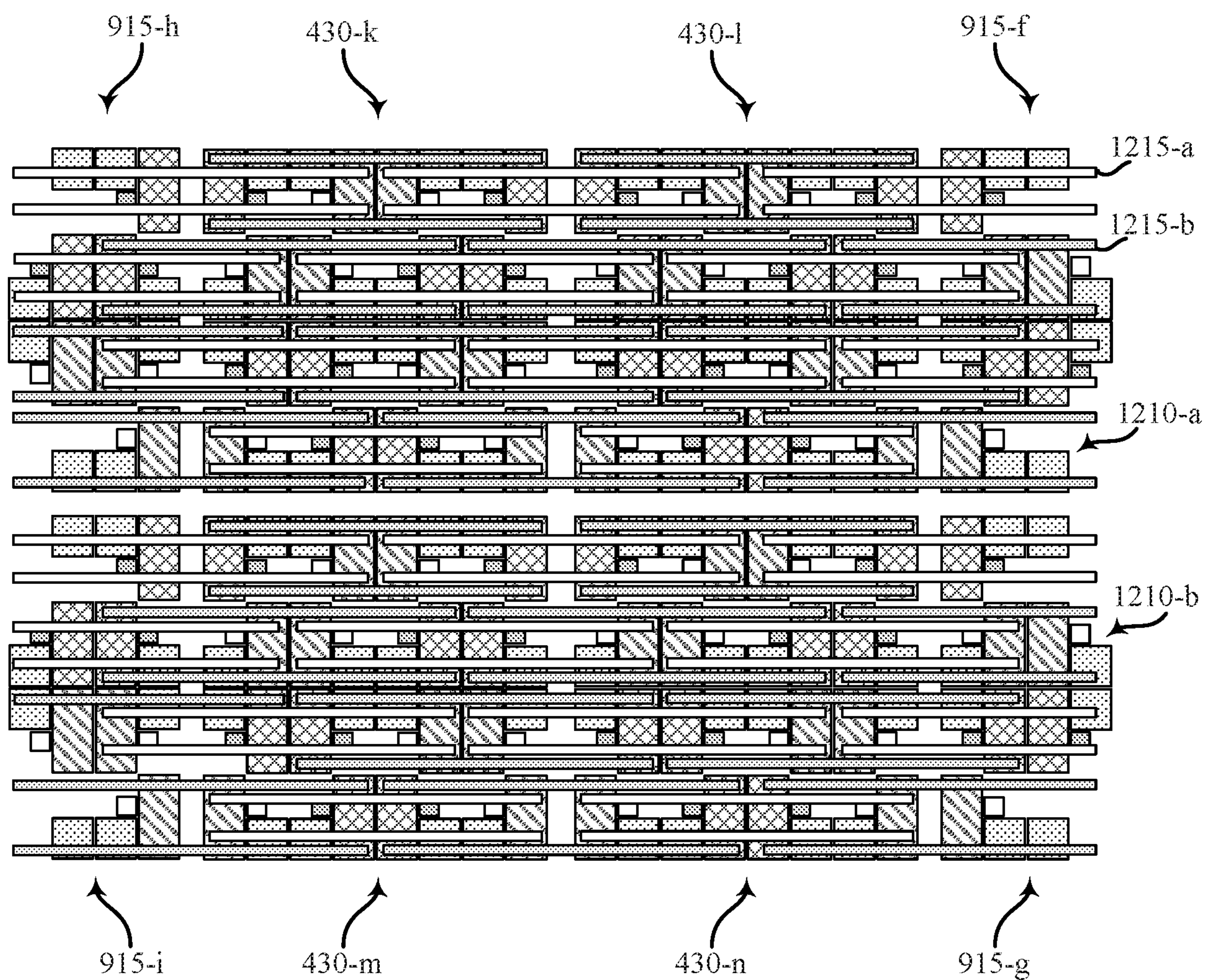
-  Column line decoder
-  Row line decoder for first deck
-  Row line decoder for second deck
-  Sense amp for first deck
-  Sense amp for second deck

FIG. 11

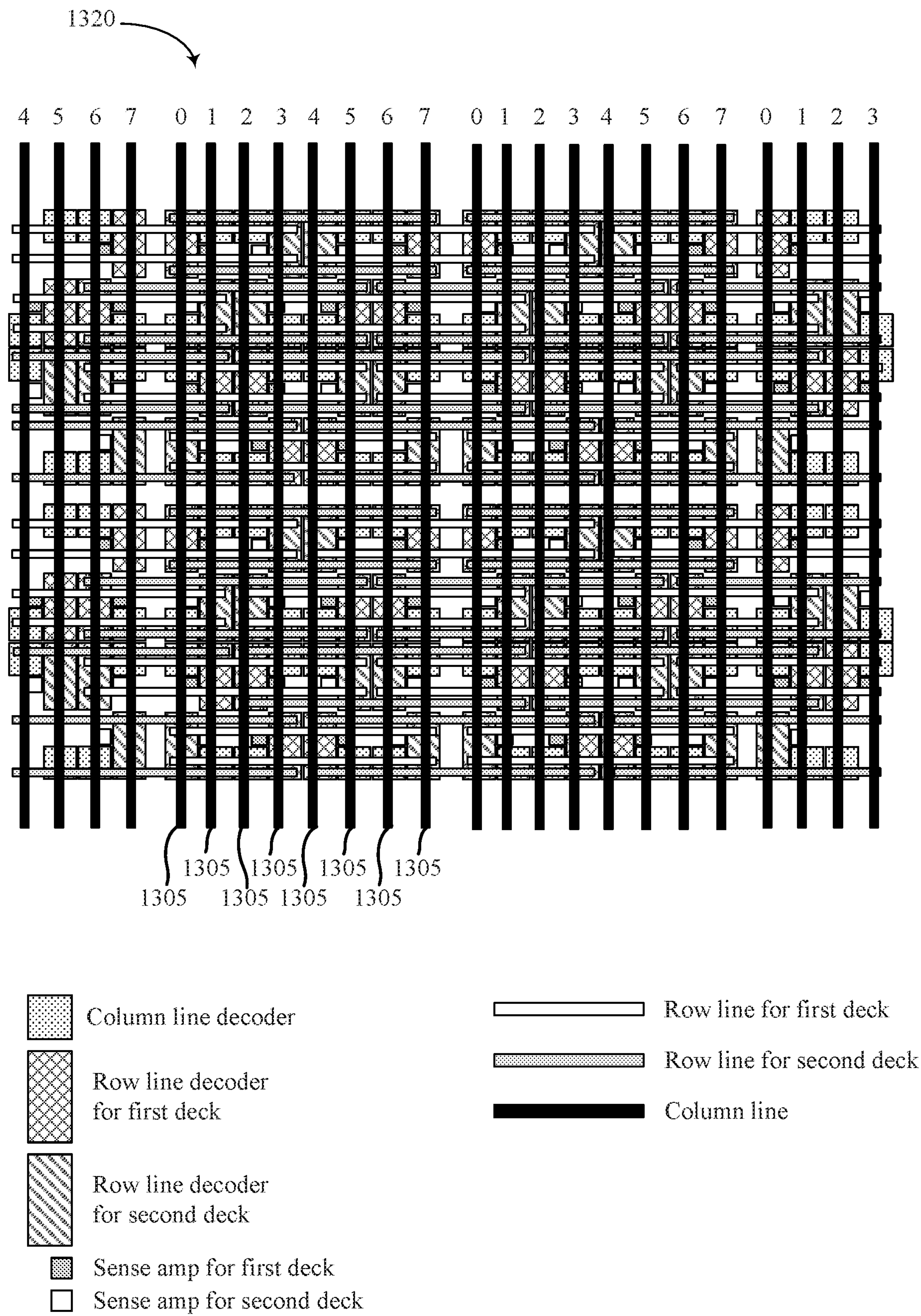
1100

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1200

FIG. 12



1300

FIG. 13

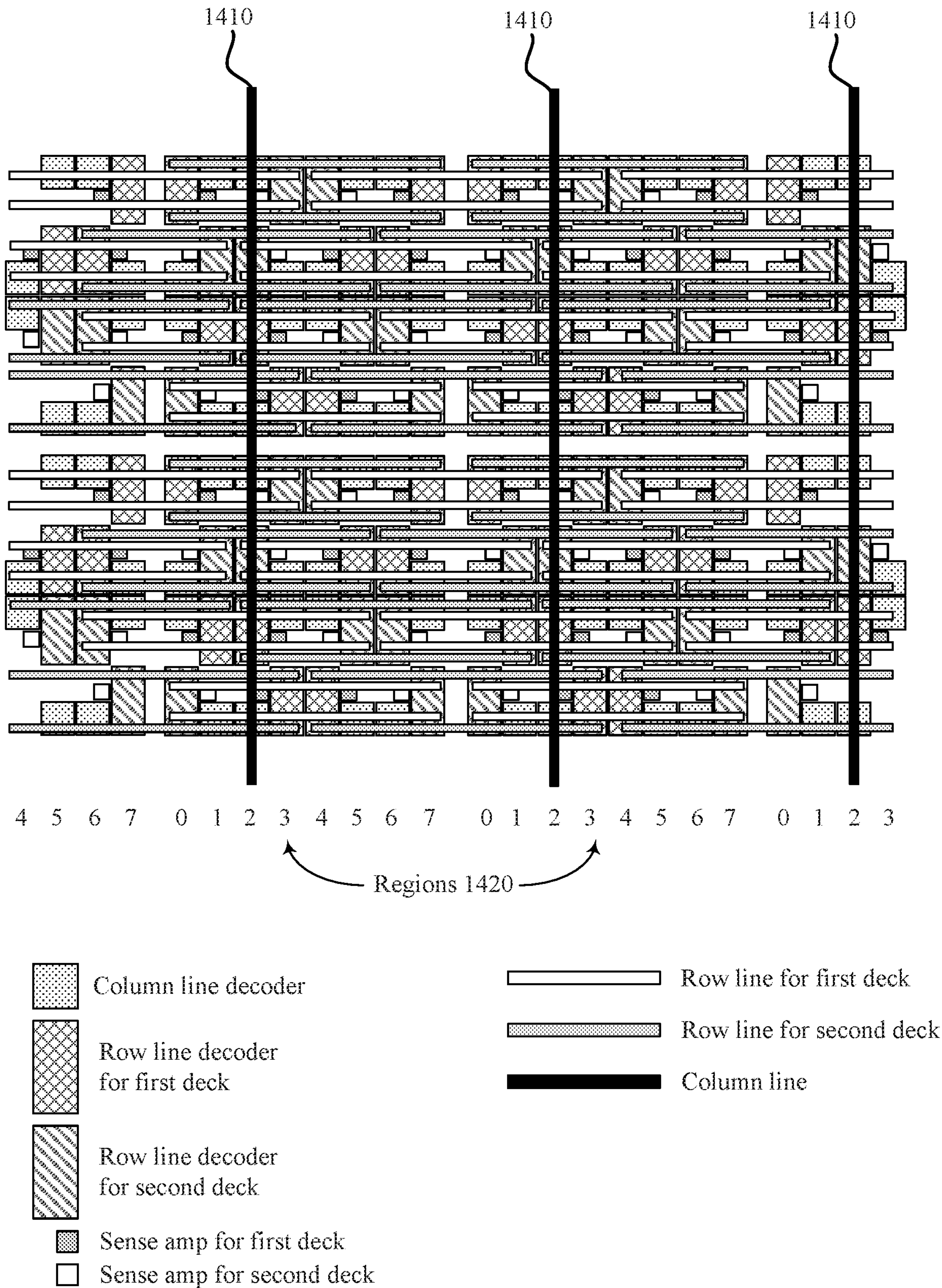


FIG. 14

1400

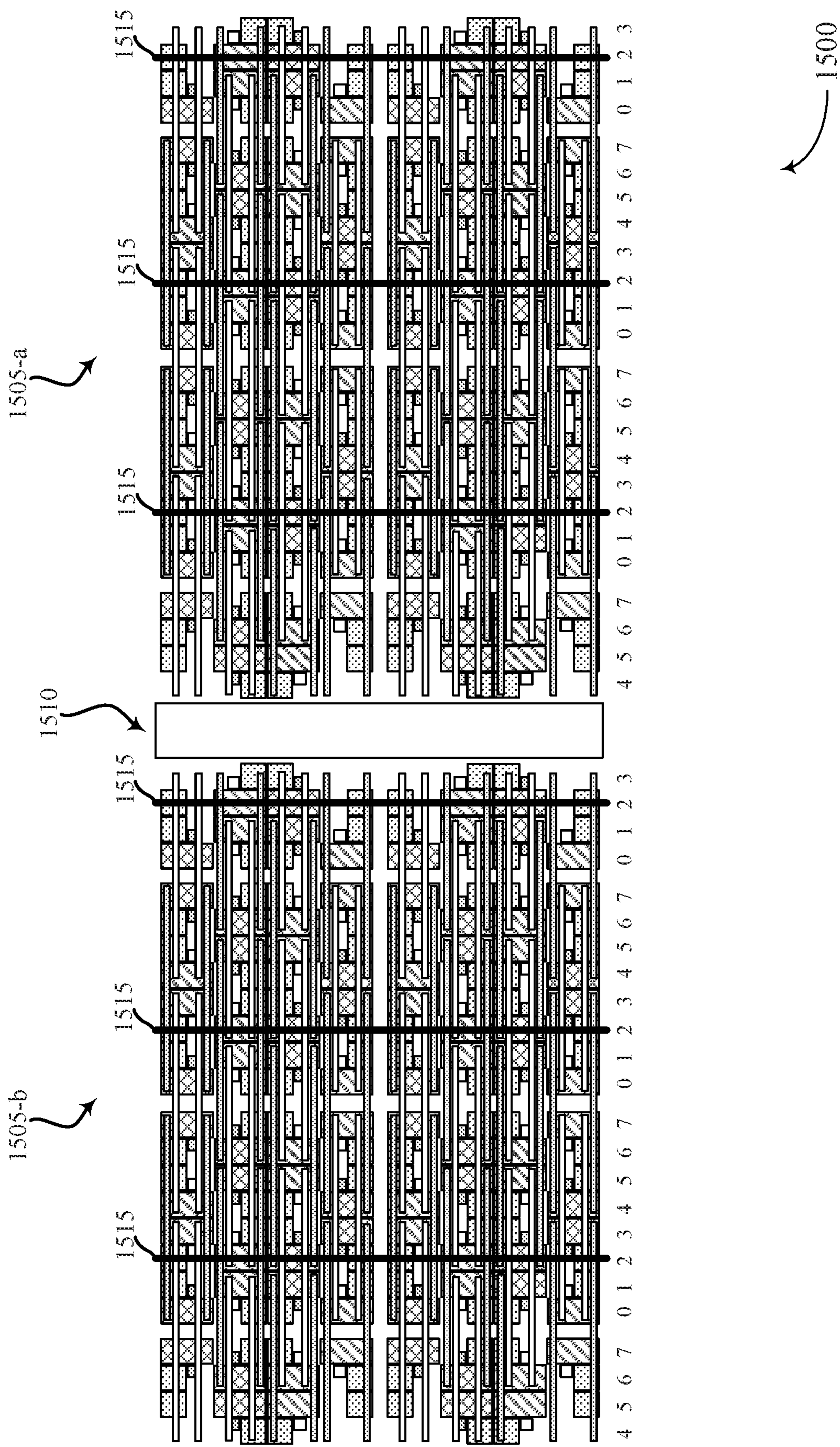


FIG. 15

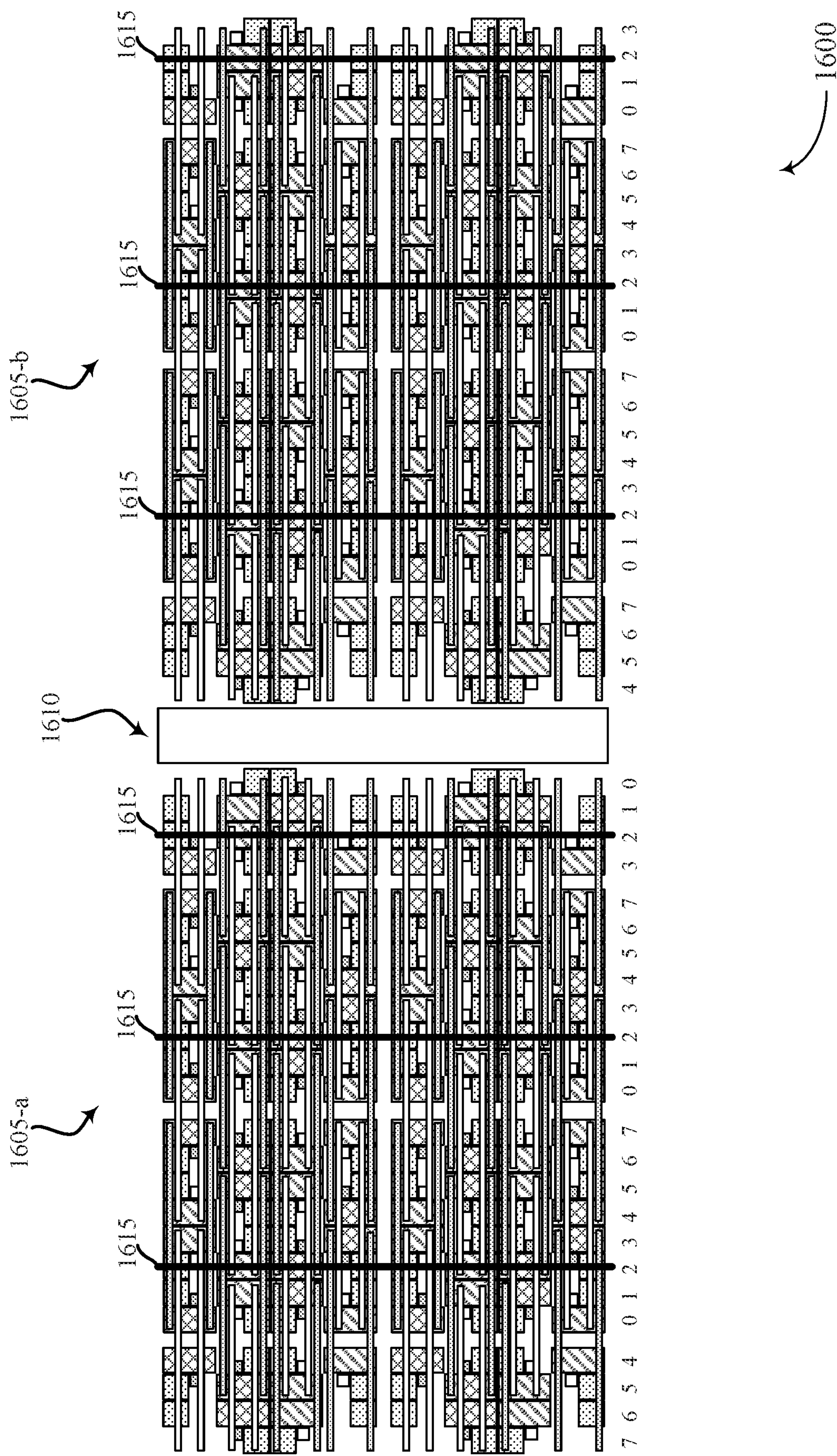


FIG. 16

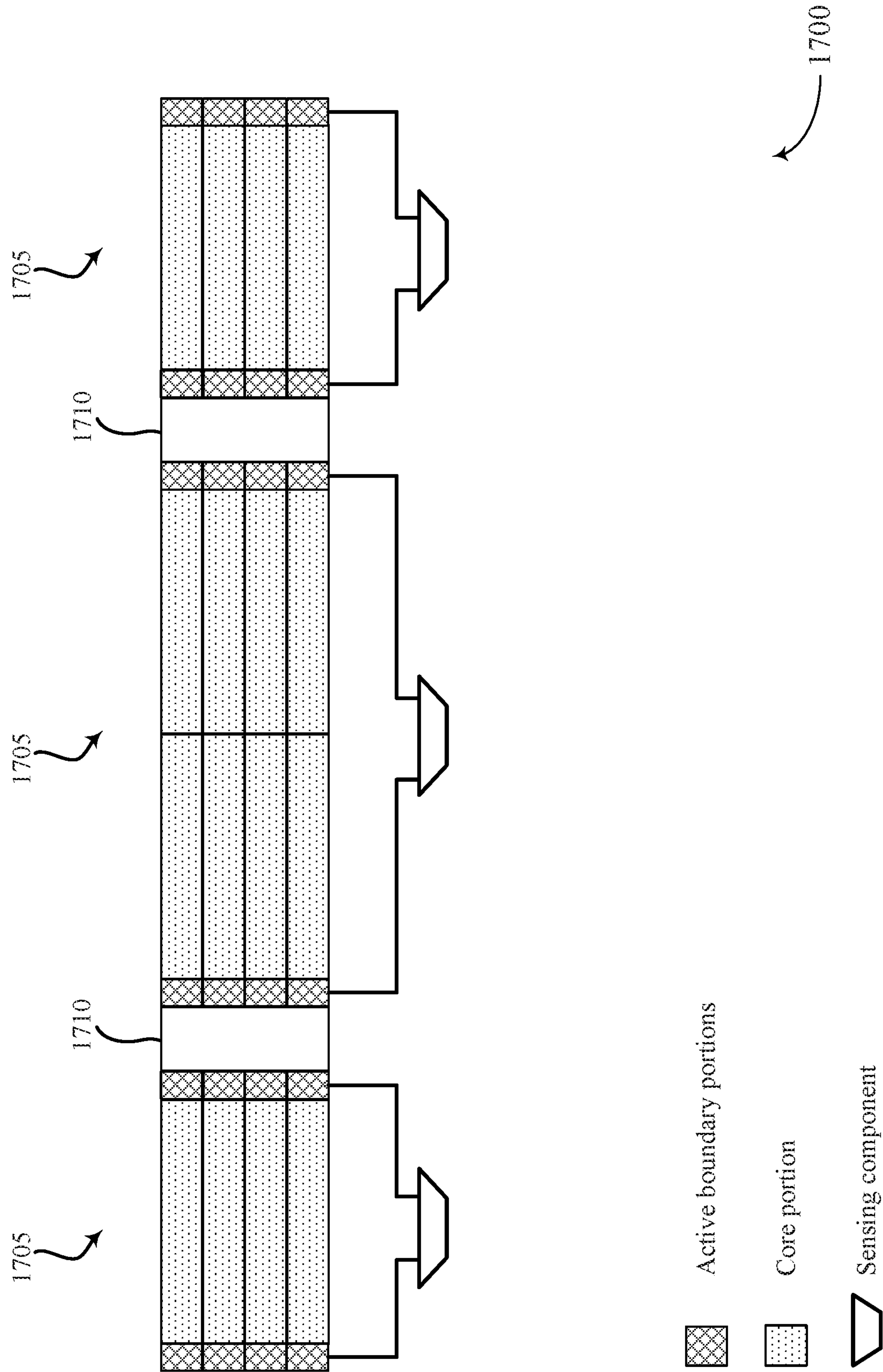


FIG. 17

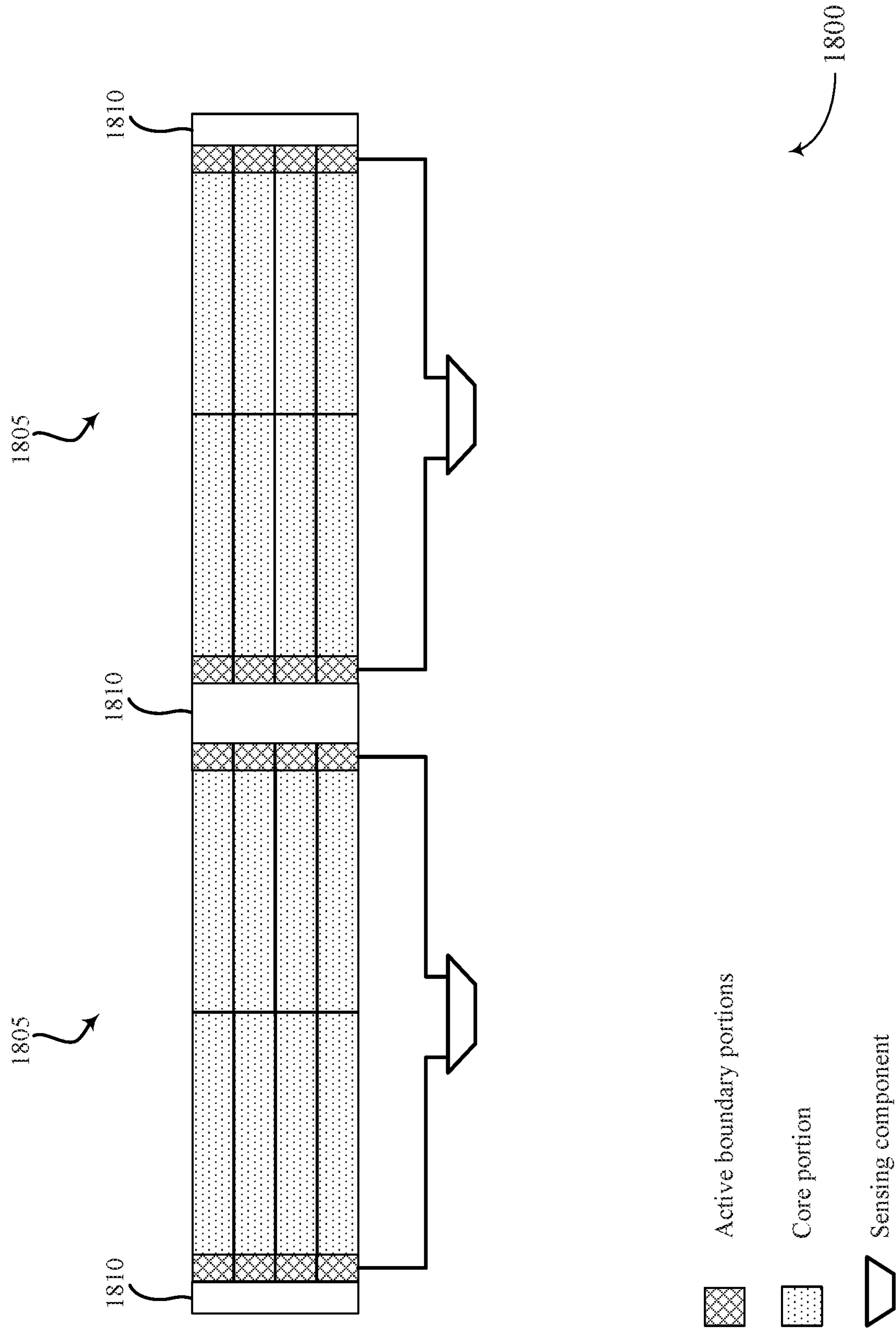


FIG. 18

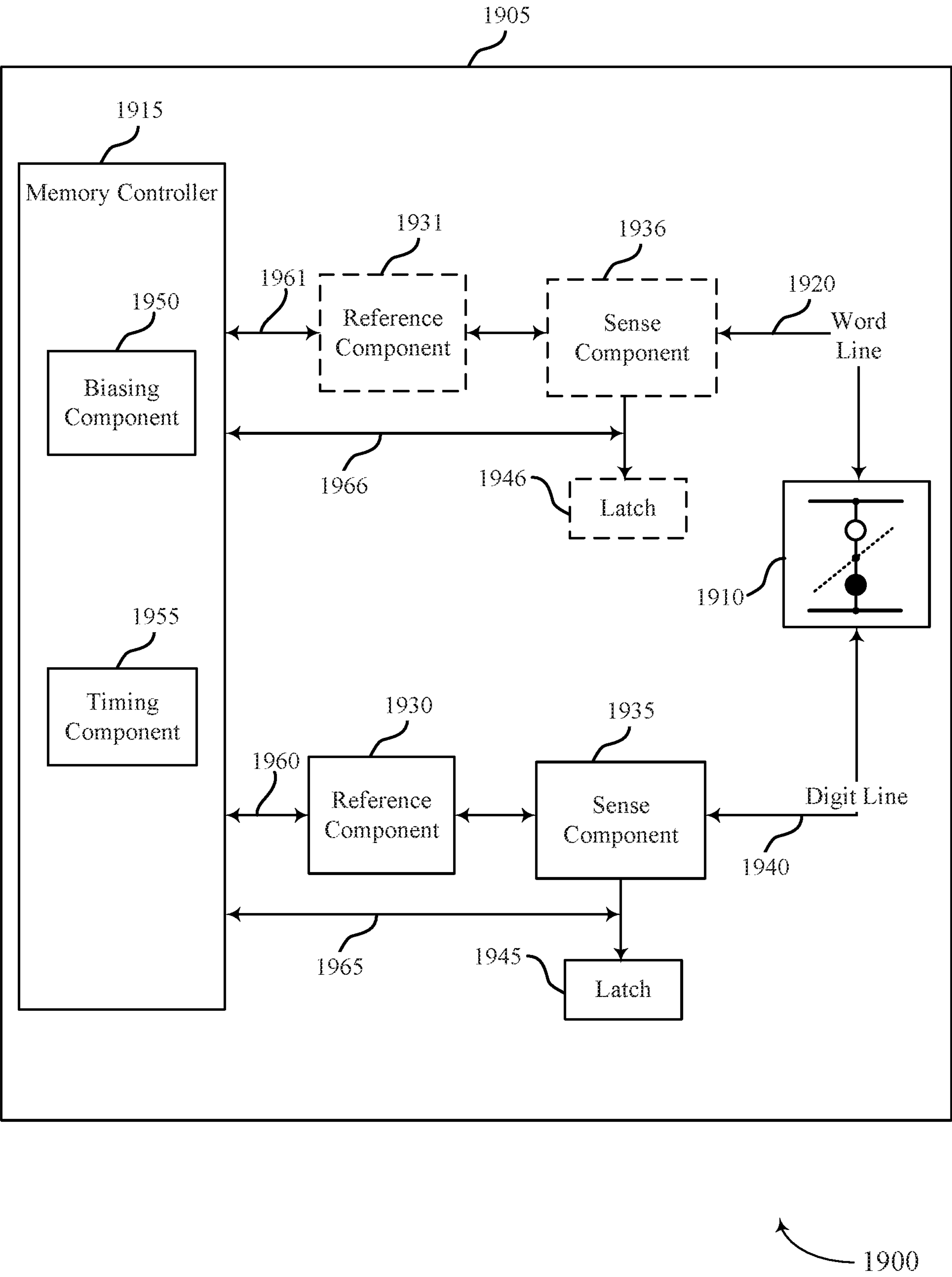


FIG. 19

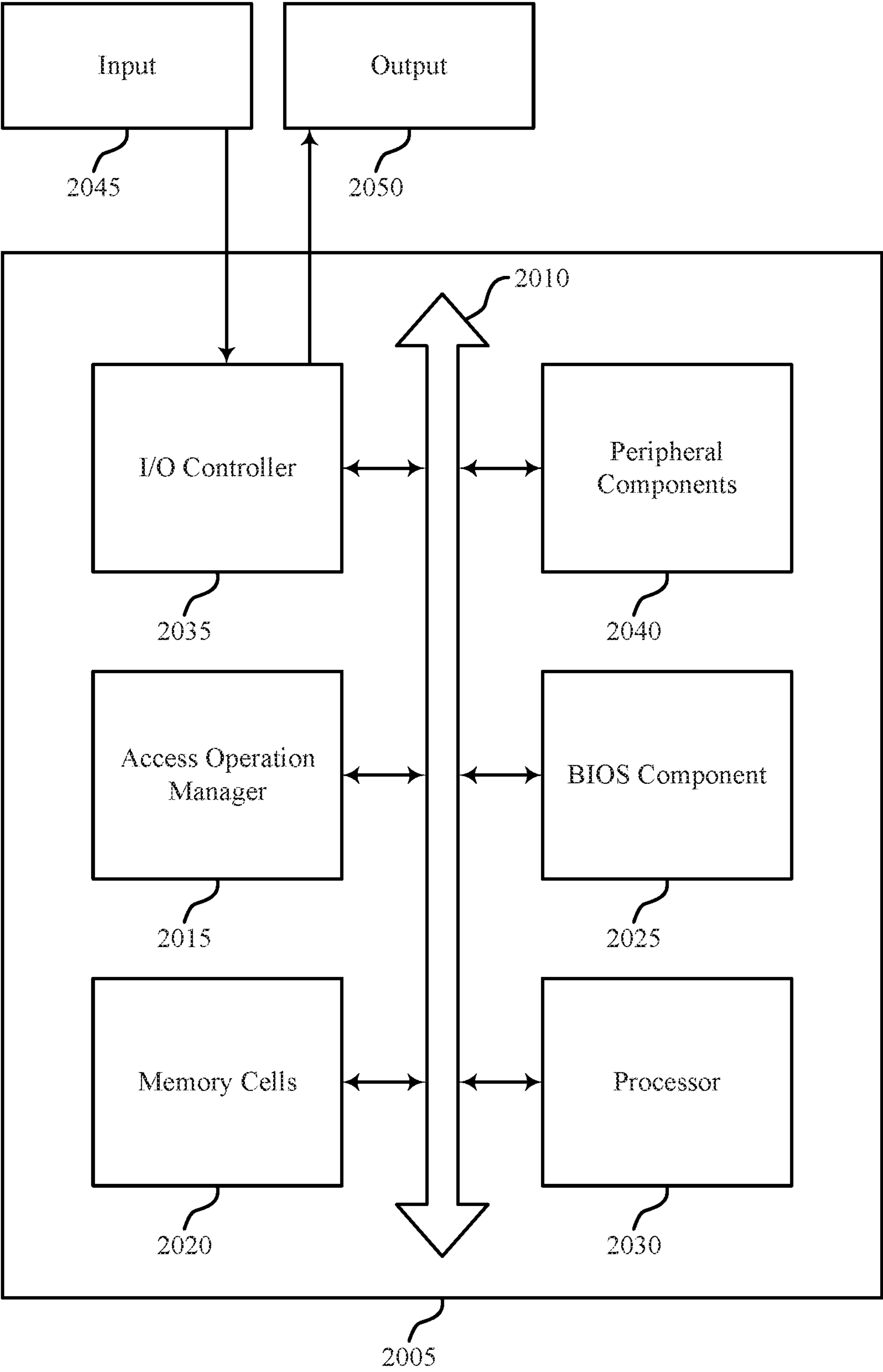


FIG. 20

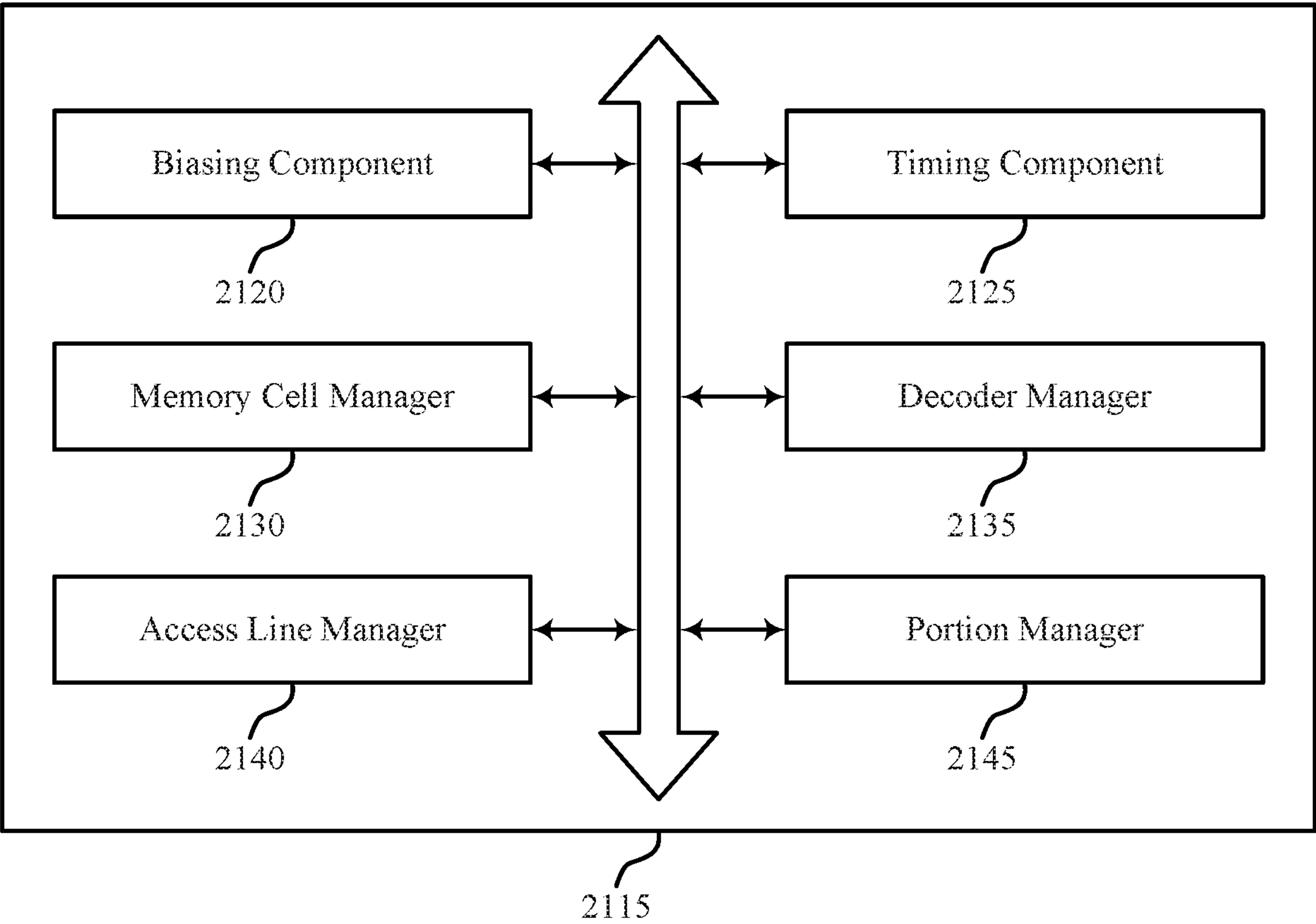


FIG. 21

2100

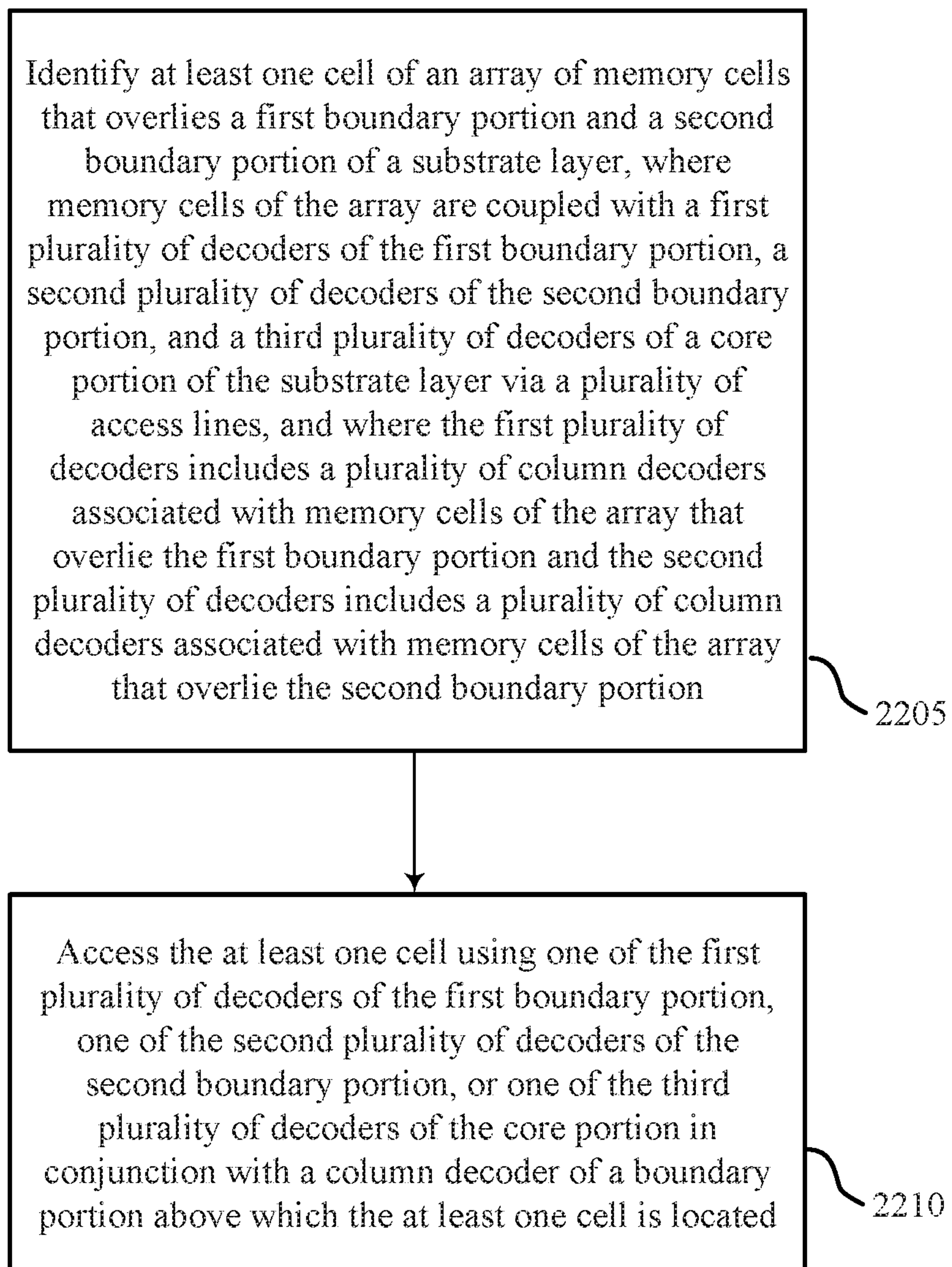


FIG. 22