

at one side of the semiconductor chip in a laminating direction for fixing the semiconductor chip to the substrate or to another semiconductor chip mounted adjacent to the one side in the laminating direction, and the permissible temperature is less than a curing start temperature at which the thermosetting resin starts to cure irreversibly.

5 **[0012]** In another effective aspect, a map forming step of forming a map indicating formation positions of the plurality of chip stacks based on the specified separation distance is further included, wherein in the temporary crimping step, the plurality of chip stacks in the temporarily crimped state are formed according to the map.

10 **[0013]** In another preferred aspect, the following is further included: a plurality of disposition regions in which the chip stacks are disposed are set to be arranged in a lattice shape at a prescribed pitch P on the substrate, and the specifying step, after specifying the separation distance and when setting the separation distance as Dd, further specifies an integer N satisfying $\{(N-1) \times P\} \leq Dd < N \times P$, and in the temporary crimping step, the chip stacks in the temporarily crimped state are formed with N disposition regions
15 therebetween.

[0014] In another preferred aspect, the substrate is a semiconductor wafer.

[0015] Another method of manufacturing a semiconductor device of the disclosure is including: a temporary crimping step of sequentially laminating one or more semiconductor chips in each of two or more locations on a substrate while temporarily
20 crimping the one or more semiconductor chips to thereby form chip stacks in a temporarily crimped state; and a permanent crimping step of repeating twice or more a process of simultaneously heating and pressurizing top surfaces of the two or more chip stacks in the temporarily crimped state and simultaneously performing permanent crimping to change all of the chip stacks in the temporarily crimped state formed in the
25 temporary crimping step to a permanently crimped state, wherein the method repeats the

mark as a reference for positioning. The camera images the substrate 30 and the semiconductor chip 10 so that the alignment marks are reflected. The control part 130 grasps the relative positional relationship between the substrate 30 and the semiconductor chip 10 based on the image data obtained by this imaging and adjusts the rotation angle
5 of the mounting head 122 around the rotation axis Rb and the horizontal position of the stage 120 according to the needs.

[0028] The control part 130 controls the driving of each part and includes, for example, a CPU which performs various calculations and a memory part 138 which stores various data and programs. The control part 130 functions as a temporary crimping part 132, a
10 permanent crimping part 134, and a separation distance specifying part 136 by reading programs from the memory part 138. The temporary crimping part 132 drives the bonding part 106 to sequentially laminate one or more semiconductor chips while temporarily crimping them to form a chip stack in a temporarily crimped state. The permanent crimping part 134 drives the bonding part 106 and heats and pressurizes a top
15 surface of the chip stack formed in the temporarily crimped state, thereby collectively permanently crimping the one or more semiconductor chips which form each chip stack. The separation distance specifying part 136 specifies a separation distance prior to the temporary crimping. The separation distance, which will be described in detail later, is a separation distance of the chip stack in the temporarily crimped state, which is
20 necessary for well laminating the semiconductor chips 10.

[0029] In addition, the configuration of the mounting device 100 described here is an example and may be changed as appropriate. For example, in the embodiment, both the temporary crimping and the permanent crimping are performed by one mounting head 122, but a mounting head for the temporary crimping and a mounting head for the
25 permanent crimping may be provided. Further, in the embodiment, the stage 120 is

disposition regions 34. Furthermore, the mounting procedure described below may be performed under normal pressure or may be performed in a vacuum to prevent inclusion of air bubbles and the like.

[0040] In the embodiment, a temporary crimping step of forming two or more chip stacks ST in the temporarily crimped state and a permanent crimping step of permanently crimping the two or more chip stacks ST sequentially are repeated to mount the plurality of chip stacks ST.

[0041] Specifically speaking, first, at the beginning, as shown in (a) of FIG. 5, the mounting head 122 is used to dispose the semiconductor chip 10 in the region A on the substrate 30. At this time, the substrate 30 is positioned with respect to the semiconductor chip 10 so that the bumps 18 of the semiconductor chip 10 face electrode terminals 32 on the substrate 30. In addition, at this time, the mounting head 122 is heated to the first temperature T1 which is the temperature for temporary crimping. Next, as shown in (b) of FIG. 5, the semiconductor chip 10 is pressurized with the prescribed first load F1 by the mounting head 122, and the semiconductor chip 10 is temporarily crimped to the substrate 30. At this time, the NCF 20 is heated to the softening start temperature Ts or more by the heat transfer from the mounting head 122 and exhibits appropriate fluidity. In this way, the NCF 20 fills the gap between the semiconductor chip 10 and the substrate 30 without any gap. In addition, the first load F1 is not particularly limited as long as the amount of the first load F1 allows the bumps 18 to contact the electrode terminals 32 of the substrate 30 by pushing away the softened NCF 20 without significantly deforming the bumps 18.

[0042] When the first-layer semiconductor chip 10 can be temporarily crimped, then the second-layer semiconductor chip 10 is further temporarily crimped onto the temporarily crimped first-layer semiconductor chip 10. When the second-layer

semiconductor chip 10 is being temporarily crimped, the same as the case in the first-layer semiconductor chip 10, the mounting head 122 is used to dispose the second-layer semiconductor chip 10 on the first-layer semiconductor chip 10 so that the bumps 18 of the second-layer semiconductor chip 10 face the electrode terminals 16 of the first-layer semiconductor chip 10. Then, in this state, the second-layer semiconductor chip 10 is heated at the first temperature T1 and pressurized with the first load F1 to be temporarily crimped to the first-layer semiconductor chip 10.

[0043] Thereafter, similarly, the third-layer semiconductor chip 10 is temporarily crimped onto the second-layer semiconductor chip 10, and the fourth-layer semiconductor chip 10 is temporarily crimped onto the third-layer semiconductor chip 10. (c) of FIG. 5 shows a mode in which the four layers of semiconductor chips 10 are laminated in the region A while being temporarily crimped. A laminate body in which the four semiconductor chips 10 are laminated becomes the chip stack ST in the temporarily crimped state.

[0044] When the chip stack ST in the temporarily crimped state can be formed in the region A, the chip stack ST in the temporarily crimped state is also formed in another disposition region 34 in the same procedure. However, at this stage, the chip stack ST in the temporarily crimped state is not formed in the region B but is formed in the region C in order to make the distance between the chip stacks ST in the temporarily crimped state to be the separation distance Dd or more. (c) of FIG. 6 shows a mode in which the chip stacks ST in the temporarily crimped state are formed in two or more disposition regions 34 (the region A and the region C). At this stage, a crimping step for the first time is completed.

[0045] After the crimping step is completed, subsequently, the chip stacks ST formed in the temporarily crimped state are permanently crimped sequentially. Specifically, as

shown in (b) of FIG. 6, first, the mounting head 122 is heated to the second temperature T2 which is the temperature for permanent crimping. Then, as shown in (b) of FIG. 6, the chip stack ST in the temporarily crimped state is pressurized with the second load F2 by the mounting head 122 heated to the second temperature T2, and the four semiconductor chips 10 are permanently crimped collectively. The second load F2 is not particularly limited as long as the pressing amount of the bumps 18 can be properly maintained.

[0046] By being pressed by the mounting head 122 heated to the second temperature T2, the four semiconductor chips 10 forming the chip stack ST are also heated. However, the heating temperature decreases as the distance from the mounting head 122 increases. Specifically, the uppermost-layer (fourth-layer) semiconductor chip 10 is heated to substantially the same temperature as the second temperature T2, but the lowermost-layer (first-layer) semiconductor chip 10 is heated to a lower layer temperature $T_a = T_2 - \Delta T$, which is less than the second temperature T2 by ΔT . The second temperature T2 is set so that the lower layer temperature T_a becomes a target temperature greater than the melting temperature T_m and the curing start temperature T_t . That is, at the time of permanent crimping, all the four semiconductor chips 10 forming the chip stack ST are heated to a temperature greater than the melting temperature T_m and the curing start temperature T_t .

[0047] Each semiconductor chip 10 is heated to above the curing start temperature T_t , whereby the NCF 20 of the semiconductor chip 10 gradually cures. Then, by curing the NCF 20, the semiconductor chip 10 and the crimped body (the substrate 30 or the lower semiconductor chip 10) are firmly fixed mechanically. In addition, the bumps 18 can be melted and glued to the opposite electrode terminals 32 and 16 by being heated to above the melting temperature T_m . Then, in this way, the four semiconductor chips 10 and the substrate 30 become to be in a mounting state in which they are electrically bonded to

each other. Then, the step of collectively permanently crimping the four semiconductor chips 10 which form the chip stack ST becomes the permanent crimping step.

[0048] However, the heat transferred to the lower layer is also transferred to the vicinity via the substrate 30 (the semiconductor wafer) with a high thermal conductivity.

5 Due to the heat transferred via the substrate 30, other chip stacks ST in the vicinity may be adversely affected. In order to avoid such an adverse effect due to the heat, in the embodiment, the chip stacks ST in the temporarily crimped state are separated by the separation distance Dd or more, which will be described in detail later.

[0049] When one chip stack ST can be permanently crimped, then another chip stack
10 ST is also permanently crimped. That is, the permanent crimping is sequentially performed in all of the two or more disposition regions 34 such as the region C and the like. Then, when all the chip stacks ST formed in the temporarily crimped state have all been permanently crimped, subsequently, the temporary crimping step for the second time is performed. That is, the chip stacks ST in the temporarily crimped state are
15 formed in the disposition regions where the chip stacks ST are not formed in the temporary crimping step for the first time, such as the region B and the like in the example of FIG. 6. (c) of FIG. 6 is a diagram showing the mode of the temporary crimping step for the second time. As in the temporary crimping step for the first time, when the chip stacks ST in the temporarily crimped state can be formed in two or more
20 disposition regions, then the permanent crimping step for the second time is performed for permanently crimping these chip stacks ST sequentially. Thereafter, the mounting process is completed by repeating the temporary crimping step and the permanent crimping step until the chip stacks ST can be mounted in all the desired disposition regions.

25 **[0050]** As is clear from the above description, the embodiment uses the parallel

[0065] That is, as shown in the upper left of FIG. 10, in the case of forming the chip stack ST in the temporarily crimped state in the region A in the temporary crimping step for the first time, the regions C and I which skip one disposition region 34 in the longitudinal direction and the transverse direction viewed from the region A and the region K which is separated from the regions C and I by one region are also formed with the chip stacks ST in the temporarily crimped state. Then, when the chip stacks ST in the temporarily crimped state can be formed in the regions A, C, K, and I, subsequently, these four chip stacks ST are permanently crimped sequentially. Even though the permanent crimping has been performed, since other chip stacks ST in the temporarily crimped state are not present in the regions where the substrate 30 is at a high temperature (the regions less than the separation distance Dd), undesirable thermal changes such as unintended curing of the NCF 20 and melting of the bumps 18 can be prevented.

[0066] In the temporary crimping step for the second time, the chip stacks ST in the temporarily crimped state are formed in the open disposition regions 34. For example, in the case of forming the chip stack ST in the temporarily crimped state in the region B in the temporary crimping step for the second time, the regions D and J which skip one disposition region 34 in the longitudinal direction and the transverse direction viewed from the region B and the region L which is separated from the regions D and J by one region are also formed with the chip stacks ST in the temporarily crimped state. Then, when the chip stacks ST in the temporarily crimped state can be formed in the regions B, D, L and J, subsequently, these four chip stacks ST are permanently crimped sequentially. That is, the permanent crimping step for the second time is performed. At this time, in the vicinity of the chip stack ST being permanently crimped, such as in the regions A and C which are in the vicinity of the chip stack ST in the region B, other chip stacks ST are

time of the entire mounting process can be further reduced. Further, in this case, since the chip stacks in the temporarily crimped state not to be permanently crimped simultaneously are separated by the separation distance Dd or more, unintended curing of the NCF 20 and melting of the bumps 18 can be effectively prevented.

- 5 **[0072]** In addition, in the above description, each chip stack ST is described as four layers, but the number of lamination in the chip stack ST is not particularly limited as long as it is one or more. Moreover, in the above description, a semiconductor wafer is used as the substrate 30, but other substrates may be used. However, the technique of the embodiment is particularly suitable to a case in which a substrate made of a material
- 10 with a relatively high thermal conductivity is used.

WHAT IS CLAIMED IS:

Claim 1. A method of manufacturing a semiconductor device in which one or more semiconductor chips are laminated and mounted in a plurality of locations on a substrate, comprising:

5 a temporary crimping step of sequentially laminating the one or more semiconductor chips in each of two or more locations on the substrate while temporarily crimping the one or more semiconductor chips to thereby form chip stacks in a temporarily crimped state; and

 a permanent crimping step of sequentially heating and pressurizing top surfaces
10 of all of the chip stacks formed in the temporarily crimped state to thereby collectively permanently crimp the one or more semiconductor chips which form each of the chip stacks,

 wherein the method

 repeats the temporary crimping step and the permanent crimping step twice or
15 more until a desired number of the chip stacks are reached,

 further comprises a specifying step prior to the temporary crimping step for specifying a separation distance which is a distance from the chip stacks under permanent crimping to a location at which a temperature of the substrate, the temperature having been raised by heating for the permanent crimping, becomes less than or equal to
20 a prescribed permissible temperature,

 in the temporary crimping step, forms the chip stacks in the temporarily crimped state to be separated from each other by the separation distance or more, and

 in the permanent crimping step, permanently crimps the chip stacks which are in the temporarily crimped state and are formed separated from each other by the separation
25 distance or more.

Claim 2. The method of manufacturing a semiconductor device according to claim 1, wherein the specifying step specifies the separation distance based on mounting conditions of the semiconductor chips.

Claim 3. The method of manufacturing a semiconductor device according to
5 claim 2, wherein a lower layer temperature which is a temperature of lowermost layers of the chip stacks when the permanent crimping step is performed is comprised,

in the specifying step, the separation distance is specified so that the separation distance becomes greater as the lower layer temperature is greater.

Claim 4. The method of manufacturing a semiconductor device according to any
10 one of claims 1 to 3, wherein

a thermosetting resin is provided on an end surface at one side of the semiconductor chip in a laminating direction for fixing the semiconductor chip to the substrate or to another semiconductor chip mounted adjacent to the one side in the laminating direction, and

15 the permissible temperature is less than a curing start temperature at which the thermosetting resin starts to cure irreversibly.

Claim 5. The method of manufacturing a semiconductor device according to any one of claims 1 to 4, further comprising:

a map forming step of forming a map indicating formation positions of the
20 plurality of chip stacks based on the specified separation distance,

wherein in the temporary crimping step, the plurality of chip stacks in the temporarily crimped state are formed according to the map.

Claim 6. The method of manufacturing a semiconductor device according to any

one of claims 1 to 3, wherein

a plurality of disposition regions in which the chip stacks are disposed further set to be arranged in a lattice shape at a prescribed pitch P on the substrate,

the specifying step, after specifying the separation distance and when setting the
5 separation distance as Dd, further specifies an integer N satisfying $\{(N-1) \times P\} \leq Dd < N \times P$, and

in the temporary crimping step, the chip stacks in the temporarily crimped state are formed with N disposition regions therebetween.

Claim 7. The method of manufacturing a semiconductor device according to
10 claim 1, wherein the substrate is a semiconductor wafer.

Claim 8. A method of manufacturing a semiconductor device, comprising:

a temporary crimping step of sequentially laminating one or more
semiconductor chips in each of two or more locations on a substrate while temporarily
crimping the one or more semiconductor chips to thereby form chip stacks in a
15 temporarily crimped state; and

a permanent crimping step of repeating twice or more a process of
simultaneously heating and pressurizing top surfaces of the two or more chip stacks in
the temporarily crimped state and simultaneously performing permanent crimping to
change all of the chip stacks in the temporarily crimped state formed in the temporary
20 crimping step to a permanently crimped state,

wherein the method

repeats the temporary crimping step and the permanent crimping step twice or
more until a desired number of the chip stacks are reached,

further comprises a specifying step prior to the temporary crimping step for
25 specifying a separation distance which is a distance from the chip stacks under

permanent crimping to a location at which a temperature of the substrate, the temperature having been raised by heating for the permanent crimping, becomes less than or equal to a prescribed permissible temperature, and

in the temporary crimping step, forms the chip stacks in the temporarily crimped state not to be permanently crimped simultaneously to be separated from each other by the separation distance or more.

Claim 9. A mounting device for laminating and mounting one or more semiconductor chips in a plurality of locations on a substrate, comprising:

a temporary crimping means of sequentially laminating the one or more semiconductor chips in each of two or more locations on the substrate while temporarily crimping the one or more semiconductor chips to thereby form chip stacks in a temporarily crimped state;

a permanent crimping means of sequentially heating and pressurizing top surfaces of all of the chip stacks formed in the temporarily crimped state to thereby collectively permanently crimp the one or more semiconductor chips which form each of the chip stacks; and

a separation distance specifying means for specifying a separation distance prior to the temporary crimping, the separation distance being a distance from the chip stacks under permanent crimping to a location at which a temperature of the substrate, the temperature having been raised by heating for the permanent crimping, becomes less than or equal to a prescribed permissible temperature,

wherein the temporary crimping means forms the chip stacks in the temporarily crimped state to be separated from each other by the separation distance or more, and

the permanent crimping means permanently crimps the chip stacks which are in the temporarily crimped state and are formed separated from each other by the separation

distance or more.

Claim 10. A mounting device for laminating and mounting one or more semiconductor chips in a plurality of locations on a substrate, comprising:

5 a bonding part for sequentially laminating the one or more semiconductor chips in each of two or more locations on the substrate while temporarily crimping the one or more semiconductor chips to thereby form chip stacks in a temporarily crimped state and for sequentially heating and pressurizing top surfaces of all of the chip stacks formed in the temporarily crimped state to thereby collectively permanently crimp the one or more semiconductor chips which form each of the chip stacks;

10 a separation distance specifying means for specifying a separation distance prior to the temporary crimping, the separation distance being a distance from the chip stacks under permanent crimping to a location at which a temperature of the substrate, the temperature having been raised by heating for the permanent crimping, becomes less than or equal to a prescribed permissible temperature; and

15 a control part for controlling the bonding part so that after the chip stacks in the temporarily crimped state are formed separated from each other by the separation distance or more, the chip stacks formed in the temporarily crimped state are permanently crimped.

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